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Micron and submicron patterning of polydimethylsiloxane resists on electronic materials by decal transfer lithography and reactive ion-beam etching: Application to the fabrication of high-mobility, thin-film transistors

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We describe a technique for fabricating micron and submicron-sized polydimethylsiloxane (PDMS) patterns on electronic material substrates using decal transfer lithography (DTL) in conjunction with reactive ion-beam etching (RIE). We validate the use of this unconventional polymeric system as a suitable resist material for fabricating Si-based microelectronic devices. In this process, an O_2/CF_4 gas mixture was used to etch a supporting PDMS thin film that resides atop a closed-form decal polymer to reveal conventional resist structures. These structures provide an effective latent image that, in turn, provides for an extension of soft lithography as a form of multilayer lithography—one yielding submicron structures similar to those obtained from the conventional photochemical methods used to prepare such resists. This combined DTL/RIE patterning procedure was found to be compatible with commercially available planarization layers and provides a direct means for preparing high aspect ratio resist features. We illustrate the applicability of soft lithography as a means for fabricating electronic devices by using it to prepare model silicon-based thin-film transistors exploiting silicon-on-insulator wafer technology. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2356784]

I. INTRODUCTION

Soft lithography is a general term referring to high-resolution, nonphotolithographic patterning techniques based on printing, molding, or embossing processes that are carried out using a polydimethylsiloxane (PDMS) elastomeric "stamp."[1–4] The stamps can be prepared in various ways, although it is most typically carried out by casting prepolymers against masters patterned by conventional photolithographic techniques. Representative soft-lithographic techniques that have found varying degrees of attention in research and for possible applications in technology include microcontact printing (μCP),[5–7] replica molding (REM),[8,9] microtransfer molding (μTM),[10–13] micromolding in capillaries (MIMIC),[14–16] and solvent assisted micromolding (SAMIM).[17] These techniques are useful for fabricating a variety of functional components and devices for use in areas such as optics,[18,19] microelectronics,[20–22] microanalysis,[23–26] and microelectromechanical system (MEMS).[27] The work reported to date establishes the broad utility of PDMS as a foundation material for soft-lithographic patterning—its properties being exploited with benefit for myriad forms of contact-lithographic patterning and, more recently, as a component material for constructing the complex forms of MEMS and microfluidic devices.[28] The latter exploitations of PDMS provide an interesting counterpoint for the developments of soft lithography seen in microelectronics, where protocols that use it for printing tools have come to dominate.[29] Relatively little work has been done that exploits PDMS as a direct resist material. This omission is one that the current work addresses.

We recently reported a form of soft lithography, decal transfer lithography (DTL), that is based on the transfer of PDMS patterns to a substrate via the engineered adhesion and release properties of a compliant PDMS stamp.[30] The conventional DTL process appears to be most useful for delivering micron-sized PDMS patterns (ones that can be used as resists for subsequent processing) to flat or curved large area electronic materials such as silicon (Si), silicon dioxide (SiO_2), and other metal and metal-oxide thin films with high fidelity and low defect densities.[30,31] Submicron-sized patterns, however, are more difficult to transfer with high fidelity and low defect densities due to the limitations of the

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mechanical properties of the PDMS structures used to form the decal. To overcome this limitation, a second variant of the DTL technique was developed. This method, based on a cohesive mechanical failure (CMF) mechanism, exploits the transfer of PDMS patterns to a substrate via a sequence of interfacial adhesion and mechanical decohesion of the PDMS stamp:[32] submicron multilayer resist patterns have been fabricated in this way, but because the primary PDMS layers transferred are very thin (10–70 nm), secondary pattern transfer to an organic planarization layer must be carried out to generate any form of high aspect ratio structures as are commonly required for device fabrication processes. The present work describes means that can be used not only to create submicron-sized PDMS patterns in conventional resist structures but also in a direct way to pattern PDMS resist structures suitable for fabricating high performance Si-based thin-film transistors (TFTs). The method uses a PDMS thin-film membrane residing atop and supporting the patterned structures of the (closed-form) decal, followed by a reactive ion-beam etching (RIE) processing step to transfer that latent image to either a conventional resist material or more directly to an underlying single-crystalline Si microstructure.

II. EXPERIMENT

The general procedures used to fabricate the PDMS decals and bond them onto target substrates have been described previously in the literature.[30] Briefly, PDMS prepolymer (Dow Corning Sylgard 184) was spun cast onto a master bearing micron- and submicron-sized features (i.e., photoresist patterned silicon wafer) and cured at 70 °C. After curing, the PDMS coated master was exposed to UV/ozone (UVO) (mercury lamp from BHK, 173 μW/cm^2) and tridecafluoro-1,1,2,2-tetrahydrooctyl trichlorosilane ("no stick," Gelest). After UVO/no stick treatment, the PDMS coated master was covered with an additional thick layer of PDMS prepolymer, which was then cured in an oven at 70 °C [Fig. 1(a)(i)]. After the PDMS stamp was extracted from the master, the patterned PDMS film was exposed to UVO for 150 s, placed in contact with the substrate [i.e., glass slide (Gold Seal), silicon (Silicon Sense Inc.), SiO_2, or other materials promoted with an Al/SiO_2 adhesion layer] and baked at 70 °C for 20 min [Fig. 1(a)(ii)].[33] The closed PDMS decal was transferred to the substrate by simply peeling away the supporting PDMS layer [Fig. 1(a)(iii)]. In the last step, the top layer of the PDMS decal was removed by RIE [Uniaxis 790, 300 mTorr of total gas pressure, 5 SCCM (SCCM denotes standard cubic centimeter per minute at STP) O_2 and 35 SCCM CF_4 gas flow rates, and 200 W of rf power] to give conventional discrete resist structures [Fig. 1(a)(iv)]. After etching, the surface of the PDMS decal was rinsed sequentially with ethanol, isopropyl alcohol, and de-ionized water and dried in a stream of high-purity nitrogen gas. Anisotropic etching of the planarization layer (PL) (Shipley 1805) was carried out using 20 mTorr of total gas pressure, a 10 SCCM O_2 gas flow rate, and 100 W of rf power. Scanning electron microscopy (SEM) was performed with a Philips XL30 ESEM-FEG or a Hitachi S-4700 SEM.

Silicon-based transistors were fabricated from 1.5 $\times$ 1.5 cm pieces of silicon-on-insulator (SOI) wafers (SOITEC) using DTL and RIE. A SOI wafer was cleaned with isopropyl alcohol and acetone and dried in a stream of nitrogen gas prior to metal deposition. The cleaned SOI wafer was loaded immediately into an electron beam evaporator (Temescal, FC-1800) and 300 nm of Al and 10 nm of SiO_2 were sequentially deposited on the top silicon. A source-drain-patterned, closed-form decal was transferred onto the SiO_2/Al/Si substrate using the procedure described above. The top layer of the closed-form PDMS decal was removed by RIE using 300 mTorr of total gas pressure, 5 SCCM O_2 and 35 SCCM CF_4 gas flow rates, and 200 W of rf power. After removing the top layer, the sample was immersed in an aqueous HF [49% (aq), Fisher] for 5 s to remove the regions of the SiO_2 not protected by the decal. Next, the sample was rinsed with de-ionized water and immersed in an aluminum etchant (Cyantek Co., AL-11) for 30 s to remove the exposed Al. The sample was then rinsed with de-ionized water and immersed in 1*M* tetrabutylammonium fluoride (TBAF) (Al-

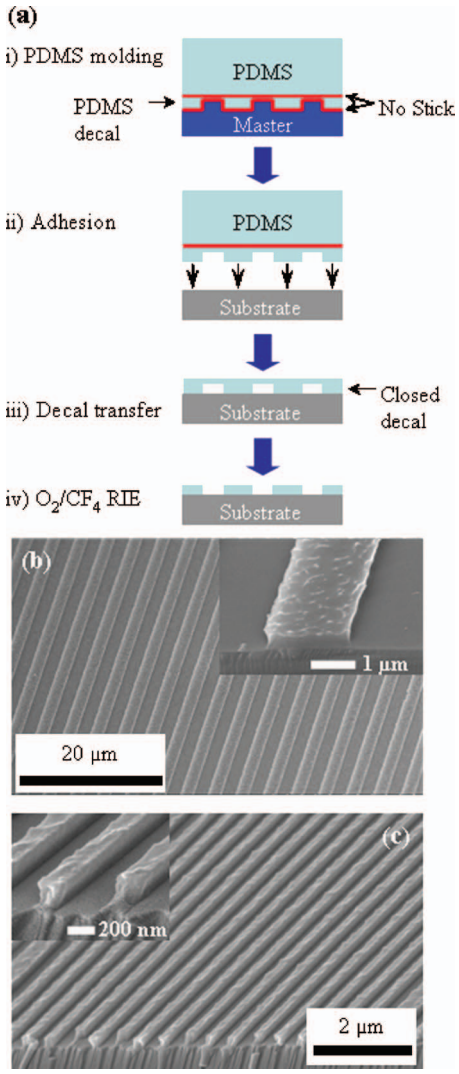

FIG. 1. (Color) (a) Schematic illustration of the procedure for preparing a closed-type PDMS decal and removing the top layer by RIE. SEM images of (b) 2 μm and (c) 300 nm wide PDMS lines on glass created by removing the top layer of closed PDMS decals by RIE. Insets are high resolution cross-sectional SEM images.

drich) solution in tetrahydrofuran (THF) for 2 min to remove the PDMS decal. In the last step, HF [49% (aq)] was used to remove the SiO_2 layer on the remaining Al microstructure. The electrical testing followed procedures described in the literature.[34]

III. RESULTS AND DISCUSSION

Figure 1(a) illustrates the procedure used to fabricate submicron, high-aspect-ratio resist features on a substrate. Specific details of the procedures used are given in the Experiment section. The key feature of this method consists of the development of a latent image of a resist pattern, one embedded within a closed-form decal.[30] As shown in Fig. 1(a), the irreversible bonding of a composite PDMS stamp to a substrate is followed by a mechanical debonding procedure to generate the nascent substrate-bonded decal. This decal is typically sealed by a thin PDMS membrane that is several microns thick (the latter being an explicit design rule of the decal). This overlaying membrane is then subsequently removed using an RIE process, thereby generating resist patterns suitable for use in subsequent fabrication processes. Oxygen plasmas are commonly used to etch hydrocarbon containing polymers.[35] In the case of PDMS, however, a thin SiO_2 layer is formed during the processing which serves to greatly impede its etching.[36] A fluorine-based plasma is required, therfore, to etch the capping PDMS membrane of the decal.[37] In this process, we employed an O_2/CF_4 gas mixture to etch back the PDMS membrane. Figures 1(b) and 1(c) show SEM images of representative 2 μm and 300 nm thick PDMS lines patterned as large area features after removing the top layer of a closed-type PDMS decal by RIE. In this case, the PDMS decal was transferred onto a glass substrate and the RIE performed at 300 mTorr of total gas pressure, with 5 SCCM O_2 and 35 SCCM CF_4 gas flow rates, at 200 W of rf power. This etching procedure rapidly ablated the capping membrane, leaving in its place a grasslike structure on the top of the PDMS exposed to the plasma. The formation of similar grasslike structures has been observed in the anisotropic etching of Si, GaAs, and a number of organic polymers.[38–40] Although the mechanism for the formation of these structures is not completely understood, Nam *et al.* have suggested that etching-rate anisotropies are amplified by defects or contaminants underlay their growth.[40] In this model, the etching rate of material in the vicinity of a defect or impurity (the tip) is thought to be slower than that of the bulk material. The grasslike filaments, thus, grow vertically as the etching proceeds. We found that for the Sylgard 184 PDMS polymer used in this study, the characteristic shapes of the filaments obtained are very sensitive to the etching procedures used. Less anisotropic etching conditions (e.g., higher pressures and/or lower power) led to finer scale structures but no conditions we examined fully eliminated them. We found, however, that the grasslike structures can be easily removed by sequentially rinsing with acetone, isopropyl alcohol, and de-ionized water and then drying the sample in a high-purity nitrogen gas stream. The structures shown in Figs. 1(b) and 1(c) were obtained in this way. We also found (but did not extensively explore) that other forms of PDMS were less prone to form the fibular structures under all etching conditions. Specifically, an experimental PDMS (Nano-Print Silicone from Dow Corning) yielded resists presenting significantly fewer fibril-like structures. This PDMS is more densely cross-linked than Sylgard 184 and has a Young's modulus of 5.4 MPa.

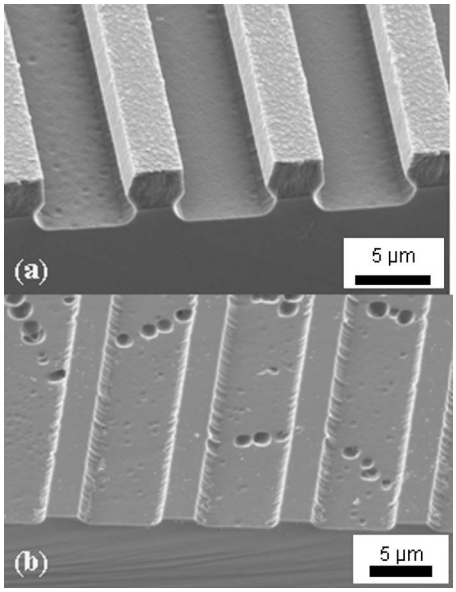

FIG. 2. (a) SEM image of 5 μm wide PDMS lines patterned on Si(100) after removing the top layer of a closed PDMS decal by RIE. The sample was rinsed with isopropyl alcohol, acetone, and de-ionized water and dried under pure nitrogen gas stream. (b) SEM image of the same silicon surface after removing the PDMS by TBAF.

We explicitly evaluated, as part of this work, the suitability of directly using PDMS decals of the form shown in Fig. 1 as resist materials for fabricating high performance silicon semiconductor devices. Two features of the process led us to develop modifications that explicitly empower the processing of Si-based devices. The elastomeric nature of PDMS greatly restricts the aspect ratios, pitches, and spacings of dimensionally stable (freestanding) structures that can be accommodated in patterns derived from it.[1,41] This could limit the scope of fabrication methods that use such resist structures. Closed-formed decals (see Fig. 1) remove this constraint by stabilizing the nascent resist features with the covering membrane layer. This layer has to be removed and this engenders its own potentially adverse impacts, namely, that PDMS is an exceptionally difficult material to etch. The processes required to etch back the membrane sealing the closed-form decal are, as a result, exceptionally damaging to any Si-based material lying below the regions opened by the plasma. For example, when a closed PDMS decal is transferred directly onto a silicon substrate and subsequently etched using an O_2/CF_4 RIE plasma to remove the top membrane layer, the silicon substrate is also invariably damaged (results shown in Fig. 2). To prevent this, a 200 nm thick film of aluminum (Al) was deposited onto the silicon substrate. This layer acts as an extremely effective etch stop towards the plasma used to effect the membrane removal by RIE. The DTL method works poorly on Al, however, and for this reason a 10 nm thick layer of silicon dioxide (SiO_2) film

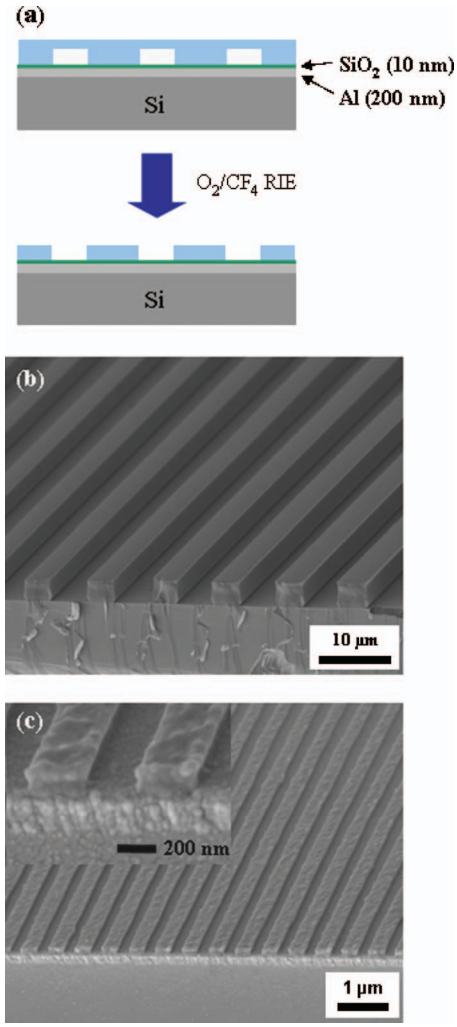

FIG. 3. (Color) (a) Schematic illustration of the procedure for preparing the PDMS decal on a $SiO_2/Al/Si(100)$ substrate and removing the top PDMS layer by RIE. SEM images of (b) 5 μm and (c) 300 nm wide PDMS lines patterned on $SiO_2/Al/Si(100)$ after removing the top layer of closed PDMS decals by RIE. Inset is a high resolution cross-sectional SEM image.

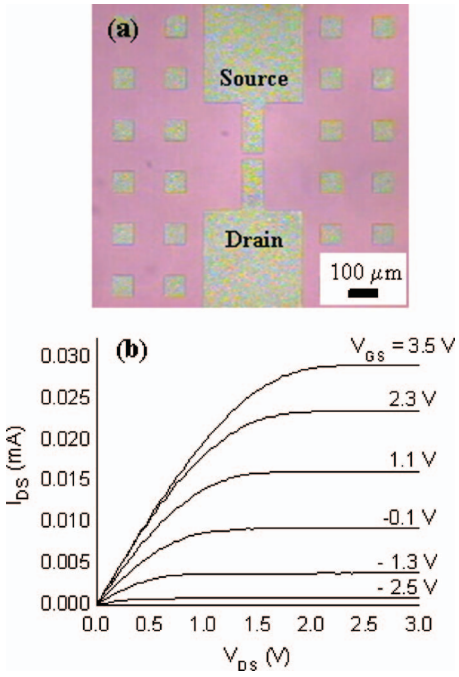

FIG. 4. (Color) (a) An optical micrograph of a silicon transistor fabricated from SOI using a combination of DTL and RIE. (b) Current-voltage (*I-V*) characteristics of the transistor fabricated by this methodology. I_{DS}, V_{DS}, and V_{GS} correspond to drain current, drain-to-source voltage, and gate-to-source voltage, respectively.

was deposited on top of the Al layer by an e-beam evaporation protocol to promote the adhesive transfer of the PDMS decal [Fig. 3(a)]. Figures 3(b) and 3(c) present SEM images of 5 μm and 300 nm wide PDMS lines patterned on such a $SiO_2/Al/Si$ multilayer substrate after removal of the top PDMS layer by RIE. These data suggest that the thin Al layer fully protects the silicon substrate from damage engendered by the RIE processing step. A control experiment in which only the SiO_2 layer was deposited did not show a similar protective capacity.

The results described above encouraged us to examine the utility of this form of soft lithography as a potentially efficient method for the fabricating important forms of microelectronics devices.[20–22,42,43] To do so, we carried out a process sequence yielding silicon-based thin-film transistors using SOI source wafers as a model system. The details of the procedures used to fabricate these transistors are given in the Experiment section. In order to simplify the process flows, we did not dope the source or drain contact regions of the device. For this reason,[44] we adopted a somewhat larger channel length for the TFT devices (50 μm) than the length corresponding to the 0.3 μm feature sizes shown above. Figure 4(a) shows an optical micrograph of one transistor embedded in a large area array of identical devices. Figure 4(b) shows representative current-voltage (*I-V*) characteristics of the devices fabricated using this methodology. A quantitative analysis of the electrical data showed that the devices exhibited mobilities of 97 cm^2/V s at a constant source-drain voltage (V_{ds}=0.5 V). These performance characteristics, while not optimized, are of the order expected for 0.145 μm thick SOI bottom gate TFTs with channel lengths of this size using undoped source-drain contacts.[45]

The combination of the DTL and RIE procedures described above also was found to be compatible with the PLs that are commonly used in commercial microelectronics fabrication processes. Multilayer lithography (i.e., bilayer and trilayer) methods have been developed by the microelectronics industry and provide critical process improvements that are required both to achieve higher resolution (e.g., by smoothing underlying substrate topography) and provide higher-aspect-ratio resist structures after etching.[39] For bilayer lithography, a resist structure is coated directly on top of the PL. For trilayer lithography, a resist is coated on top of an additional etch mask layer, which in turn is coated (or deposited) on the PL. Photoresists and spin-on-glass materials have been widely used as PL materials, with the former finding more extensive use given its ability to provide a more planar surface.[46] In this work, we modeled a multilayer lithography process exploiting DTL for the pattern transfer step using a 400 nm thick layer of PL (Microposit 1805) that was cast by spinning onto a Si substrate at 5500 rpm for 30 s, as illustrated in the process scheme given in Fig. 5. We used a 5 nm thick layer of SiO_2 as an adhesion layer for the

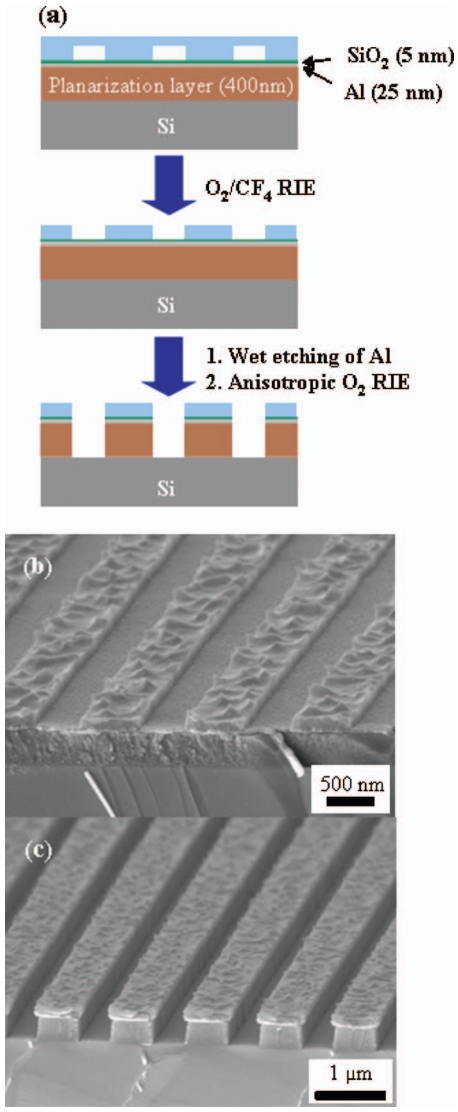

FIG. 5. (Color) (a) Schematic illustration of the procedure for preparing submicron, high aspect ratio resist structures on a silicon substrate using a combination of DTL and RIE. (b) Cross-sectional SEM image of 500 nm PDMS lines on SiO_2/Al/PL/Si(100) substrate after removing the top layer of a closed PDMS decal by RIE. (c) Cross-sectional SEM image of the resulting PDMS/SiO_2/Al/PL resist structures on a silicon substrate that corresponds to (a) (iii).

decal and a 25 nm thick layer of Al as an etch stop. These layers were deposited in sequence onto the PL by electron beam evaporation. Figure 5(b) shows a cross-sectional SEM image of representative 500 nm PDMS lines transferred onto a SiO_2/Al/PL/Si substrate after removing the top layer of the closed PDMS decal by RIE. The total area patterned for this demonstration was about 1 cm^2 in size. As seen in this figure, the 25 nm thick Al layer is still intact and served as an etch stop for the O_2/CF_4 RIE process step. In the following step [Fig. 5(a)], the exposed Al/PL layer was subsequently removed by a sequence of wet etching and anisotropic O_2 RIE. This process yielded the higher aspect ratio of 0.5 Si-supported resist features shown in Fig. 5(c).

The data presented above demonstrated an interesting quality when examined in the context of other nonphotolithographic methods, which provide capacities for submicron patterning of large area resist features, most notable of which are imprint lithographies (Fig. 6).[47,48] The latter methods have been shown to provide extremely high quality resist structures, ones with feature sizes that extend far below 0.1 μm.[48] Imprint lithographies using liquid organic prepolymers that are photocured against a hard mask that also serves as a mold, appear to hold special promise for commercialization.[49] These methods,[48,50,51] and DTL, provide polymer microstructures (the resist patterns) that share a common feature—a residual (and sometimes thick) layer of polymer that connects the resist features. In imprint lithography, this material is subsequently removed using an anisotropic RIE processing step. As shown in Fig. 6, this aspect of the procedure closely resembles the etch-back step used in the DTL-based process, with the exception that the PDMS membrane initially rests atop the nascent resist structures.

The point above implicitly addresses one of the more challenging problems associated with PDMS-based elastomeric pattern transfers, namely, that the features tend to deform and the recesses of the relief collapse. These effects limit the size of the area that can be generated without significant registration errors occurring and are magnified by strains induced in the stamp during printing from mechanical handling.[42] This problem can be addressed and minimized

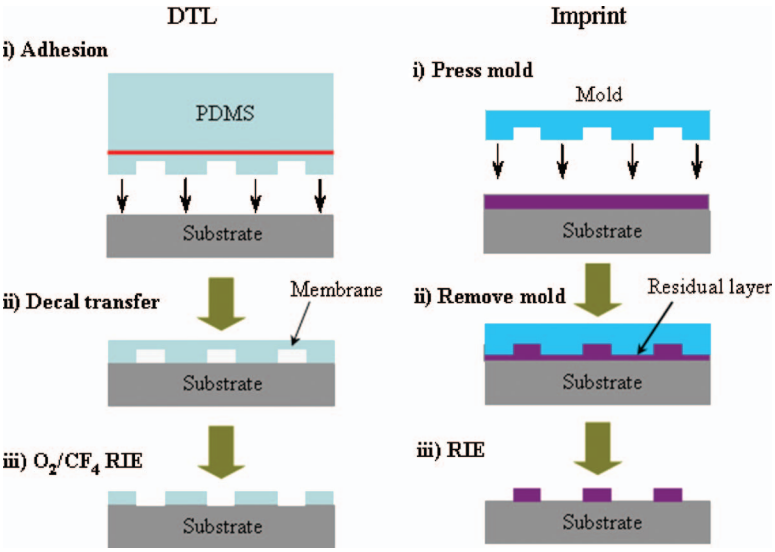

FIG. 6. (Color) Schematic illustrations of the procedure for fabricating resist structures using decal transfer lithography and imprint technique.

through the use of composite stamps[52] or solid backings,[53] enabling larger areas to be patterned. Stamp collapse can limit the spacing of the features, however, with the method described here this is not a critical design limit because the thin PDMS membrane is removed by the RIE. DTL methods have been demonstrated as an effective method for patterning micron-scale features over areas as large as the masters accessible to the conventional laboratory scale for fast prototyping methods ($\geqslant 25\ \mathrm{cm}^2$) with very low density of defects.[31] Other modifications of soft-lithographic patterning methods have been demonstrated on larger areas ($256\ \mathrm{cm}^2$), albeit with somewhat larger design rules.[42]

At this stage of its development, we have not used the DTL method to generate feature sizes that are smaller than the 0.3 μm demonstration provided here. This limitation, however, is one due to the mastering protocol (a phase shift lithography process) used to generate the mold for the decal.[54] We do not see any reasons based on intrinsic materials properties that would preclude extending the method to much smaller feature sizes.

IV. CONCLUSION

In summary, we describe a technique for fabricating micron- and submicron-sized polydimethylsiloxane (PDMS) resist patterns on electronic material substrates using decal transfer lithography (DTL) which, in conjunction with reactive ion-beam etching (RIE), appears to hold interesting promise as a soft-lithographic patterning scheme for electronic devices. The method complements imprint lithographies based on molding and embossing and provides a variation for multilayer lithography recently reported by us[32] that directly enables the fabrication of electronic devices.

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[1] Y. Xia and G. M. Whitesides, Annu. Rev. Mater. Sci. **28**, 153 (1998); J. A. Rogers and R. G. Nuzzo, Mater. Today **8**, 50 (2005).
[2] B. Michel *et al.*, IBM J. Res. Dev. **45**, 697 (2001); C. A. Mirkin and J. A. Rogers, MRS Bull. **26**, 506 (2001).
[3] H. Schmid, H. Wolf, R. Allenspach, H. Riel, S. Karg, B. Michel, and E. Delamarche, Adv. Funct. Mater. **13**, 145 (2003); E. Menard, L. Bilhaut, J. Zaumseil, and J. A. Rogers, Langmuir **20**, 6871 (2004).
[4] S. Jeon, J.-U. Park, R. Cirelli, S. Yang, C. E. Heitzman, P. V. Braun, P. J. A. Kenis, and J. A. Rogers, Proc. Natl. Acad. Sci. U.S.A. **101**, 12428 (2004); J. Maria, S. Jeon, and J. A. Rogers, J. Photochem. Photobiol., A **166**, 149 (2004).
[5] A. Kumar and G. M. Whitesides, Appl. Phys. Lett. **63**, 2002 (1993).
[6] A. Kumar, N. L. Abbott, E. Kim, H. A. Biebuyck, and G. M. Whitesides, Acc. Chem. Res. **28**, 219 (1995).
[7] N. B. Larsen, H. Biebuyck, E. Delamarche, and B. J. Michel, J. Am. Chem. Soc. **119**, 3017 (1997).
[8] Y. Xia, E. Kim, X.-M. Zhao, J. A. Rogers, M. Prentiss, and G. M. Whitesides, Science **273**, 347 (1996).
[9] Y. Xia, J. J. McClelland, R. Gupta, D. Qin, X.-M. Zhao, L. L. Shon, R. J. Celotta, and G. M. Whitesides, Adv. Mater. (Weinheim, Ger.) **9**, 147 (1997).
[10] X.-M. Zhao, Y. Xia, and G. M. Whitesides, Adv. Mater. (Weinheim, Ger.) **8**, 837 (1996).
[11] P. M. Moran and F. F. Lange, Appl. Phys. Lett. **74**, 1332 (1999).
[12] R. C. Bailey, K. J. Stevenson, and J. T. Hupp, Adv. Mater. (Weinheim, Ger.) **12**, 1930 (2000).
[13] M. Cavallini, M. Murgia, and F. Biscarini, Nano Lett. **1**, 193 (2001).
[14] E. Kim, Y. Xia, and G. M. Whitesides, Nature (London) **376**, 581 (1995).
[15] E. Kim, Y. Xia, and G. M. Whitesides, J. Am. Chem. Soc. **118**, 5722 (1996).
[16] W. S. Beh, I. T. Kim, D. Qin, Y. Xia, and G. M. Whitesides, Adv. Mater. (Weinheim, Ger.) **11**, 1038 (1999).
[17] E. Kim, Y. Xia, X.-M. Zhao, and G. M. Whitesides, Adv. Mater. (Weinheim, Ger.) **9**, 651 (1997).
[18] B. J. Scott, G. Wirnsberger, M. D. McGehee, B. F. Chmelka, and G. D. Stucky, Adv. Mater. (Weinheim, Ger.) **11**, 37 (1999).
[19] J. A. Rogers, R. J. Jackman, G. M. Whitesides, J. L. Wagener, and A. M. Vengsarkar, Appl. Phys. Lett. **70**, 7 (1997).
[20] N. L. Jeon, P. G. Clem, D. Y. Jung, W. B. Lin, G. S. Girolami, and D. A. Payne, Adv. Mater. (Weinheim, Ger.) **9**, 891 (1997).
[21] N. L. Jeon, J. Hu, G. M. Whitesides, M. K. Erhardt, and R. G. Nuzzo, Adv. Mater. (Weinheim, Ger.) **10**, 1466 (1998).
[22] M. K. Erhardt and R. G. Nuzzo, Langmuir **15**, 2188 (1999).
[23] M. A. Unger, H. Chou, T. Thorsen, A. Scherer, and S. R. Quake, Science **288**, 113 (2000).
[24] A. Bernard, B. Michel, and E. Delamarche, Anal. Chem. **73**, 8 (2001).
[25] E. Eteshola and D. Leckband, Sens. Actuators B **72**, 129 (2001).
[26] T. Deng, M. Prentiss, and G. M. Whitesides, Appl. Phys. Lett. **80**, 461 (2002).
[27] T. Deng, G. M. Whitesides, M. Radhakrishnan, G. Zabow, and M. Prentiss, Appl. Phys. Lett. **78**, 1775 (2001); J. S. Kim and D. R. Knapp, J. Am. Soc. Mass Spectrom. **12**, 463 (2001).
[28] T. Thorsen, S. J. Maerkl, and S. R. Quake, Science **298**, 580 (2002); S. Deladi, V. Svetovoy, G. Krijnen, and M. Elwenspoek, J. Micromech. Microeng. **14**, 1659 (2004).
[29] M. A. Meitl, Z. Zhu, V. Kumar, K. Lee, X. Feng, Y. Huang, R. G. Nuzzo, and J. A. Rogers, Nat. Mater. **5**, 33 (2006); K. Lee, M. J. Motala, M. A. Meitl, W. R. Childs, E. Menard, A. K. Shim, J. A. Rogers, and R. G. Nuzzo, Adv. Mater. (Weinheim, Ger.) **17**, 2336 (2005).
[30] W. R. Childs and R. G. Nuzzo, J. Am. Chem. Soc. **124**, 13583 (2002).
[31] W. R. Childs and R. G. Nuzzo, Adv. Mater. (Weinheim, Ger.) **16**, 1323 (2004); Langmuir **21**, 195 (2005).
[32] H. Ahn, K. J. Lee, A. Shim, J. A. Rogers, and R. G. Nuzzo, Nano Lett. **5**, 2533 (2005).
[33] Alternatively, it is possible to induce adhesion by irradiating an untreated stamp that has been placed in contact with a substrate from the back side using the same exposure source. This method, though, was subject to bonding failures that, while sporadic, were hard to eliminate.
[34] B. G. Streetman and S. Banerjee, *Solid State Electronic Devices* (Prentice-Hall, Englewood Cliffs NJ, 2000).
[35] G. N. Taylor and T. M. Wolf, Polym. Eng. Sci. **20**, 1087 (1980); M. A. Hartney, D. W. Hess, and D. S. Soane, J. Vac. Sci. Technol. B **7**, 1 (1989).
[36] N. J. Chou, C. H. Tang, J. Parazczak, and E. Babich, Appl. Phys. Lett. **46**, 31 (1985).
[37] J. Garra, T. Long, J. Currie, T. Schneider, R. White, and M. Paranjape, J. Vac. Sci. Technol. B **20**, 975 (2002).
[38] H. Jansen, M. Legtenberg, R. de Boer, and M. Elwenspoek, J. Micromech. Microeng. **5**, 115 (1995).
[39] A. J. Fleischman, C. A. Zorman, and M. Mehregany, J. Vac. Sci. Technol. B **16**, 536 (1998).
[40] P. S. Nam, L. M. Ferreira, T. Y. Lee, and K. N. Tu, J. Vac. Sci. Technol. B **18**, 2780 (2000).
[41] E. Delamarche, B. Michel, H. A. Biebuyck, and C. Gerber, Adv. Mater. (Weinheim, Ger.) **9**, 741 (1997).
[42] J. A. Rogers *et al.*, Proc. Natl. Acad. Sci. U.S.A. **98**, 4835 (2001).
[43] T. Deng, L. B. Goetting, J. M. Hu, and G. M. Whitesides, Sens. Actuators, A **86**, 122 (2000).
[44] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[45] S. Cristoloveanu, D. Munteanu, and M. S. Liu, IEEE Trans. Electron Devices **47**, 1018 (2000); J. B. Kuo and S. C. Lin, *Low-Voltage SOI CMOS VLSI Devices and Circuits* (Wiley-Interscience, New York, 2001).
[46] M. Madou, *Fundamentals of Microfabrication* (CRC, Boca Raton, FL, 1997).
[47] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, J. Vac. Sci. Technol. B **14**, 1429 (1996); S. Zankovych, T. Hoffmann, J. Seekamp, J.-U. Bruch, and C. M. Sotomayor Torres, Nanotechnology **12**, 91 (2001).
[48] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Science **272**, 85 (1996).
[49] D. J. Resnicka, S. V. Sreenivasan, and C. G. Willson, Mater. Today **8**, 34

(2005).
[50]K. H. Schlereth and H. Bötther, J. Vac. Sci. Technol. B **10**, 114 (1992).
[51]S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Appl. Phys. Lett. **67**, 3114 (1995).
[52]T. W. Odom, J. C. Love, D. B. Wolfe, K. E. Paul, and G. M. Whitesides, Langmuir **18**, 5314 (2002).
[53]J. A. Rogers, K. E. Paul, and G. M. Whitesides, J. Vac. Sci. Technol. B **16**, 88 (1998).
[54]J. A. Rogers, K. E. Paul, R. J. Jackman, and G. M. Whitesides, J. Vac. Sci. Technol. B **16**, 59 (1998).