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Enhanced electrical characteristics of Au nanoparticles embedded in high-*k* HfO_2 matrix

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We present experimental results for laser-induced Au nanoparticle (NP) embedded in a HfO_2 high-*k* dielectric matrix. Cross-sectional transmission electron microscopy images showed that the Au NPs of 8 nm in diameter were clearly embedded in HfO_2 matrix. Capacitance-voltage measurements of $Pt/HfO_2/Au\ NPs/HfO_2$ on *p*-type Si substrate reliably exhibited metal-oxide-semiconductor behavior with a large flatband shift of 4.7 V. In addition, the charge retention time at room temperature was found to exceed 10^5 h. This longer time was attributed to the higher electron barrier height via high work function of the Au NP. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2347703]

Recently, a type of nonvolatile memory using nanoparticles (NPs) as floating gates has attracted much research attention because of its excellent memory performance and high scalability.[1,2] By utilizing discrete NP as the charge storage element, NP memory is more immune to local oxide defects than flash memory, thus exhibiting longer retention time and allowing more aggressive tunnel oxide scaling than conventional flash memory.[3] So far, several techniques have been developed to form uniform NP in gate oxides because the device performance and reliability will depend on many factors, such as the ability to control NP size, size distribution, crystallinity, area density, oxide passivation quality, and the isolation that prevents lateral charge conduction in the NP layer.[3,4] Although a considerable number of studies concern the formation of NP embedded in gate oxide, yet each of these techniques has a few problems, such as density, uniformity, reproducibility, commercialization, etc.

In this Letter, we report a fabrication method for the Au NP by exposing a Nd:YAG (yttrium aluminum garnet) laser (wavelength=355 nm) on Si substrates. Primary emphasis is placed on the simple and direct fabrication of the Au NPs without performing any preciously well-known nanopattering or postannealing process. In this method, Au NP is easily formed from thin film with thicknesses of only a few nanometers. In particular, the average size of the Au NPs is simply controlled with an initially determined film thickness. Finally, as one of potential applications with Au NP, Au metal NPs fabricated by our laser exposure technique are embedded in a high-*k* HfO_2 dielectric matrix for nonvolatile memory applications, demonstrating a means to further improve the data retention. The HfO_2 barrier is chosen as a promising alternative gate dielectric because of its high permittivity (about 15–30) and excellent thermal stability.[5] The Au metal is selected due to its high work function (about 5.2 eV), good thermal stability, and resistance to oxidation.[6]

To clarify the structural properties of the Au NP, various measurements are taken using atomic force microscope (AFM), scanning electron microscope (SEM), and transmission electron microscope (TEM) both before and after the laser irradiation process. The memory effects of the Au NP embedded in a HfO_2 dielectric matrix are measured using capacitance, conductance, and retention characteristics.

Figure 1 present typical TEM images of the Au NP in various sizes, controlled by the initial thickness of the Au thin film. As shown in Fig. 1, 6 nm [(a) high resolution TEM, inset of (a), wide-range area], 8 nm [(b) and above right inset of (b)], and 10 nm [(c) and inset of (c)] Au NPs

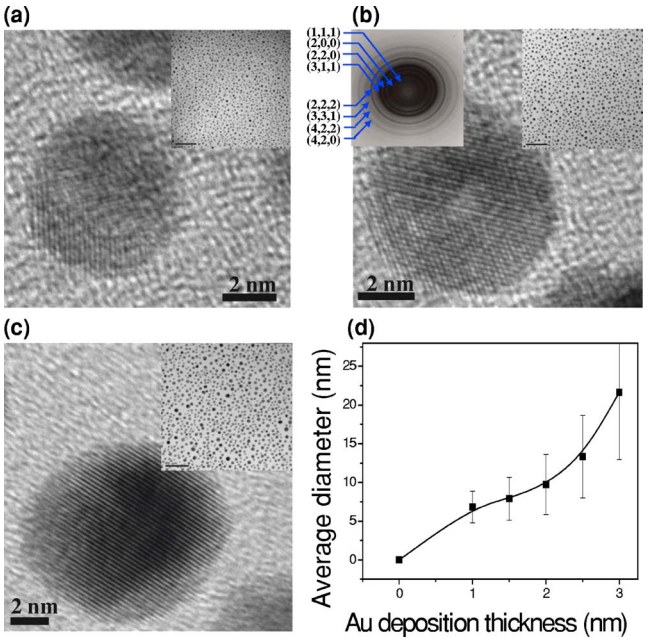

FIG. 1. (Color online) Plan-view TEM images of Au NP with different diameters: (a) 6 nm, (b) 8 nm, and (c) 10 nm NP. (d) Diameter of the Au NP as a function of initial Au thin film thickness. Inset images of (a) (b) and (c) are wide-area images and the above left inset in (b) is an electron diffraction pattern. The electron diffraction patterns confirm a face centered cubic structure for the Au NP.

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are fabricated with initial film thicknesses of 1, 1.5, and 2 nm, respectively. The average size variations of the Au NP in Figs. 1(a)–1(c) are about 30%, 35%, and 40%, respectively. Although the formation conditions of NP are dependent on the materials because of the differences in thermal and ultraviolet (UV: 355 nm) absorption coefficients between the different materials,[7] however, the optimum laser power of the Au NP was experimentally determined to be 0.05 W. Also, the Au NPs are not formed at powers less than 0.01 W or more than 0.2 W. We believe that the laser energy of below 0.01 W is not high enough to form the Au NP, and the high laser energy above 0.2 W easily etches out or burns the thin films. More detailed laser irradiation technique for formation of NP is described elsewhere.[8] As the initial thickness of the Au film was increased, the diameter of the Au NP also increased, as shown in Fig. 1(d). The high resolution TEM images of all Au NP reveal distinct lattice fringe patterns, indicating the highly crystalline nature of the Au NP. In addition, the electron diffraction patterns of the 8 nm Au NP were well matched to those of a face centered cubic structure, as shown in the upper left inset of Fig. 1(b). It is expected that our approach employed to get NP arises from the following simple process. When a pulsed laser beam is radiated on ultrathin films, the following steps occur in rapid succession: rapid heating of the ultrathin film by laser energy, almost all melting, weak vaporization and ionization, and then supercooling to form NPs in an extremely short time. In addition, it is expected that an optimal combination of laser processing and conventionally available annealing appears to accelerate various NPs of much higher crystal phases. Of the various experimental parameters, the initial thickness of the thin film is the most important factor for controlling the NP diameter due to the dependence of absorbed energy in each material on thickness. However, no NP was formed at film thickness more than 4 nm because thicker films do not perfectly segregate to form NP spontaneously.

Ultrathin high-k HfO_2 films were used as tunneling and control oxides. The tunneling oxide was prepared using an atomic layer deposition (ALD) system to allow reliable operation, such as low leakage current, while the control oxide was grown by utilizing an inductively coupled sputtering technique for simple growth and commercialization. The low laser power (0.05 W) used in this experiment did not affect the structural properties of the ALD-HfO_2 tunneling oxide due to the relatively high thermal stability of crystalline HfO_2. It is well known that HfO_2 exhibits good thermal stability, with a Gibbs free energy of about −260 kcal/mol.[5] Therefore, the reliability of laser annealing process is dependent on having tunneling oxide materials with a relatively high thermal stability in order to retain the tunneling oxide's required functional characteristics without having any damage during laser exposure. The existence of Au NP inside the high-k matrix was confirmed by a cross-sectional TEM micrograph, as shown in Fig. 2(a). The Au NP (8 nm average size) was distributed at a depth of about 10 nm from the Si substrate/HfO_2 interface. The thicknesses of tunnel oxide, control oxide, and interfacial layer between Si wafer and HfO_2 were approximately 10, 20, and 1.5 nm, respectively.

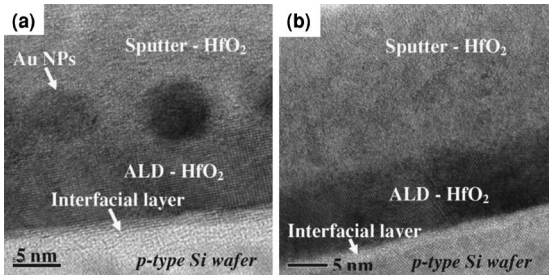

FIG. 2. Cross-sectional TEM images of MOS structure (a) with Au NP and (b) without Au NP, where the tunneling, control oxide, and interfacial layer thicknesses are 10, 20, and 1.5 nm, respectively.

As shown in Fig. 2(a), the Au NP were well isolated by the surrounding control oxide and Si substrate. This implies memory characteristics of electric charges through the Au NP. In our experiment, it was also found that the interface layer between the Si substrate and HfO_2 tunneling oxide did not exhibit any charging behavior. Figure 2(b) shows cross-sectional TEM images of the sample without any Au NP inside the HfO_2 matrix for comparison measurements.

The high-frequency (1 MHz) capacitance-voltage (C-V) curves of the metal-oxide-semiconductor (MOS) devices are shown in Fig. 3. Figure 3(a) shows the C-V curve of the MOS structure without the Au NP (device A). Device

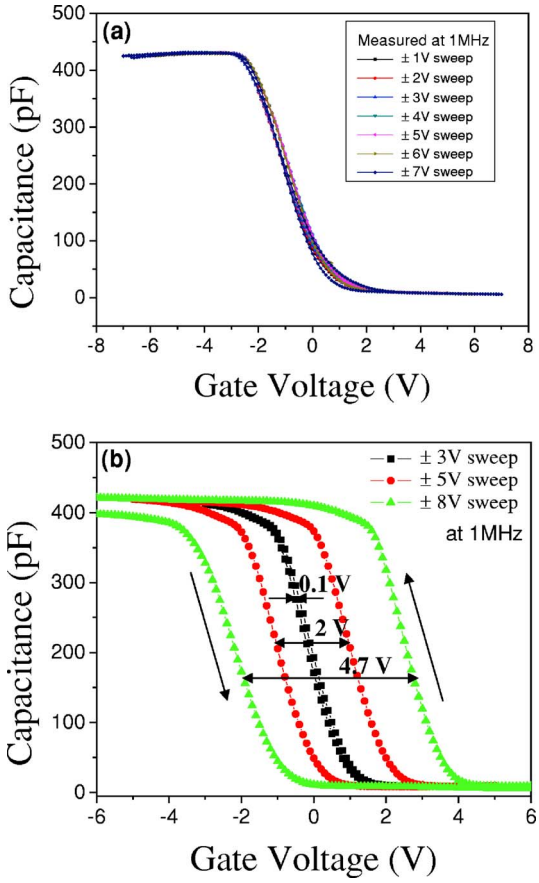

FIG. 3. (Color online) Typical capacitance-voltage curves of MOS structures (a) without Au NP and (b) with 8 nm diameter Au NP, as a function of various voltage sweep ranges. No shift of the C-V curve is observed in (a) However, shift of C-V curves toward positive and negative voltages are observed with increasing the voltage sweep range in (b) indicating hole charging and electron charging, respectively.

A clearly exhibits a conventional MOS structure *C-V* trend without charge trap sites. There have been several studies indicating that memory or charging effects are induced by voltage stresses in MOS structures.[9,10] Two types of traps that are responsible for charging effects are generally bulk traps in the insulator and interface states at the substrate/insulator film. The type of traps responsible for the charge state can be directly distinguished by the reversible changes in the *C-V* curve. As shown in Fig. 3(a), device A does not show any shift in the *C-V* curves with increasing the voltage sweep (positive voltage to negative voltage and back to positive voltage) width from 1 to 7 V. If charge traps in the HfO_2 layer itself are due to bulk traps, the width of the *C-V* hysteresis would be proportional to the voltage sweep width because the flatband voltage shift (ΔV_{FB}) is strongly dependent on applied voltage stress.[11,12] However, the *C-V* curve of device A is independent of voltage sweep width, as shown in Fig. 3(a). Therefore, the *C-V* curve of device A is believed to have no trap sites in the gate oxide layer or little interface states at substrate/HfO_2 and HfO_2/Au NPs. The MOS structure with Au NP (device B) showed the expected *C-V* behavior due to the existence of three-dimensionally confined Au NP. A large hysteresis in the *C-V* curve with an 8 to −8 V voltage sweep is shown in Fig. 3(b), indicative of charging effects due to the existence of trap sites in the Au NP. Because ΔV_{FB} increased up to 4.7 V with increasing applied sweep voltage, these charging behaviors indicate the existence of trap sites in the gate oxide layer by Au NP, as mentioned above. The hysteresis loop direction was counterclockwise, indicating that the carrier transfer between the Au NP and the *p*-type Si substrate occurs by a tunneling process.[13] The carrier trap density was estimated by using a simple formula: $N=(C_{HfO_2}/q)\Delta V_{FB}$, where C_{HfO_2} and q have values of 400 fF and 1.6×10^{-19} C, respectively, and ΔV_{FB} is as noted above.[14] The estimated trap density was about $8\times10^{12}/cm^2$ [gate electrode area was $\pi\times(150\ \mu m)^2$]. The comparison of the Au NP density ($1\times10^{12}/cm^2$) obtained by TEM images implies that each Au NP can store about eight electrons or equivalent positive charges. The ΔV_{FB} positive to negative sweep is greater than ΔV_{FB} negative to positive sweep, suggesting that electron injection is more involved than holes due to the asymmetrical electron and the hole barrier height of the HfO_2 film.[15]

To further analyze the memory characteristics of our devices, the charge retention time at room temperature was measured for device B through the application of ±5 V gate voltage stresses for 10 s. The capacitance after electron (write) or hole (erase) injection as a function of time is shown in Fig. 4. The logarithmic dependence of the retention characteristics on time has been observed previously by various groups.[11,15] The evolution for device B shows a programming window completely stable with time during the first 1 h. If we define the retention time as the time required for a 10% loss of the stored electrons, the retention time of our device is found to exceed 10^5 h. This was attributed to the higher electron barrier height via high work function (5.2 eV) of the Au NP, as predicted by the metal's properties. These results indicate a sufficient possibility for metal NP nonvolatile memory.

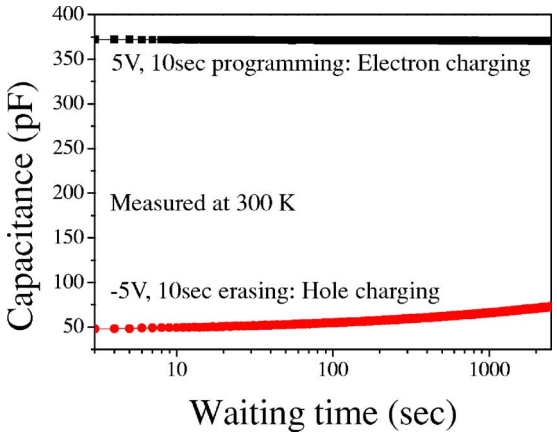

FIG. 4. (Color online) Retention characteristics of MOS device with Au NP. Data retention time is obtained by electron charging (5 V, 10 s) or hole charging (−5 V, 10 s) once and monitoring the capacitance at zero gate bias and room temperature.

In conclusion, we emphasized experimental results of a unique laser irradiation technique suitable for the formation of single crystal Au NP with three-dimensional structures and the development of NP-based nonvolatile memory. One of the key advantages of our method is that our process does not require any pre—or postprocessing high temperature annealing to efficiently fabricate NP, which is very appealing in its performance characteristics and compatible with semiconductor processing, resulting in a significant reduction of manufacturing costs. Finally, the use of Au metal NP in floating gate memory devices with a high-*k* HfO_2 provided an excellent long-term retention with the required functional characteristics of NP, rendering it feasible for the near-future development of unique NP-based floating gate memory.

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