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Postannealing effect on pseudobilayer $HfO_2/HfSi_xO_y/Si$ gate oxides formed by an inductively coupled sputtering process

Won Joon Choi, Eun Joung Lee, Jong Hyun Lee, Jung Yup Yang, Young Ho Do, and Jin Pyo Hong[a)]
New Functional Material and Device Laboratory, Department of Physics, Hanyang University, Seoul 133-791, Korea

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Pseudobilayer $HfO_2/HfSi_xO_y$ gate dielectrics in metal-oxide-semiconductor devices were prepared using an inductively coupled rf plasma sputtering technique. This sputtering method was designed to improve the uniformity and efficiency of formation of high-quality gate dielectrics at room temperature. Crystallization of the gate dielectrics was easily controlled from amorphous to monoclinic by varying the external power from 0 to 60 W at RT. The chemical bond states of the interfacial layers in the as-deposited and postannealed samples were analyzed with an x-ray photoelectron spectroscopy (XPS) system. The XPS results revealed that the interfacial layers of the as-deposited and annealed samples were hafnium silicide and hafnium silicate, respectively. Compared with the as-deposited sample, the pseudobilayer $HfO_2/HfSi_xO_y$ gate dielectric annealed at 750 °C yielded excellent electrical characteristics due to the hafnium silicate interfacial layer. The dielectric constant and leakage current of the postannealed samples were about 15 at 100 kHz and less than $\sim 10^{-6}$ A/cm^2 at −1.5 V, respectively. © *2006 American Vacuum Society.*
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I. INTRODUCTION

Scaling down bulk Si metal-oxide-semiconductor (MOS) devices requires commensurate increases in the gate dielectric capacitance. The equivalent oxide thickness will need to be as thin as 0.8 nm for complementary metal-oxide-semiconductor technology at the 50 nm node in the year 2011.[1] With conventional SiO_2-based dielectrics, the leakage current through gate dielectrics and reliability become serious problems. Therefore, an alternative material with a higher dielectric constant must eventually be developed to replace the current SiO_2 material. Recently, various materials with high dielectric constants, such as Ta_2O_5,[2] Al_2O_3,[3] $SrTiO_3$,[4] HfO_2,[5] and ZrO_2,[6] have been studied as SiO_2 replacements. Among them, bulk HfO_2 is regarded as one of the most promising candidates because of its large dielectric constant (~25), band gap of 5.68 eV, good conduction band offset, and thermal stability with a Si interface.[7] Another important aspect for obtaining a high-quality dielectric layer is the fabrication method. Several methods such as conventional sputtering, physical vapor deposition, atomic layer deposition, chemical vapor deposition, pulsed laser deposition, etc., have already been employed.[8] But HfO_2 gate dielectrics fabricated by a conventional sputtering process at room temperature (RT) show various crystalline structures depending on the process conditions. The crystallized phase of HfO_2 gate dielectrics is well known to induce a relative increase in leakage current density through grain boundaries.

In this work, we focus on the efficient formation of HfO_2 gate dielectrics using an inductively coupled rf plasma sputtering (ICPS) method at RT. This technique allows the useful capability of suppressing the crystallization of HfO_2 gate dielectrics by varying the external rf power through an external electrode during the conventional sputtering process. As-deposited and postannealed samples were compared to observe the annealing effect on the chemical bond states of the interfacial layer (IL) between the HfO_2 film and Si substrate. The capacitance and leakage current density versus voltage were measured to analyze the electrical properties of both samples. In addition, the transmission electron microscopy (TEM) measurement was done to determine the thickness of our HfO_2 gate dielectrics.

II. EXPERIMENTS

The HfO_2 gate dielectrics were prepared on *p*-type Si (100) substrates by utilizing an inductively coupled rf plasma sputtering method at RT. This sputtering system positions a ring-shaped electrode between the Hf target and the substrate as shown in Fig. 1. The ring-shaped electrode concentrates the plasma density around the target and substrate by the external application of rf power. Therefore, this technique can reduce the self-bias effect on gate dielectrics and increase the atomic oxygen concentration by using two rf power sources, compared with a conventional rf reactive sputtering method. The substrates were cleaned with trichloroethylene, acetone, and methanol and immersed in a dilute (1%) HF solution to remove the native oxide or contaminants from the substrate surfaces. This cleaning method produced a hydrogen-passivated surface on the substrates.[9] The chamber was pumped down to a base pressure of $\sim 1 \times 10^{-6}$ Torr, and the working pressure during deposition was maintained at 4×10^{-3} Torr. The internal deposition power of the sputtering system was fixed at 50 W, and the external power was varied from 0 to 60 W through an external electrode inserted

a)Author to whom correspondence should be addressed; electronic mail: jphong@hanyang.ac.kr

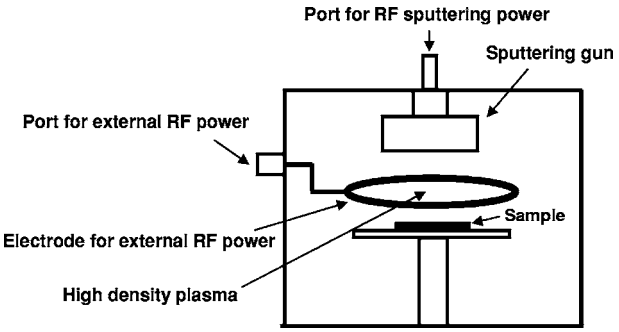

FIG. 1. Schematic diagram of unique inductively coupled rf sputtering system for the efficient formation of gate dielectrics at room temperature.

inside the conventional rf sputtering system. Also, the annealing process of the HfO_2 gate dielectrics was performed by a rapid thermal annealing (RTA) process at 750 °C for 2 min in ambient N_2. As a gate electrode, 100 nm thick aluminum was grown on the HfO_2 film through a metal shadow mask using dc magnetron sputtering. The junction size was $7\times10^{-4}cm^2$. The capacitance-voltage (C-V) at 100 kHz and leakage-current-density–voltage (J-V) measurements were performed to analyze the electrical characteristics of the pseudobilayer gate dielectrics of Al/HfO_2 (8.5 nm)/IL (4.5 nm)/Si. And each thickness of pseudobilayer gate was obtained by the TEM images, as shown in Fig. 2. In addition, the structural properties of HfO_2 (100 nm) gate dielectrics

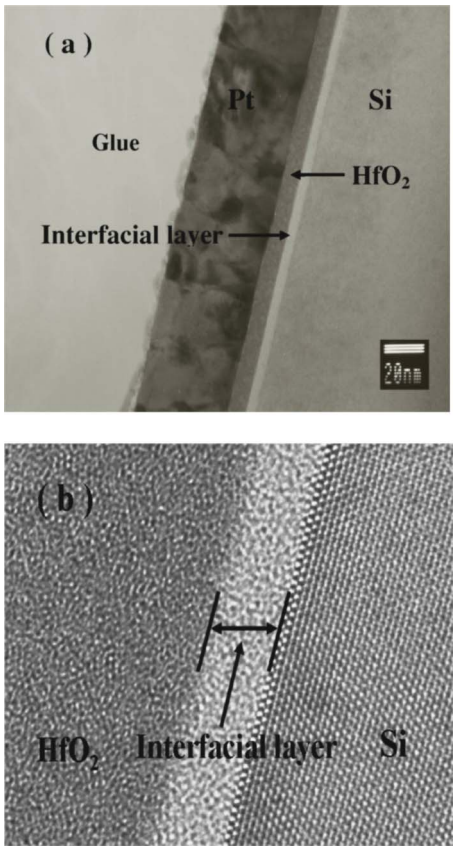

FIG. 2. Typical TEM image of as-deposited HfO_2/IL/Si gate dielectrics.

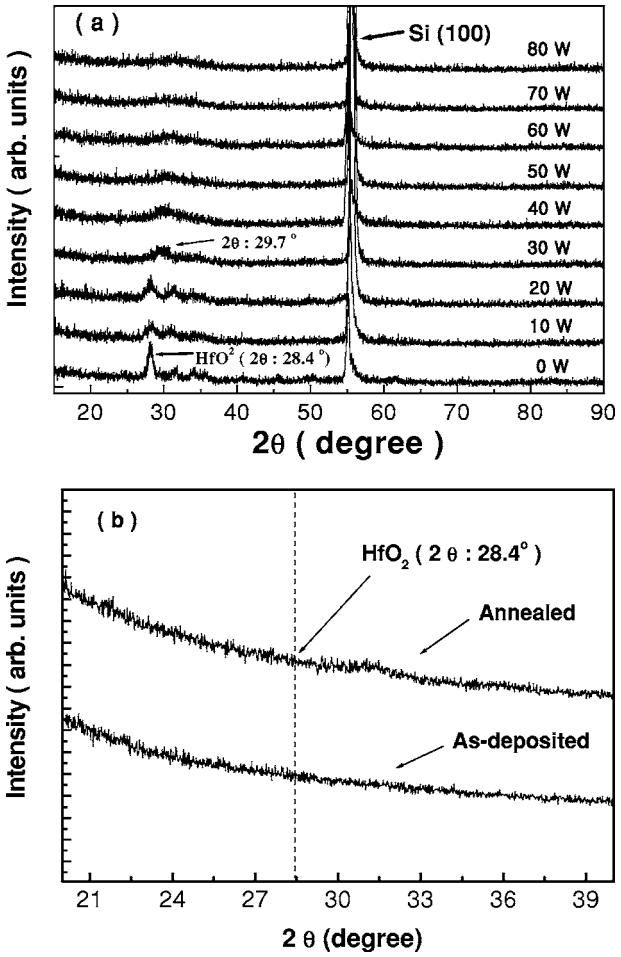

FIG. 3. (a) XRD results of the as-deposited HfO_2 (100 nm) gate dielectrics as a function of external power and (b) XRD patterns of as-deposited and postannealed samples (10 nm) at 750 °C.

were analyzed with x-ray diffraction (XRD) using a Cu $K\alpha$ source. Finally, x-ray photoelectron spectrometry (XPS) was performed to investigate the chemical bonding states of the interfacial layer between the HfO_2 and Si substrate. The depth profile properties of the HfO_2/IL/Si structure were investigated according topa etching time.

III. RESULTS AND DISCUSSION

Figure 3 shows the structure properties of thick (100 nm) and thin (10 nm) HfO_2 gate dielectrics. The crystallization of the thick gate dielectrics was investigated by varying the external power, and the thin ones were fabricated in order to investigate the thermal stability and structure properties for application in a MOS device. Figure 3(a) shows typical XRD patterns as a function of external power for 100 nm thick, as-deposited HfO_2 gate dielectrics. Samples fabricated by the conventional rf sputtering method[10,11] mainly exhibit a strong crystallized monoclinic phase, with the main peak at 2θ=28.4°.[12] However, the HfO_2 gate dielectrics fabricated by the ICPS technique exhibit various crystalline phases up to amorphous phase, depending on different external powers. The structural properties of the HfO_2 film varied from crys-

talline to amorphous phase with increasing external power, as shown in Fig. 3(a). A weak crystalline phase started to form at 50 W and then the amorphous phase was observed at 60 W, confirming that the HfO_2 and IL prepared by the ICPS technique have amorphous phases, as shown in Fig. 2(b). In our sputtering system, the distribution of oxygen plasma was strongly influenced by the external rf power, and applying this external rf power to the electrode was found to be the key parameter for the efficient formation of various structural phases at RT. Without an electrode inside the conventional rf sputtering system, mixed monoclinic, tetragonal and orthorhombic phases were observed.[13] Therefore, this method can fabricate a HfO_2 gate dielectric with a weak crystalline phase for MOS devices in a magnetron sputtering system because the crystalline phase of the HfO_2 gate dielectric is well known to induce a relative increase in the leakage current density through grain boundaries. Also, the thermal stability of the HfO_2 films was investigated in order to apply our HfO_2 film to MOS devices. The 10 nm thick HfO_2 gate dielectrics were directly deposited onto the Si substrate, and Fig. 3(b) shows the XRD patterns of the as-deposited and postannealed HfO_2 gate dielectrics. As shown in Fig. 3(b), although the HfO_2 gate dielectrics were annealed at 750 °C for 2 min in ambient N_2, both the as-deposited and postannealed HfO_2 gate dielectrics exhibit very weak crystalline phases, indicating enhanced thermal stability property by keeping weak crystalline phases. Also, the HfO_2 gate dielectrics directly deposited on Si substrates essentially create a strong interfacial layer between the HfO_2 and Si substrate. This may be due to strong Hf–Si bonding and Si diffusion during sputtering. The thickness of the interfacial layer is about 4.5 nm, as shown in Fig. 2(a). Therefore, the MOS device was composed with a pseudobilayer gate dielectric of HfO_2 (8.5 nm)/IL (4.5 nm)/Si.

Figure 4 reveals the Hf 4*f* core level spectra of the as-deposited and postannealed pseudobilayer gate dielectrics of HfO_2 (8.5 nm)/IL (4.5 nm)/Si. Figure 4(a) shows the XPS results of the as-deposited sample as a function of etching time. In this case, the Hf $4f_{7/2}$ (16.9 eV) and Hf $4f_{5/2}$ (18.3 eV) core level spectra of the HfO_2 gate dielectrics were observed up to an etching time of 200 s. As can be seen in this figure, the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks with binding energies of 16.9 and 18.3 eV, respectively, are related to Hf–O bonding in the HfO_2 itself. The curve fitting indicates that the fourth 4*f* doublet in the spin-orbit splitting and area ratio values are 1.4 eV and 0.73–0.76, respectively.[14,15] However, the XPS results of etching time from 1400 to 1800 s display the peak at a low binding energy. The existence of an XPS spectra peak at a low binding energy corresponds to the formation of Hf–Si at interfaces between the HfO_2 film and Si substrate, confirming the formation of silicide (~15 eV). After the postannealing process, the XPS spectrum of the pseudobilayer gate dielectrics showed a shift of whole peaks, corresponding to the silicate formation, as shown in Fig. 4(b). The peak shift to a higher binding energy may be related to the formation of (Hf–O–Si) silicate at the interfacial layer in the vicinity of the Si substrate. But there

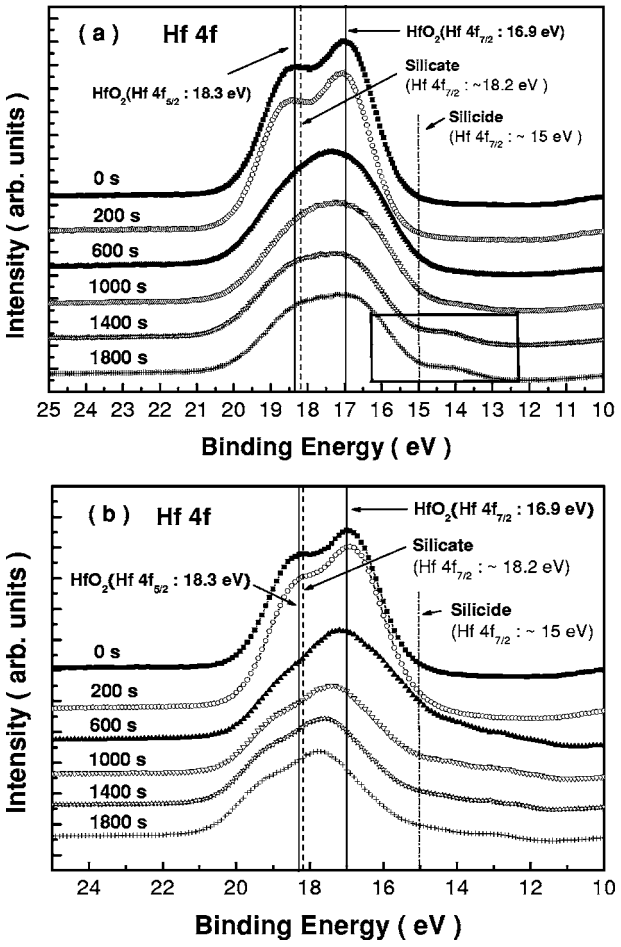

FIG. 4. XPS spectra of the pseudobilayer gate dielectrics with HfO_2/IL/Si formed at an external power of 60 W. The Hf 4*f* core level spectra of (a) as-deposited and (b) postannealed samples shown as a function of sputtering time.

is a possibility of the peak shift and broadness due to etching damage or sample charging effect during the XPS measurements. Therefore, in order to remove any possible effects of charging or etching damage, all of the data were calibrated with the peaks of C 1*s* and Si 2*p* (not shown in this article) after the XPS measurements. In addition, if the shift and broadness behaviors in the XPS measurements come from the sputtering damages or charging profile, both as-deposited and annealed MOS devices in *C-V* measurement would have the same electrical property. However, it is well known that the dielectric constant of silicide film is smaller than that of silicate film and our electrical measurement exhibits different *C-V* properties, depending on the formation of silicide and silicate layers. Therefore, it is expected that the formation of silicate interfacial layer induces a higher dielectric constant and a lower leakage current density than the interfacial layer of the as-deposited sample after annealing process.

Figure 5(a) shows the *C-V* curves of as-deposited and postannealed pseudobilayer gate dielectrics with HfO_2 (8.5 nm)/IL (4.5 nm)/Si. As can be seen in the figure, the as-deposited sample exhibited a dielectric constant and accumulation capacitance value lower than those of the postan-

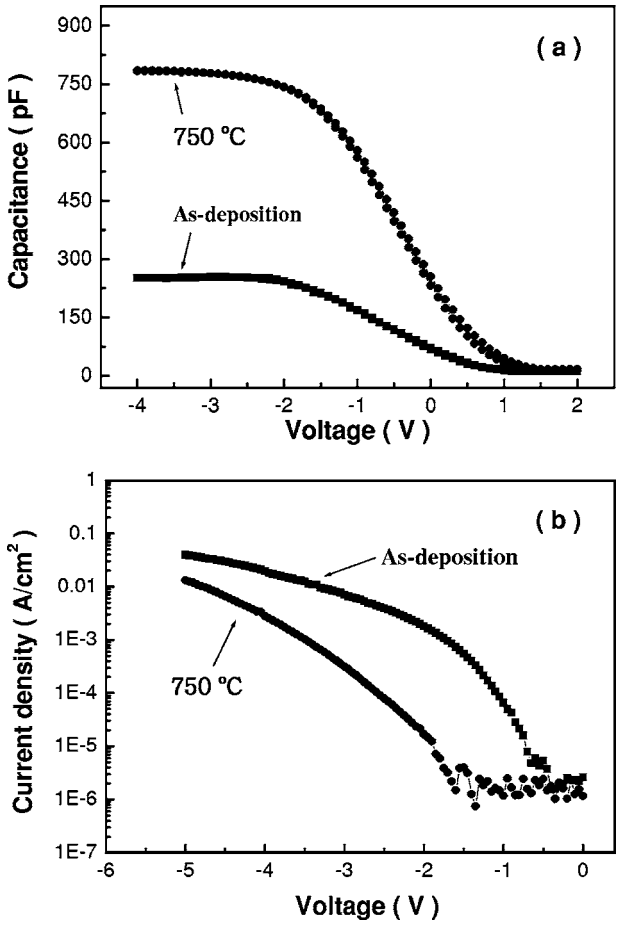

FIG. 5. (a) *C-V* curves at 100 kHz and (b) *J-V* curves of as-deposited and postannealed samples with the HfO_2 (8.5 nm)/IL (4.5 nm)/Si structure.

nealed gate dielectrics. The dielectric constant and accumulation capacitance of the postannealed gate dielectrics were ~15 and 784.9 pF, respectively. In the postannealed sample, the hysteresis of the *C-V* curve was found to be 120 mV at a flatband voltage of 0.84 V. The existence of hysteresis suggests charge trapping and mobile charge shifting in the oxide layer.[16] Figure 5(b) shows the *J-V* curves of the pseudobilayer gate dielectrics after annealing. The postannealed pseudobilayer gate dielectrics showed a leakage current density of $\sim 10^{-6}$ A/cm^2 less than that of the as-deposited sample with $\sim 10^{-4}$ A/cm^2 at −1.5 V. The significant increase in capacitance and reduction of leakage current density in the annealed sample are due to the dominant formation of Hf–O–Si bonds rather than Hf–Si bonds, as shown in Fig. 3(b). Therefore, the annealing process is able to improve the electrical properties of gate dielectrics by changing the chemistry of the interfacial layer from silicide to silicate.

IV. CONCLUSIONS

An inductively coupled sputtering technique for gate dielectrics reveals that the formation of crystalline phases over amorphous phases can be easily controlled by varying the external power during sputtering. An amorphous HfO_2 film was obtained at an optimized power of 60 W in this case. In the MOS structure, the silicide interfacial layer between the HfO_2 and Si substrate was transformed into a silicate by the postannealing process at 750 °C, enhancing the leakage current density of the pseudobilayer gate dielectrics by one order of magnitude.

ACKNOWLEDGMENTS

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