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## Topical Review

# Atomic layer deposition for nanoscale oxide semiconductor thin film transistors: review and outlook

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**Abstract**

Since the first report of amorphous In–Ga–Zn–O based thin film transistors, interest in oxide semiconductors has grown. They offer high mobility, low off-current, low process temperature, and wide flexibility for compositions and processes. Unfortunately, depositing oxide semiconductors using conventional processes like physical vapor deposition leads to problematic issues, especially for high-resolution displays and highly integrated memory devices. Conventional approaches have limited process flexibility and poor conformality on structured surfaces. Atomic layer deposition (ALD) is an advanced technique which can provide conformal, thickness-controlled, and high-quality thin film deposition. Accordingly, studies on ALD based oxide semiconductors have dramatically increased recently. Even so, the relationships between the film properties of ALD-oxide semiconductors and the main variables associated with deposition are still poorly understood, as are many issues related to applications. In this review, to introduce ALD-oxide semiconductors, we provide: (a) a brief summary of the history and importance of ALD-based oxide semiconductors in industry, (b) a discussion of the benefits of ALD for oxide semiconductor deposition (*in-situ* composition control in vertical distribution/vertical structure engineering/chemical reaction and film properties/insulator and interface engineering), and (c) an explanation of the challenging issues of scaling oxide semiconductors and ALD for industrial applications. This review provides valuable perspectives for researchers who have interest in semiconductor materials and electronic device applications, and the reasons ALD is important to applications of oxide semiconductors.

Keywords: atomic layer deposition (ALD), oxide semiconductor, thin film transistor (TFT)

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## 1. Introduction

### *1.1. Recent progress in oxide semiconductors for thin-film transistors*

The first demonstration of an amorphous oxide semiconductor (AOS) in 1996 shocked conventional views of semiconducting materials because they exhibited superior electrical performance, in spite of their amorphous structure. In early reports on semiconductors such as crystalline silicon-based, organic, oxide semiconductors and amorphous hydrogenated silicon (a-Si:H), the amorphous structure was considered an obstacle to high mobility, but it did promise better uniformity and lower process temperature for mass production [1]. In a-Si:H channel thin film transistor (TFT), the highly localized band structure and following limited mobility edge led to a low mobility of just $\sim$1 cm$^2$ V$^{-1}$ s$^{-1}$ [2].

However, it was proposed that AOS could have different orbital structures and electron pathways. It was suggested that metal cations with electronic configurations of $(n-1)\mathrm{d}^{10}\mathrm{ns}^0$ ($n \geqslant 4$) could have a small electron effective mass because the electron path, i.e., the conduction band minimum (CBM), is composed of widely spread and overlapping isotropic $n\mathrm{s}^0$ orbitals. As a result, they could exhibit high mobility despite the amorphous phase. Based on this theoretical background, in 2004, amorphous In–Ga–Zn–O (a-IGZO) was reported by Nomura *et al* [3]; its orbital structure and bandgap formation are described in figures 1(a) and (b). The percolation transport model, which is described in figure 1(c), was suggested by Nomura *et al* to be the reason for the high Hall mobility, which exceeded 10 cm$^2$ V$^{-1}$ s$^{-1}$, and the 6–9 cm$^2$ V$^{-1}$ s$^{-1}$ saturation mobility of the a-IGZO channel TFT [4]. After this, reports on AOS in both industry and academia dramatically increased. The AOS were reported to have superior electrical characteristics and processing conditions, including high TFT mobility, low off-current, adequate operating voltage, low process temperature, high uniformity, and wide flexibility of chemical compositions and deposition methods [5].

As noted, AOS was a promising semiconducting material. However, its mobility was far lower ($\sim$10 cm$^2$ V$^{-1}$ s$^{-1}$) than low-temperature polycrystalline silicon (LTPS, $>$80 cm$^2$ V$^{-1}$ s$^{-1}$). Also, inferior bias stabilities induced by oxygen-related defect sites still needed to be improved for industrial applications. Various approaches have been explored to overcome such issues in mass production. However, recent research has reported there is a trade-off relation between mobility and stability in AOS-TFT fabricated by conventional processes [6]. AOS-TFTs with high mobility have critical stability issues. Oxygen is considered to be key to mobility and stability, because of its role as both the source of free carriers and defect sites ($V_\mathrm{o}$). Cation and oxygen ratio control have been studied to overcome this issue. Cation dopants such as Sn, which have large cation orbitals, have been introduced, and are expected to provide high electron mobility [7]. To achieve high stability, dopants such as Zr (Zr–In–Zn–O) [8], Hf (Hf–In–Zn–O) [9], and Si (Si–In–Zn–O) [10] have been suggested. Small amounts of W doping have also been introduced to suppress $V_\mathrm{o}$ and achieve high stability using the high tungsten-oxide bond-dissociation energy in the $In_2O_3$ matrix (In–W–O) [11, 12]. Fabrication of crystalline oxide semiconductors was also explored to enhance electrical performance. In 2012, *c*-axis aligned crystalline IGZO (CAAC-IGZO) reported by the Semiconductor Energy Laboratory (SEL) exhibited high mobility (50 cm$^2$ V$^{-1}$ s$^{-1}$), extremely low off-current ($\sim 10^{-24}$ A $\mu$m$^{-1}$) and enhanced bias stability, but it was necessary to increase the process temperature up to 800 °C [13]. A double active layer [14], back-channel treatment [15], and front-channel modulation [16] of TFTs were studied to optimize device properties. In addition to these studies, TFT structure optimization [17], interface engineering [18], post-treatment [19], and anion doping [20] were also investigated to improve the mobility and stability of oxide semiconductors.

### *1.2. History of oxide semiconductor TFTs in display and memory industries*

Since the first report of a-IGZO based TFTs, industry interest in oxide semiconductor channel-based TFTs has dramatically increased. Figure 1(d) is an illustration of the development of oxide semiconductors in the display and memory industries. After the announcement of a-IGZO, the display industry shifted their interest from a-Si:H to AOS. The first commercialization of an AOS TFT was reported in 2012 in a liquid crystal display panel by Sharp Corporation. This is quite a rapid adoption considering the short history of the material itself. It was possible because the demand for flexible and transparent displays on thermally vulnerable substrates at large scale could be accomplished with the a-IGZO, at lower temperature (under 300 °C) with high uniformity[3]. Also, fully transparent circuits could be achieved in AOS-TFTs if the oxide compartments were selected properly, and this drove the adoption of AOS-TFT circuits for display applications. Low-temperature poly-silicon (LTPS) was limited by issues with its large-scale uniformity, high off-current, and high cost, and this resulted in broad research and various commercialized AOS-TFTs for displays, including large organic light emitting diode (OLED) TVs [21–24]. Currently, low-temperature polycrystalline oxide based backplanes are used [25]. These employ LTPS as the driving transistor for high on-current, and AOS as the switching transistor with low off-current.

At the same time, research in the memory field has concentrated on scaling down, to reduce unit area and enable three-dimensional (3D) integration, rather than investigating another semiconductor material [26]. To achieve high-density unit cells, the memory industry has expanded device structures from planar to 3D-structures such as vertical- [27], fin- [28], gate-all-around (GAA) [29], and channel-all-around (CAA) [30] devices. However, the scaling down approach now faces hurdles because of the steady increase in off-current in the unit transistors at reduced scale.

The first adoption of oxide semiconductors in a memory device was reported by Atsumi *et al* and involved dynamic oxide semiconductor random access memory (DOSRAM) [31]. The extremely low off-current of the oxide

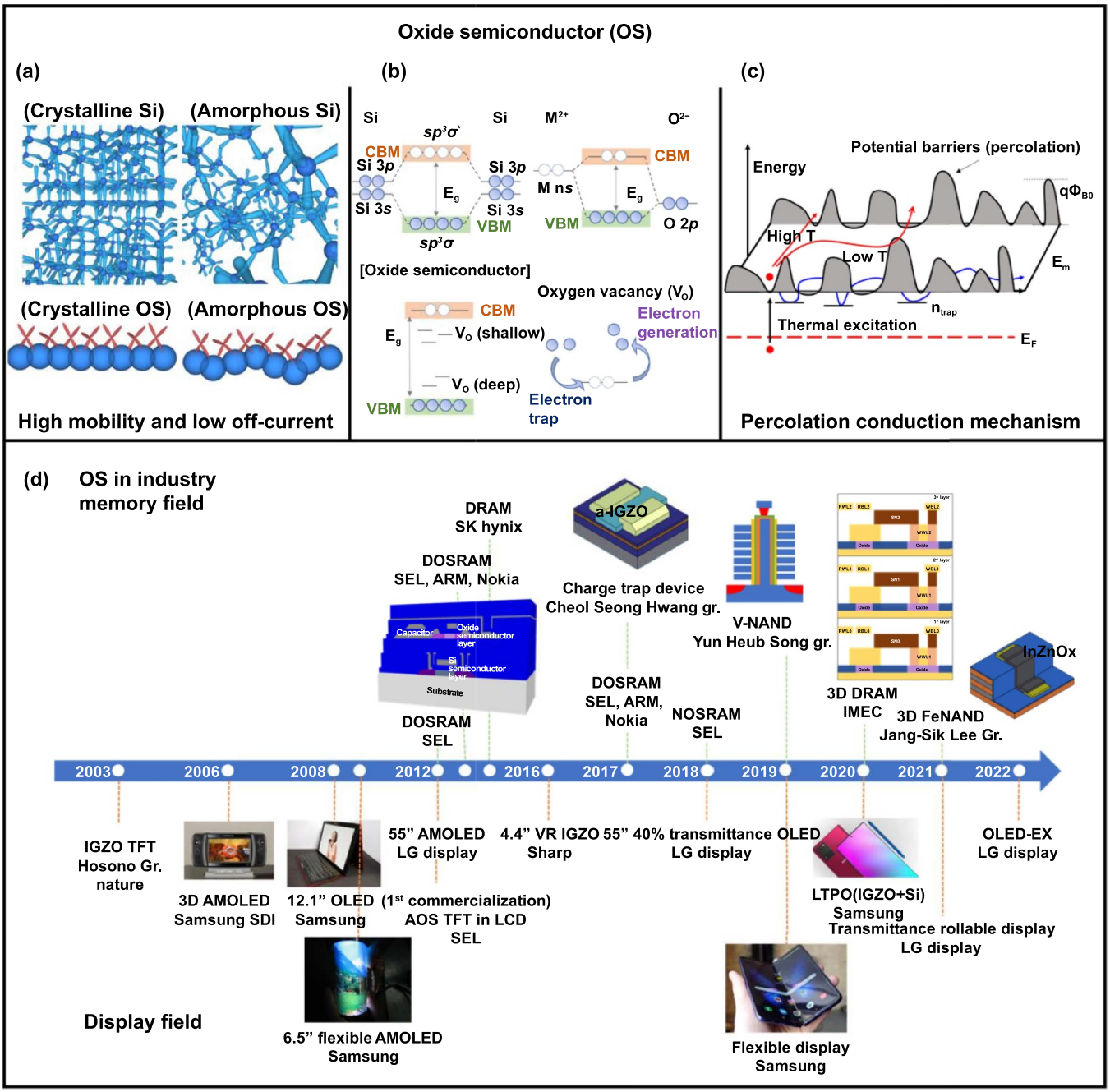


**Figure 1.** Overview of the oxide semiconductor concept and its history in industry. (a) Orbital structure of crystalline (c-Si) and amorphous Si (a-Si) oxide semiconductors. (b) Differences in the formation mechanism of bandgaps in a-Si, c-Si, and a-IGZO. (c) Schematic illustration of percolation conduction mechanism and the proportional relationships of carrier density and mobility. (d) Developments related to oxide semiconductors in the display and memory industry after the report of a-IGZO. Images of devices are permitted from Samsung display.

semiconductors made them candidates to replace silicon semiconductors in memory, and studies on this topic increased. Various research on DOSRAM [32, 33], and other devices such as charge trap devices [34], vertical-NAND (V-NAND) [35], monolithic 3D DRAM [36], vertical Fe-NAND [37], and CAA field effect transistors (FETs) [30] have been reported to date, as shown in figure 1(d). However, insufficient on-current, the low device stability of the AOS-TFT, and sputtering-based processes are huge barriers to further expansion in display and memory fields, and still need to be overcome.

## 2. Value of ALD as a fabrication process for oxide semiconductor channel TFTs

To fabricate the latest electronic devices a next-generation processing technique is required to overcome the disadvantages of conventional processes. Atomic layer deposition (ALD) is a highly developed, Å-scale controlled thin film deposition technique, and has progressed from chemical vapor deposition (CVD). In ALD, self-limiting behaviors and complementary reactions occur during the deposition process [38, 39]. In the

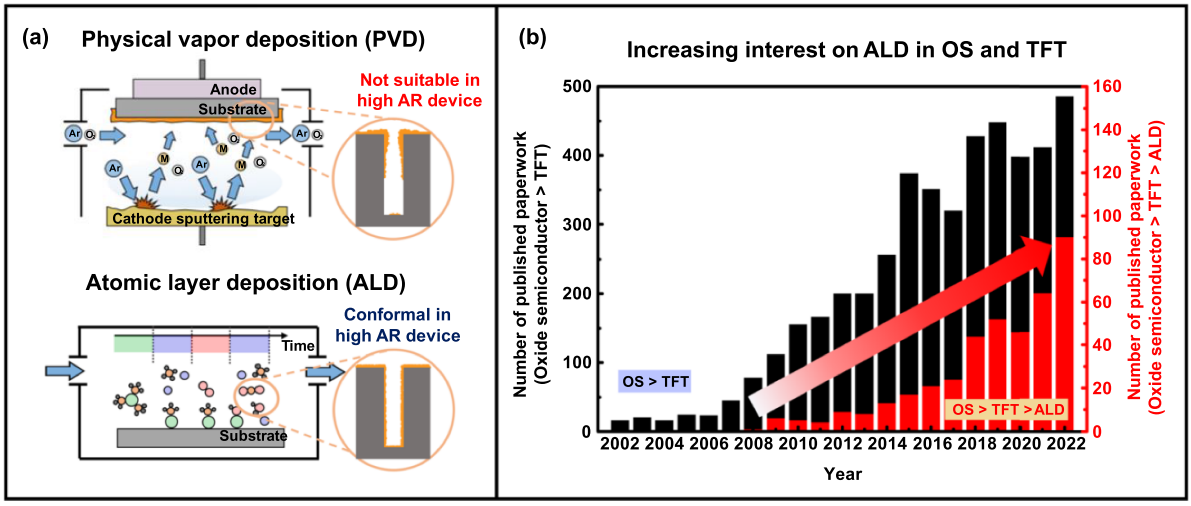


**Figure 2.** The merits of ALD, and growing interest. (a) Schematic illustration of PVD and ALD, and the deposition characteristics on a structured surface. (b) The graph shows the number of published works from scopus.com in September 2022 which includes the keyword on ALD/oxide semiconductor/TFT in the article title, abstract, and keywords.

self-limiting behavior, the chemical reaction of precursors and reactants on surfaces self-saturate when the initial reactive site is fully occupied, regardless of dosing amount. Complementary reactions are responsible for ALD chemical reactions, involving at least two different molecules separately exposed to the surface, for thin film deposition. These two mechanisms lead to conformal and high-quality thin film deposition at low temperature (<350 °C). With ALD, high uniformity can be achieved with the chemical reaction mechanism, even on high aspect ratio (AR) structured surfaces. This is still a problematic issue with conventional physical vapor deposition (PVD) processes [39]. Figure 2(a) exhibits a schematic illustration of a sputtering system used for ALD and the difference in film deposition morphology with high AR devices. Because of these merits, ALD is already used for dielectric layer deposition in commercial dynamic random access memory (DRAM) and NAND flash memory [40] and for OLED displays as an encapsulation layer deposition process [41].

For oxide semiconductors, conventional sputtering systems clearly have many advantages in terms of mass production. High throughput and scalability have led to mature a-IGZO sputtering processes. However, several issues have emerged. These include non-uniformity on large-area substrates [85], limited process parameters to optimize, difficulty in modulating composition, and trade-offs in mobility-reliability, which are critical issues in devices but are hard to control using a single target and the limited process conditions of a sputtering system [6]. On the other hand, ALD avoids these issues. The unique nature of ALD enables both high uniformity and facile control in composition and stacking processes. Also, interest in a fabrication process for each layer has increased recently, with the requirements of continuously scaled-down devices. Figure 2(b) shows publication trends, which reflect increasing interest in ALD, in oxide semiconductors and in TFTs. The combined study of oxide semiconductors, thin film transistors, and ALD together only emerged about 10 years ago. This trend coincides with the increasing need for oxide semiconductors, especially for display and memory industries, as shown in figure 1(d).

Table 1 is a summary of representative reports of ALD-deposited n-type oxide semiconductor channel TFTs in the last 3 years (2020–2022). With the growing interest in ALD, studies on materials using ALD have also rapidly increased, as shown in the table, which will be discussed in this review. In particular, superior electrical performances have been recently reported, including a remarkable mobility of over 100 $cm^2\ V^{-1}\ s^{-1}$ [43, 46], an exceptionally low subthreshold swing under 100 mV/decade [64, 66, 80, 83], and highly improved stability using a stack structure [14]. However, the main benefits of employing ALD for oxide semiconductor channel TFTs have not been clearly suggested. So, what are the main differences between ALD-deposited oxide semiconductors compared to conventionally deposited ones, and how can we achieve desired performance with ALD processes?

This section will introduce several recent studies that provide an explanation for why ALD-oxide semiconductor TFTs have become industrially important. We suggest ALD provides four benefits in oxide semiconductor TFT fabrication. Each subsection includes suitable examples of ALD oxide semiconductor films or TFTs from research.

### 2.1. *In-situ* composition control

The first benefit of ALD is the controllability of composition during an *in-situ* process. Multiple components, which can readily make ternary- and quaternary- amorphous phases, are favored over binary oxide semiconductors, because crystallinity and grain size degrade electrical performance. In multi-component oxide semiconductors, the elemental distribution and composition significantly influence the electrical characteristics, especially when used for TFT channel layers. Unlike conventional processes, the cycle-dependent composition and thickness controllability of ALD allows wide control over cation distribution in the bulk-, front- and back-channel

**Table 1.** Representative studies in three recent years (2020–2022) of ALD-based n-type oxide semiconductor channel TFT fabrication and evaluation. Channel materials are classified as binary, ternary, quaternary, and stacked structure. The precursor, reactant, process condition and TFT parameters of each report are listed.

| Channel information | Material | Precursor[a] | Reactant | $T_{dep}$[b] (°C) | TFT mobility (max) ($cm^2\ V^{-1}\ s^{-1}$) | $V_{TH}$ | S.S (V/dec) | Year | References |
|---|---|---|---|---|---|---|---|---|---|
| Binary | $In_2O_3$ | $In(CH_3)_3[CH_3OCH_2CH_2NHtBu]$ | $H_2O$ | 150 | 6.1 | 0.85 | 0.36 | 2020 | [42] |
| | | TMIn | $H_2O$ | 225 | 113 | $<-1$ | 0.150 | 2021 | [43] |
| | | TMIn | $H_2O$ | 225 | >20 | $<-3$ | N/S | 2021 | [44] |
| | | TMIn | $H_2O$ | 225 | N/S | $<-2$ | 0.10–0.12 | 2022 | [45] |
| | | TMIn | $H_2O$ | 225 | >100 | N/S | N/S | 2022 | [46] |
| | | DADI | $Ar/O_2$ plasma | 250 | 12.6 | −9.6 | 0.83 | 2022 | [47] |
| | | DMION | $Ar/O_2$ plasma | 300 | 32.4 | −5.5 | 0.49 | 2022 | [48] |
| | | $(C_2H_5)_2InCH_3$ | $O_2$ plasma | 250 | 17 | 0.06 | 0.069 | 2022 | [49] |
| | ZnO | DEZ | $H_2O$ | 100–200 | 11.8 | 1.1 | 0.175 | 2020 | [50] |
| | | DEZ | $NaOH/H_2O$ | 150 | 1.7 | — | N/S | 2021 | [51] |
| | | DEZ | $O_2$ plasma | 250 | 28.7 | — | 0.101 | 2021 | [52] |
| | | DEZ | $H_2O/O_3$ | 150 | 31.1 | 0.14 | 0.21 | 2021 | [53] |
| | | DEZ | $H_2O/O_2$ | 100 | 32.1 | 1 | 0.27 | 2022 | [54] |
| | | N/S | N/S | N/S | 17.9 | 3.23 | 0.225 | 2022 | [55] |
| | | DEZ | $H_2O$ plasma | 70 | 1.10 | 2.29 | 0.205 | 2022 | [56] |
| | | DEZ | $H_2O_2$ | 150 | 10.7 | 1.41 | 0.25 | 2022 | [57] |
| | | N/S | N/S | 200 | 39.2 | 0.36 | 0.37 | 2022 | [58] |
| Ternary | InGaO | DADI TMGa | $O_3$ | 250 | 40.3 | −0.6 | 0.41 | 2020 | [59] |
| | | TMION TMGON | $Ar/O_2$ plasma | 200 | 36.7 | −5.5 | 0.30 | 2021 | [60] |
| | | DATI TMGa | $Ar/O_2$ plasma | 150 | 71.27 | −0.3 | 0.074 | 2022 | [61] |
| | | DADI TMGa | $O_3$ | 250 | 50.1 | −0.5 | 0.25 | 2022 | [62] |
| | InZnO | DADI DEZ | $O_3$ | 200 | 40.95 | 0.21 | 0.34 | 2022 | [63] |
| | | DADI DEZ | $O_3$ | 250 | 48.1 | 0.07 | 0.20 | 2022 | [62] |
| | InAlO | DMAI TMA | $O_2$ plasma | N/S | 18.9 | −0.4 | 0.09 | 2021 | [64] |
| | | DMAI TMA | $Ar/O_2$ plasma | 200 | 6.07 | 2.16 | 1.50 | 2022 | [65] |
| | InSnO | TMIn | $H_2O$ | 225 | 28 | N/S | 0.08 | 2022 | [66] |

(Continued.)

**Table 1.** (Continued.)

| Channel information | Material | Precursor[a] | Reactant | $T_{dep}$[b] (°C) | TFT mobility (max) ($cm^2\ V^{-1}\ s^{-1}$) | $V_{TH}$ | S.S (V/dec) | Year | References |
|---|---|---|---|---|---|---|---|---|---|
| | | TDMASn | | | | | | | |
| | ZnGaO | DEZ | $H_2O$ | 150 | 16.2 | N/S | 0.22 | 2020 | [67] |
| | | $Ga_2(NMe_2)_6$ | | | | | | | |
| | ZnSnO | DEZ | Thermal $H_2O$ | 200 | 13.8 | N/S | 0.43 | 2020 | [68] |
| | | TDMASn | and $O_2$ plasma | | | | | | |
| | | DEZ | $O_3$ | 250 | 13.6 | −0.1 | 0.33 | 2020 | [69] |
| | | TDMASn | | | | | | | |
| | | N/S | Thermal $H_2O$ | 150 | 12.4 | 3.73 | 0.223 | 2022 | [70] |
| | | | and | | | | | | |
| | | | $O_2$ plasma | | | | | | |
| Quaternary | InGaZnO | DADI | $O_2$ plasma | 150 | 21.11 | 0.82 | 0.22 | 2020 | [71] |
| | | TMGa | | | | | | | |
| | | DEZ | | | | | | | |
| | | In–Ga | $O_3$ | 150 | 0.19 | N/S | 0.54 | 2021 | [72] |
| | | bimetallic single | | | | | | | |
| | | precursor | | | | | | | |
| | | DEZ | | | | | | | |
| | | TEIn | $O_3$ | 200 | 13.6 | N/S | 0.55 | 2021 | [73] |
| | | In–Ga | | | | | | | |
| | | bimetallic single | | | | | | | |
| | | precursor | | | | | | | |
| | | DEZ | | | | | | | |
| | | TEIn | $O_3$ | 150 | 27.6 | N/S | 0.28 | 2021 | [74] |
| | | In–Ga | | | | | | | |
| | | bimetallic single | | | | | | | |
| | | precursor | | | | | | | |
| | | DEZ | | | | | | | |
| | | DADI | $Ar/O_2$ plasma | 200 | 28.0 | −0.5 | 0.36 | 2021 | [75] |
| | | TMGa | | | | | | | |
| | | DEZ | | | | | | | |

(Continued.)

**Table 1.** (Continued.)

| Channel information | Material | Precursor[a] | Reactant | $T_{dep}$[b] (°C) | TFT mobility (max) ($cm^2\ V^{-1}\ s^{-1}$) | $V_{TH}$ | S.S (V/dec) | Year | References |
|---|---|---|---|---|---|---|---|---|---|
| | | DADI<br>TMGa<br>DEZ | $O_2$ plasma | 200 | 27.52 | 1.07 | 0.24 | 2021 | [76] |
| | | DADI<br>TMGa<br>DEZ | $O_3$ | 250 | 21.7 | 1.18 | 0.13 | 2021 | [77] |
| | | In–Ga bimetallic single precursor<br>DEZ | $O_3$ | 150 | 3.21 | N/S | 0.46 | 2021 | [78] |
| | | DADI<br>TMGa<br>DEZ | $Ar/O_2$ plasma | 200 | 23.26 | 0.13 | 0.20 | 2022 | [14] |
| | | TEIn<br>In–Ga bimetallic single precursor<br>DEZ | $O_3$ | 150 | 0.3 | 0.09 | 0.29 | 2022 | [79] |
| | | DADI<br>TMGa<br>DEZ | $O_2$ plasma | 250 | N/S | −3.5 | 0.23 | 2022 | [30] |
| | | DADI<br>TMGa<br>DEZ | $Ar/O_2$ plasma | 200 | 40.86 | 0.19 | 0.068 | 2022 | [80] |
| | InSnAlO | TMIn<br>TDMASn<br>TMA | $H_2O$ | 200 | 2.2 | 9.5 | 0.33 | 2021 | [81] |
| | | TMIn<br>TDMASn<br>TMA | $H_2O$ | 200 | 2.28 | 6.8 | 0.366 | 2022 | [82] |
| | InSnGaO | DADI<br>BDMADMSn<br>TMGa | $Ar/O_2$ plasma | 200 | 33.8 | −0.5 | 0.079 | 2022 | [83] |

(Continued.)

**Table 1.** (Continued.)

| Channel information | Material | Precursor[a] | Reactant | $T_{dep}$[b] (°C) | TFT mobility (max) ($cm^2\ V^{-1}\ s^{-1}$) | $V_{TH}$ | S.S (V/dec) | Year | References |
|---|---|---|---|---|---|---|---|---|---|
| Stacked | InZnO/GaZnO | DADI<br>TMGa<br>DEZ | $O_3$ | 250 | 76.7 | −0.37 | 0.13 | 2022 | [62] |
| | InGaO/GaZnO | DADI<br>TMGa<br>DEZ | $O_3$ | 250 | 68.1 | −0.73 | 0.19 | 2022 | |
| | InZnO/InGaZnO | DADI<br>TMGa<br>DEZ | Ar/$O_2$ plasma | 200 | 38.77 | −1.33 | 0.19 | 2022 | [14] |
| | InZnO/InGaZnO | TEIn<br>In–Ga bimetallic single precursor<br>DEZ | $O_3$ | 200 | 50.8 | N/S | N/S | 2022 | [84] |

[a] Precursor names represent the chemicals as follows: dimethylbutylamino(trimethyl indium) (DATI), trimethyl gallium (TMGa), diethyl zinc(DEZ), imethyl[N-(tert-butyl)-2-methoxy-2-methylpropan-1-amine] indium (DMION), triethyl indium (TEIn), trimethyl indium (TMIn), trimethyl aluminum (TMA), tetrakis (dimethylamido)tin (TDMASn), dimethylaluminum isopropoxide (DMAI), $In(CH_3)_3[CH_3OCH_2CH_2NHtBu]$ (TMION), $Ga(CH_3)_3[CH_3OCH_2CH_2NHt\text{-}Bu]$) (TMGON), tetrakiszirconium (TDMAZr).

[b] ALD process temperature of fabricated TFT channel layer in the references.

[c] N/S: No Report (No Data).

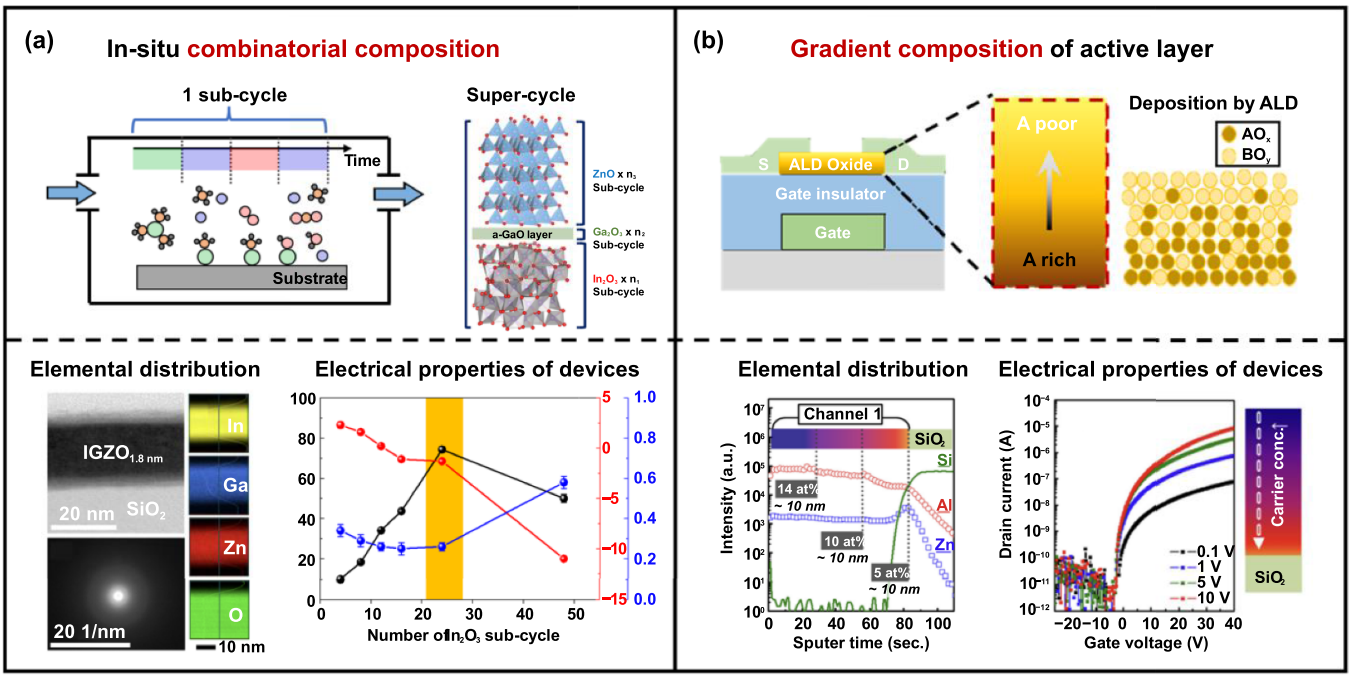


**Figure 3.** Description of ALD benefits 1: *in-situ* composition control in vertical distribution. (a) Schematic illustration of ALD super-cycle and electrical performance optimization of ALD-IGZO by screening $In_2O_3$ sub-cycles. Reprinted with permission from [86]. Copyright (2019) American Chemical Society. (b) Description of gradient composition in active layer and improvement in TFT performance by designing gradient distribution of Al from the front to the back-channel region. Reprinted from [87], with the permission of AIP Publishing.

regions. In sum, (a) composition control of multi-component oxide semiconductors and (b) vertical gradient distributions of cation composition can be achieved in ALD-fabricated oxide semiconductor channel TFTs, as will be described in detail in this section.

*2.1.1. Homogeneous composition control via ALD super-cycle in multi-component oxide semiconductors.* Figure 3(a) exhibits a scheme for ALD super-cycles and shows the differences in observed TFT performance based on super-cycle. An ALD super-cycle is a procedure for processing multiple components that need several different unit cycles (sub-cycles). ALD is basically used in repeated unit cycles, and deposition proceeds with precursor pulsing/inert gas purging/reactant pulsing/inert gas purging steps. The precursor and reactant dosing steps are separated by inert gas purging steps, which release physisorbed precursor, reactant, and by-products. To fabricate an A–B–$O_x$ thin film by ALD, a combination of one $AO_y$ sub-cycle and one $BO_z$ sub-cycle, i.e., an $(AO_x)$–$(BO_z)$ super-cycle, is selected. Likewise, if we need to fabricate an In–Ga–Zn–$O_x$ thin film by ALD, sub-cycles of $InO_y$, $GaO_z$ and $ZnO_w$ would be needed to make a super-cycle.

Most studies of ALD-oxide semiconductors exploit this super-cycle to control compositions. The ALD super-cycles shown in figure 3(a) are representative studies of ALD-oxide semiconductor TFTs by Sheng *et al* suggesting optimization of the indium ratio and vertical dimensional control by modulating the number of indium oxide sub-cycles [86]. ALD-IGZO was fabricated by super-cycles consisting of $n$ $In_2O_3$ sub-cycles, one $Ga_2O_3$ sub-cycle and one ZnO sub-cycle, where $n$ is 4–48. Depending on the number of indium sub-cycles, the indium ratio increased from 11.5 (4 $In_2O_3$ sub-cycles) to 22.9 at% (24 $In_2O_3$ sub-cycles). Unlike sputtered IGZO, sparse-density or porous regions were not observed, and a uniform/homogeneous IGZO thin film was confirmed by transmission electron microscopy (TEM) and energy dispersive X-Ray analysis (EDAX) analysis. When the indium ratio was low, the carrier concentration and Hall mobility exhibited a temperature dependence. However, these two factors become independent of temperature when the indium ratio increased. This indicates that the conduction mechanism of ALD-deposited IGZO for an optimized indium ratio is similar to that of single-crystal IGZO [88], and this was suggested as the reason for the good electrical characteristics of ALD-IGZO TFT, including high mobility up to 74 $cm^2\ V^{-1}\ s^{-1}$, a −1.3 V threshold voltage ($V_{TH}$), and a 0.26 V/decade subthreshold swing (SS). This study illustrated the importance of having a deep understanding of the ALD process, and the main variables needed to achieve high-performance TFTs. Cycle-dependent deposition characteristics, and the chemistry of the precursor/reactant/surface, seemed to be the origin of the unreported conduction mechanism in a-IGZO deposited by conventional deposition processes.

Many studies have also reported the super-cycle-based composition screening of ALD-oxide semiconductors. Sheng *et al* reported an optimized InZnSnO (IZTO) channel using the super-cycle method [89]. Based on the ALD-IZO process, Sn-doping was conducted for one or two $SnO_2$ sub-cycles to fabricate the IZTO channel. As the Sn ratio increased, the carrier concentration, Hall mobility, and defect levels all decreased. However, when the Sn ratio increased to 15.8 at% (2 $SnO_2$ sub-cycles), increased contact resistance and

interface trap densities were observed, leading to degradation of the field-effect-mobility. Consequently, the optimized TFT was achieved with a 1-1-1 $In_2O_3$–ZnO–$SnO_2$ super-cycle, which exhibited a high mobility of 27.8 $cm^2\ V^{-1}\ s^{-1}$ and superb reliability against bending tests ($\Delta V_{TH}$ −1.7 V after 240 000 rolling cycles). Baek *et al* reported that an ALD-IZTO channel TFT exhibited an optimized cation ratio of In/Zn/Sn = 10:70:20 with a mobility of 22 $cm^2\ V^{-1}\ s^{-1}$, a $V_{on}$ of 0.8 V, and a SS of 0.15 V/decade [90]. This optimized composition was achieved using a super-cycle consisting of one ZnO sub-cycle, one $In_2O_3$ sub-cycle, and two $SnO_2$ sub-cycles. When the indium and/or tin ratio was increased, mobility increased, but $V_{TH}$ shifted to the negative region. In this study, the authors pointed out that the multi-component mixing did not perfectly agree with the calculated composition based on the rule of mixtures. However, data accumulated by cation mapping and target composition could be achieved with ALD. IGZO cation mapping was studied by Cho *et al* [77]. Depending on the In–Ga–Zn ratio, the field effect mobility varied from under 10 $cm^2\ V^{-1}\ s^{-1}$ to over 100 $cm^2\ V^{-1}\ s^{-1}$ with a wide range of $V_{TH}$. Similar research was conducted for IZO by Lee *et al* who showed two sub-cycles of $InO_x$ and one sub-cycle of ZnO were the optimized compositions for TFTs with 30 $cm^2\ V^{-1}\ s^{-1}$ mobility [91].

Oxidants could be a variable in super-cycle design. Allemang *et al* suggested an oxidant-based hybrid super-cycle ($H_2O$ for the ZnO sub-cycle and $O_2$ plasma for the $SnO_2$ sub-cycle) that led to improved electrical characteristics compared to when only $H_2O$ was used in the deposition process [68]. This study found that oxygen vacancy control could be achieved in ALD using an oxidant. The effect of an oxidant on film properties is quite important in ALD-oxide semiconductors, which will be explained in detail in section 2.3.

*2.1.2. Homogeneous composition control via co-injection of metal precursors in multi-component oxide semiconductors.* Super-cycle-based composition control is not the only way to fabricate a multi-composition oxide semiconductor thin film in ALD. Co-injection of the precursors into the ALD chamber to obtain a desired metal ratio and cation contribution has been introduced by various researchers. This method exploits the competitive adsorption of precursors, by controlling the individual dosing amounts of precursors using precursor temperature, flow rate of carrier gas, or exposure time. Illiberi *et al* reported a co-injection method for trimethyl aluminum (TMA) and diethyl zinc (DEZ) precursors in spatial ALD (S-ALD) [92]. The authors suggested that precursor co-injection method allows not only superior control of film thickness, but also fully controllable stoichiometry of the $Al_xZn_{1-x}O$ thin film. Super-cycle-based composition control leads to inevitable nucleation delay when a multi-component fabrication is implemented, which can result in a discrepancy in total GPC and film thickness from the expected one. However, using the co-injection method retains the GPC, compared to individual binary oxide deposition ($GPC_{ZnO} = 0.20$ nm/cycles, $GPC_{Al2O3} = 0.12$ nm/cycles, $GPC_{AlZnO}$ = 0.12–0.20 nm/cycle). When TMA flow was increased from 0 to 57 $\mu$mol $min^{-1}$, the Al/(Zn + Al) ratio sharply increased from 6% to 42%. The X-ray photoelectron spectroscopy (XPS) depth profile revealed that the fabricated $Al_xZn_{1-x}O$ film had a constant cation ratio, from the surface to the bottom layer of the deposited film. Hsu *et al* reported Al-doped ZnO thin film fabrication using the co-injection method in S-ALD [93]. The co-injection of TMA and DEZ led to the high doping efficiency of 73%, while the Al atoms in the super-cycle-based Al–Zn–O (AZO) acted as impurities in the matrix rather than efficient dopants. Optimized efficiency could be obtained with a 41 °C temperature for both precursors, which resulted in 1% of Al content and a low resistivity of 3.5 × $10^{-4}$ Ω $cm^{-1}$, which is comparable to an ITO electrode. Illiberi *et al* reported a co-injection method, adopted for quaternary thin film fabrication, IGZO by S-ALD [94]. DEZ, trimethyl indium (TMIn), triethyl gallium (TEGa) were used as precursors and co-injected into a chamber for deposition with $H_2O$ as the oxidant. Although TMIn and TEGa do not react with the $H_2O$, the co-injection of TMIn/DEZ and TMIn/TEGa/DEZ led to the fabrication of IZO and IGZO, respectively. This suggests that DEZ activates the chemisorbed TMIn and TEGa to cause a polarity-induced dissociation of the remaining ligand groups, and the subsequent formation of reactive sites for the next precursor dosing step. Based on this result, the authors fabricated a 15 nm a-IGZO channel TFT which exhibited a 3.5 $cm^2\ V^{-1}\ s^{-1}$ of $\mu_{FE}$ and very low hysteresis. Illiberi *et al* also reported IZO fabricated by the co-injection method, and S-ALD, which had a high $\mu_{FE}$ of 30 $cm^2\ V^{-1}\ s^{-1}$ [95]. In this study, DEZ, TMIn and $O_2/N_2$ plasma were introduced as the metal precursors and oxidant. Depending on the exposure time of the precursors, a 0.13–0.70 In/(In + Zn) ratio could be achieved. TEM confirmed a homogeneous distribution could be achieved from bottom to top in amorphous IZO thin film using this method.

*2.1.3. Vertical gradient distribution in channel layer.* Compositional distributions of oxide semiconductors are not always homogeneous because of the inherent layer by layer deposition character of ALD. Unlike conventional PVD, a vertical gradient elemental distribution can be achieved in ALD by combining several super-cycles. For example, if $AO_x$ is a conductive but defective oxide semiconductor, and $BO_y$ is an insulating but defect-less structured oxide semiconductor, we could assume that the design of a TFT as an A-rich/B-poor front channel and A-poor/B-rich back channel would be superior in mobility and reliability than a homogeneous $ABO_x$ channel layer, which is illustrated in figure 3(b).

Gradient distribution of the AZO channel in TFT was reported by Ahn *et al* [87]. In their study, three different sequences of super-cycles were employed: 19/1, 9/1, 6/1 of Zn–O/Al–O sub-cycles to achieve 95:5, 90:10, 86:14 at% Zn:Al composition ratios, respectively. They compared Channel 1, which had ascending step compositions (5/10/14 at% in Al composition) and Channel 2, which had descending step compositions (14/10/5 at% in Al composition). The mobility and reliability of the TFTs varied depending on the Al composition in the front and back-channel region, which indicates the importance

of compositional distributions of 0.05 $cm^2\ V^{-1}\ s^{-1}$ in Channel 2 and 0.6 $cm^2\ V^{-1}\ s^{-1}$ in Channel 1. Also, when the Al contents of the front-channel decreased to 0 at%, the mobility increased to 4.5 $cm^2\ V^{-1}\ s^{-1}$. Reliability also increased more in Channel 1 than Channel 2, because the high Al ratio in the back-channel resulted in fewer defect sites. When the number of sub-cycles of one element increased enough to form one discrete layer, or many super-cycles were conducted before another sequence of super-cycles were performed, individual layers could be formed in the vertical direction.

The influences of the vertical position of Al locally doped into a ZnO matrix was reported by Chung *et al* [96]. The thickness of the Al doped region was about 2 nm in all cases, as confirmed by TEM, and the Al doped region varied by 0, 5, 10, 15, 18 nm with respect to the interface of the channel and gate insulator in the bottom gate inverted staggered TFT. The fabricated TFT exhibited varied distribution in $\mu_{sat}$. When the Al doping region (∼7 at%) was increasingly distant from the depletion region, the significantly decreased $\mu_{sat}$ (0.3 $cm^2\ V^{-1}\ s^{-1}$) compared to the original ZnO TFT (4.5 $cm^2\ V^{-1}\ s^{-1}$) gradually recovered. Interestingly, above a certain thickness, the Al doped region seemed to have no impact on the electrical performance of the TFT, which could indicate the accumulation width in the channel. Further study of Al doping concentration and vertical position revealed that back-channel doping highly influenced to the $V_{TH}$ shift, and front-channel doping to $\mu_{sat}$. Optimized Al:ZnO channel exhibits 30% increased $\mu_{sat}$ (6.0 $cm^2\ V^{-1}\ s^{-1}$) compared to the original one. This vertical element distribution could be converted to a dual/multi-channel. Studies of such channels fabricated by ALD are explained in section 2.2.

Vertically gradient cation design and the subsequent film characteristics were also evaluated for application as a passivation layer. Zhao *et al* reported improved photoelectric and passivation properties by fabricating a gradient Al:ZnO film using ALD [97]. In this study, the authors adopted the gradient film fabrication method to achieve low internal stress and strong adhesion to interfaces. The 80 nm of gradient Al:ZnO was deposited by continuously changing the sub-cycle ratio of Al–O/Zn–O from 1/32 to 1/0 cycles. Five different samples with varied Al concentration gradients (0.09, 0.46, 0.71, 0.96, and 1.21% $nm^{-1}$), were fabricated and evaluated, and calculated using the XPS analysis of Al content in the Al:ZnO surface, and the interfaces between the Al:ZnO and substrates. The detailed calculation is described in the reference paper. When the Al gradient was increased from 0 to 1.21% $nm^{-1}$, crystallinity diminished, and conductive properties deteriorated. This resulted in the development of surface passivation properties. The optimal passivation performance was exhibited by the gradient film of 0.71% $nm^{-1}$ with a minority carrier lifetime of 120.6 $\mu$s and a resistivity of $1.89 \times 10^{-2}\ \Omega\ cm^{-1}$.

### 2.2. Vertical structure engineering

Homogenous oxide semiconductors deposited by the conventional PVD process have limitations boosting on-current and/or $\mu_{FE}$ because of their uniform carrier distribution. Oxide based TFTs with a homogenous active layer have a trade-off relationship between $\mu_{FE}$ and $V_{TH}$ because these parameters are closely related to the carrier concentration of the channel layer [98, 99]. For this reason, devices with high $\mu_{FE}$ characteristics typically exhibit large negative $V_{TH}$ values [6, 100]. Therefore, they cannot be used in terms of operating voltage. In contrast to a homogeneous active layer, ALD-derived oxide-semiconductors have the advantage of main channel tunability, for multi-channel and dual-channel. In addition, the main channel engineered oxide semiconductors exhibit good interface quality between the channels because of the conformality of the ALD process. In this section, we have described vertical structure engineering within the active layer using the ALD process.

*2.2.1. Nano-laminated channel layer.* Figure 4(a) shows the electrical characteristics of ALD-derived nano-laminated $(InO_x)_n(GaZnO_y)_m$ TFTs [101]. Here, the main lateral electron path via drain voltage is determined by the $InO_x$ layers because the $InO_x$ has a lot of oxygen vacancies, and the spherical 5 s orbitals of indium ions generate an overlapped orbital string. In addition, the $GaZnO_y$ layers act as barriers to the out-diffusion of oxygen in the $InO_x$ layers and suppresses the electron transmission path along the vertical channel. Therefore, as the thickness of the $InO_x$ layer increases from 4 nm to 6 nm, $V_{TH}$ negatively shifts from $-3.03 \pm 0.85$ to $-8.21 \pm 0.50$ V, and $\mu_{FE}$ is increased from $9.88 \pm 0.19$ to $18.00 \pm 0.63$ $cm^2\ V^{-1}\ s^{-1}$. However, with a further increase in $InO_x$ layer thickness from 6 nm to 8 nm, the $V_{TH}$ more negatively shifts from $-8.21 \pm 0.50$ to $-12.2 \pm 0.94$ V, whereas $\mu_{FE}$, SS, and hysteresis significantly decrease ($\mu_{FE}$: $18.00 \pm 0.63 \rightarrow 5.66 \pm 0.26$ $cm^2\ V^{-1}\ s^{-1}$, SS: $0.67 \pm 0.08 \rightarrow 0.82 \pm 0.02$ V/decade, hysteresis: $0.34 \pm 0.20 \rightarrow 0.61 \pm 0.25$ V). This result is closely related to an increase in acceptor states in both the interface and bulk nano-laminated films, despite increasing carrier concentration. The origin of the increase in acceptor states turned out to be an increase in defect states resulting from $InO_x$ crystallization at a specific thickness. The controllability of the active channel layer was also demonstrated in the ZnO nanolayers. Ahn *et al* reported a $ZnO/Al_2O_3$ superlattice active channel layer fabricated by an *in-situ* ALD process [102]. The $E_g$ of the ZnO was lower than that of $Al_2O_3$, while electron affinity was high, resulting in quantum confinement of the ZnO by the $Al_2O_3$ layers. As a result, the superlattice $ZnO/Al_2O_3$ TFT exhibited significantly improved SS ($0.7 \rightarrow 0.3$ V/decade) and $\mu$FE ($4.8 \rightarrow 27.8$ $cm^2\ V^{-1}\ s^{-1}$) compared to the single ZnO TFT.

Similarly, Kim *et al* reported hybrid semiconducting superlattices with a ZnO/4-mercaptophenol (4MP) organic layer [103]. The ZnO and 4MP layers were deposited by alternating ALD and MLD processes. Single ZnO and hybrid superlattice ZnO/4MP TFTs were evaluated at temperatures from 300 to 90 K, to determine the charge transport mechanism. The single ZnO TFT showed typical hopping conduction, while the superlattice ZnO/4MP TFT exhibited a band-like transport model. These results mean that the superlattice ZnO/4MP active layer can form ZnO-derived quantum wells. The

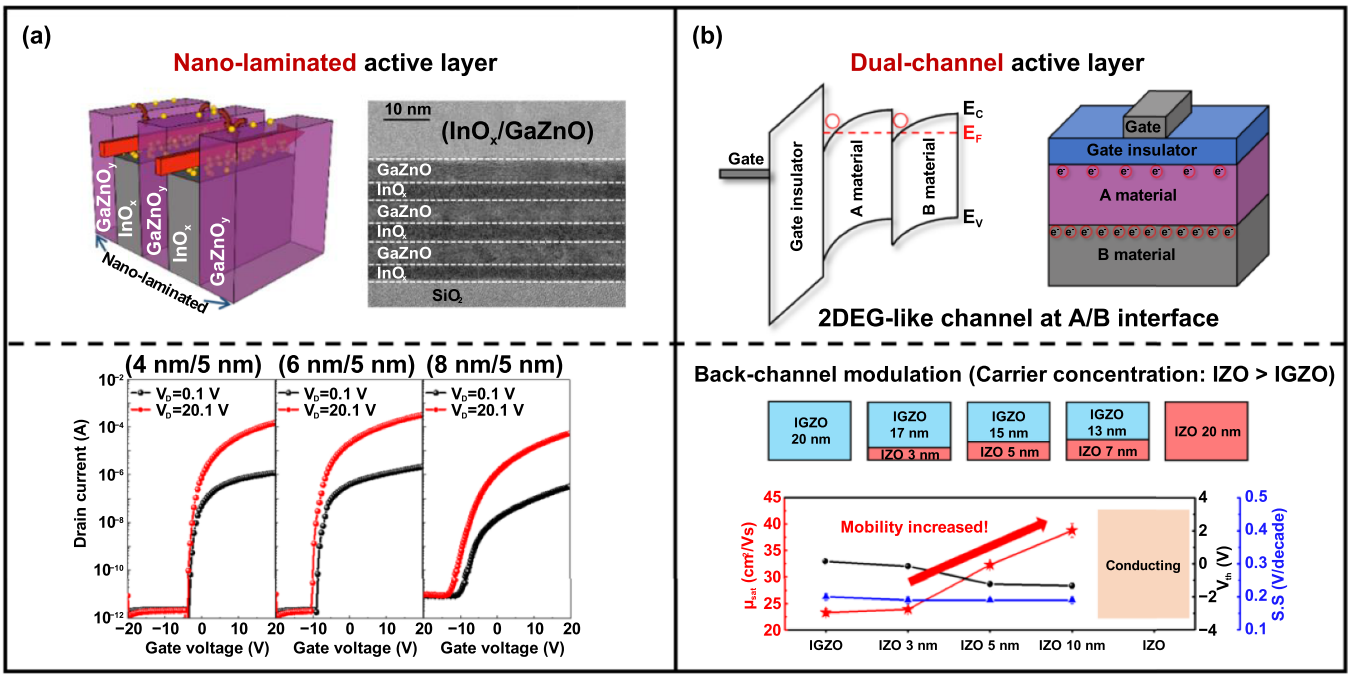


**Figure 4.** Description of ALD benefit 2: vertical structure engineering of active layer. (a) Schematic and cross-sectional TEM images of the nano-laminated active layer. The devices showed negative $V_{TH}$ shift with increasing $In_2O_3$ thickness, which confirmed the possibility of electron pathways via the $InO_x$ layer by T-CAD simulation. (b) Band diagram and schematic showing the turn-on state of the active layer fabricated by two different materials. A 2DEG-like channel was formed at the interface of the two different materials by engineering the properties of the materials. The devices showed increased $\mu_{sat}$ with a back-channel thickness at a fixed total active layer thickness.

dependence of the ZnO-derived quantum wells was verified by the multiple stacks of 4 nm and 0.7 nm-thick ZnO and 4MP, respectively. The single-stack, double-stack, and triple-stack were designated 4MP/ZnO/4MP, 4MP/ZnO/4MP/ZnO/4MP, and 4MP/ZnO/4MP/ZnO/4MP/ZnO/4MP. The intrinsic electron field-effect mobility ($\mu_{4p}$) and SS were enhanced from 30 to 73 $cm^2\ V^{-1}\ s^{-1}$ and from 165 to 110 mV/decade, respectively, increasing from single to triple quantum wells.

*2.2.2. Dual-channel layer.* Considering the bandgap and Fermi-energy level of the two different semiconductor materials, an additional two-dimensional electron gas (2DEG)-like channel can be formed at the junction interface of the stacked active layer. This is attributed to the increase in on-current and/or $\mu_{FE}$ of the device [104, 105]. Figure 4(b) represents an ALD-derived dual-channel active layer consisting of two different oxide semiconductor layers [12]. The front-channel layer consists of IGZO material with semiconductor properties (conductivity: $0.10 \pm 0.01$ S $cm^{-1}$), whereas the back-channel was a conducting IZO material (conductivity: $584.49 \pm 32.22$ S $cm^{-1}$). In the stacked active layer, the back-channel thickness varied from 0 to 20 nm, with a total thickness of 20 nm. The saturation mobility ($\mu_{sat}$) value obviously increased with back-channel IZO thickness, and eventually the $\mu_{sat}$ increased by about 60% with an IZO thickness of 10 nm. The reason for the increase in $\mu_{sat}$ was clearly revealed by technology computer-aided design (TCAD) simulations. Compared to a single IGZO channel, an additional 2DEG-like channel formed at the IZO layer under a driving gate voltage ($V_{GS} = 20$ V) in the IGZO/IZO stacked active layer. Similarly, the possibility of a 2DEG-like channel formation using hetero-junctions such as IGO/GZO, IZO/GZO, and IGO/ZnO materials has been reported [62, 106]. Bandgap and Fermi-energy level engineered homo-junction IGZO active layers were also reported.

It has also been reported that $Ga_2O_3$ has a large bandgap and narrow valence band level compared to that of $In_2O_3$ [107, 108]. In addition, $Ga_2O_3$ acts as a carrier suppressor, while the $In_2O_3$ participates in carrier generation in the IGZO system [2]. Therefore, a key factor in the homo-junction IGZO active layer is controlling the $Ga_2O_3$ and/or $In_2O_3$ composition. Cho *et al* reported a bilayer IGZO channel structure consisting of a 10 nm base layer ($In_{0.52}Ga_{0.29}Zn_{0.19}O$) and a mobility boost layer ($In_{0.82}Ga_{0.08}Zn_{0.10}O$) [77]. As a result, downward band bending of the conduction band maximum energy near the interface between the mobility boost layer and the base layer was observed, which is similar to the 2DEG-like channel formation. In addition, Bae *et al* fabricated a composition-modified bilayer IGZO channel using a 3 nm thick In-rich prompt layer and a 12 nm thick prime layer [109]. Compared to the single prime layer ($In_{0.32}Ga_{0.22}Zn_{0.46}O$), the 3 nm thick prompt IGZO ($In_{0.48}Ga_{0.11}Zn_{0.41}O$ or $In_{0.53}Ga_{0.11}Zn_{0.36}O$) layer produced an energy quantization effect due to the formation of quantum confinement wells at the junction surface. Therefore, the single prime layer IGZO TFT showed a 19.6 $cm^2\ V^{-1}\ s^{-1}$ $\mu_{sat,}$ while the 3 nm thick prompt IGZO layer boosted the $\mu_{sat}$ up to 45.5 $cm^2\ V^{-1}\ s^{-1}$.

### 2.3. Chemical reaction and film properties

In contrast to PVD, the distinguishing variables in ALD are extracted from the chemical reaction. The main variables that can significantly influence the reaction pathway (physisorption and chemisorption) and product (thin film and by-product) include precursors and reactants and process conditions such as growth temperature. Analyzing these variables becomes more important for multi-component deposition, because the density of the reactive sites on the surface and the physisorption/chemisorption energy of the components can differ depending on the chemical reactions. Using table 1, we determined that studies of indium-based oxide semiconductors have greatly increased since 2021. Not only binary $In_2O_3$ [42–49], but also a ternary as IGO [59–62], IZO [62, 63], In–Al–O (IAO) [64, 65] and ITO [66], quaternary as IGZO [4, 30, 71–80], ITAO [81, 82], and ITGO [83] have been introduced. Also, compared to other materials in table, the precursors for indium oxide are variously used. This is because lack of proper indium precursor which have low cost, high reactivity, and sufficient vapor pressure with a preferred liquid phase, while TMA, DEZ, and trimethyl gallium (TMGa) have been predominantly used. There is an inevitable question in this regard. Is there any difference between two TFTs which have oxide semiconductor channel with identical or similar cation ratio, but different precursors are used during deposition process? This is significant for future applications of ALD oxide semiconductors, but such a study has yet been reported. Accordingly, we will discuss a case study of binary indium oxide, which has been widely studied with various precursors. In this section, we introduce the properties of the ALD-deposited films, their dependence on processing variables related to chemical reactions, and we provide a case study of how a binary oxide ($In_2O_3$) depends on such variables, as shown in table 2.

*2.3.1. Importance of chemical reaction related variables in binary system: case study of indium oxide.* For ALD, the selection of a proper precursor is the first challenge because there are several requirements, including vapor pressure, viscosity, no self-decomposition, unreactive with by-products, cost, etc [126, 127]. A second problem is controlling the properties (e.g., metal–oxygen ratio, impurity level, and electrical properties) of the film being fabricated with the selected precursor. Various oxidants are also exploited as reactants for ALD-oxide semiconductors, including oxygen-based plasma, $O_3$, $O_2$, $N_2O$, $H_2O_2$ and $H_2O$. The oxidizing power of the reactant can determine the metal-oxygen ratio, impurity level, and the phase of the material. The importance of precursor/oxidant selection in a binary system will be discussed, using a case study of indium oxide ($In_2O_3$).

$In_2O_3$ is a well-known transparent conducting oxide (TCO) with a wide bandgap ($\geqslant$3.3 eV), high transmittance (>90%), low resistivity (0.1–1 m$\Omega$ cm) and high carrier concentration ($10^{18}$–$10^{20}$ $cm^{-3}$). Recently, with the demand for high current level on-current and mobility in a few-nanometers thick channel, indium-based oxide semiconducting materials have received additional attention. A more detailed discussion of this is provided in section 3. In this part, we would first like to focus on the precursor and reactants. Many studies have been published In ALD based oxide semiconductor TFTs, including $In_2O_3$, because of their superior electrical performance. Various indium precursors and oxidants have been employed to achieve $In_2O_3$ thin films, as listed in table 2. Interestingly, the film properties have varied depending on the precursor structure and oxidants.

First, we compared the ALD behavior for various precursor structures using identical kinds of reactants from the table. Film properties such as growth temperature and crystallinity were similar when ozone was used as an oxidant and TMIn [111] and TEIn [113] as precursors. However, those of $In(acac)_3$ [119], InCp [116], InCA-1 [113], DADI [113] were all different. Differences in ligand structures, and the bulkiness and viscosity of the precursors are the main variables influencing growth per cycle (GPC), and they can have a clear influence on film properties. Maeng *et al* reported such precursor dependencies using InCA-1, DADI, TEIn and ozone as a co-reactant [113]. This comparative study revealed that TEIn, a precursor that is highly reactive with ozone, tended to have a moderate GPC (0.6 Å/cycle; while InCA-1 and DADI had 0.8 and 0.5 Å/cycle, respectively) but enhanced electrical performances, such as Hall mobility (48.7 $cm^2$ $V^{-1}$ $s^{-1}$; while InCA-1 and DADI had 8.6 and 29.2 $cm^2$ $V^{-1}$ $s^{-1}$, respectively). This indicates the importance of precursor selection, especially for channel deposition.

Secondly, the influences of oxidants on film properties could be deduced from two studies of TMION by Hong *et al* using plasma [60], and Lee *et al* using $H_2O$ [42]. The former study exhibited about five-times higher GPC and Hall mobility than the latter case, which could be attributed to the higher oxidizing power of the plasma sources and the subsequent formation of a dense $InO_x$ thin film. Meanwhile, some researchers reported a more developed GPC could be obtained by combining two different oxidants. Libera *et al* revealed that InCp had a low growth rate of 0–0.15 Å/cycle when $O_2$ or $H_2O$ were used individually as oxidants, while InCp had a highly enhanced growth rate of 1.0–1.6 Å/cycle when both were used in combination [114]. Interestingly, the order of oxidant exposure also influenced the growth rate. GPC was much higher when $H_2O$ exposure was followed by $O_2$ exposure (called WO) than when $O_2$ exposure was followed by $H_2O$ exposure (called OW). The origin of the differences between WO and OW were analyzed using *in-situ* quadrupole mass spectrometry (QMS) and quartz crystal microbalance (QCM) measurements. QCM and QMS data was measured during the 60–70 ALD cycle for InCp and each reactant pair, and the collected data revealed the $In_2O_3$ ALD sequence. Firstly, the Cp ligand is released after the precursor I exposed on the surface: this is the chemisorption step for InCp. Secondly, when $H_2O$ is exposed to the chemisorbed precursor, the remaining ligand groups are released, and reactive sites (−OH) are generated. However, indium still has a low oxidation state ($In^{+1}$) for constructing an $In_2O_3$ ($In^{+3}$) phase. Finally, $O_2$ exposure leads to the oxidization of indium ($In^{+1}$ to $In^{+3}$). This sequential process of the reactant pair (WO) resulted in a highly developed GPC. A similar result was observed by Kobayashi

**Table 2.** ALD processes reported for indium oxide[a]. The table includes the precursor and reactant information, ALD growth temperature, growth per cycle, impurity level, band gap, crystallinity, Hall mobility and TFT mobility.

| | Precursor[b] | Reactant | Growth temperature (°C) | GP (Å/cycle) | Impurity (%) | Band gap (eV) | Crystallinity | Hall mobility ($cm^2\ V^{-1}\ s^{-1}$) | TFT mobility ($cm^2\ V^{-1}\ s^{-1}$) | References |
|---|---|---|---|---|---|---|---|---|---|---|
| Indium oxide | $InCl_3$ | $H_2O$ | 400–500 | 0.23–0.27 | N/S | N/S | Cubic | 63–72 | N/S | [110] |
| | TMIn | $H_2O$ | 200–251 | 0.39 | N/S | N/S | N/S | 84 | N/S | [111] |
| | | Ozone | 100–200 | 0.41–0.54 | C 1.5 | 3.6 | Cubic $\geqslant$ 200 °C | 12–50 | N/D | [112] |
| | TEIn | Ozone | 50–250 | 0.6–0.8 | N/D | 3.8–4.4 | Cubic $>$ 200 °C | 4.0–48.7 | N/D | [113] |
| | InCp | $H_2O/O_2$ | 100–250 | 1.0–1.6 | N/S | N/S | Cubic $>$ 140 °C | 38–111 | N/S | [114] |
| | | $H_2O_2$ | 160–200 | 1.4–1.5 | C 1.1–6.9 $\leqslant$180 °C | 3.4–3.8 | Cubic $\geqslant$ 170 °C | N/S | 7.8 | [115] |
| | | Ozone | 200–450 | 1.3–2.0 | N/S | N/S | Cubic at 275 °C | N/S | N/S | [116] |
| | In-EtCp | $H_2O$/ozone | 150–200 | 1.8–2.1 | C 1.3–1.8 <200 °C | N/S | Amorphous | N/S | 20.4 | [117] |
| | $In(tmhd)_3$ | $Ar/O_2$ plasma | 100–400 | 0.14 | C | 3.6 | Cubic $>$ 100 °C | N/S | N/S | [118] |
| | $In(acac)_3$ | $H_2O$ | 165–200 | 0.20 | N/S | N/S | Cubic $\geqslant$ 175 °C | N/S | N/S | [119] |
| | | Ozone | 165–225 | 0.12 | N/S | N/S | Amorphous | N/S | N/S | |
| | $Me_2In(edpa)$ | $H_2O$ | 150–300 | 0.1–0.8 | N/D | 3.7 | Cubic $\geqslant$ 200 °C | 1.1–66 | N/S | [120] |
| | InCA-1 | Ozone | 50–250 | 0.8–1.0 | N/D | 3.9–4.5 | Cubic $\geqslant$ 200 °C | 0.3–8.6 | N/S | [113] |
| | | $H_2O$ | 175–275 | 0.7 | C $<$ 200 °C | 3.8–4.1 | Cubic $\geqslant$ 200 °C | 0.5–24 | N/S | [121] |
| | | $H_2O_2$ | 150–200 | 0.7 | N/S | 4.0[e] | Cubic $\geqslant$ 200 °C[e] | 2.2–20.2 | N/S | [122] |
| | | $Ar/O_2$ plasma | 100–250 | 1.45 | C 2.5–3.9 $\leqslant$150 °C Si 1.6–3.4 | 3.5–3.6 | Amorphous | 11.0–20.2 | 39.2 | [123] |
| | DADI | Ozone | 50–250 | 0.3–0.8 | N/D | 3.8–4.5 | Cubic $\geqslant$ 200 °C | 8.2–29.2 | N/S | [113] |
| | | $H_2O$ | >275 | 0.6 | C $>$ 1 | 3.6 | Cubic | 13.1 | N/S | [124] |
| | | $Ar/O_2$ plasma | 100–250 | 0.8 | N/D | 3.5[e] | Cubic | 8.0[e] | N/S | [60] |
| | TMION | $H_2O$ | 100–250 | 0.18–0.35 | C $<$ 150 °C | N/S | Rhombohedral $<$ 200 °C Cubic $\geqslant$ 200 °C | 1.0 | 6.1 | [42] |
| | | $Ar/O_2$ plasma | 100–250 | 0.75 | N/D | 3.2[e] | Cubic | 3.2[e] | N/S | [60] |
| | DMION | $Ar/O_2$ plasma | 35–300 | 1.2 | N/D | 3.4–3.5 | Cubic | 3.1–33.1 | 0.2–34.4 | [48] |
| | DATI | $Ar/O_2$ plasma | 100–250 | 1.0–1.1 | N/D | 3.4–3.5 | Cubic | 11.3–17.3 | 10.9–17.5 | [125] |

[a] Presented film properties and GPC in table is extracted from the references.

[b] Precursor names represent the chemicals as follows: indium (II) chloride (InCl), trimethylindium (TMIn), triethylindium (TEIn), indium (I) cyclopentadienyl (InCp), ethylcyclopentadienyl indium (InEtCp), tris(2,2,6,6,-tetramethyl-3,5-heptanedionato)indium ($In(tmhd)_3$), indium (III) acetylacetonate ($In(acac)_3$), dimethyl(N-ethoxy2,2-dimethylcarboxylicpropanamide)indium ($Me_2In(edpa)$), bis(trimethylsilyl)amidodiethyl indium (InCA-1), (3-dimethylaminopropyl)dimethylindium (DADI), trimethyl[$N^1$-(tert-butyl)-$N^2$, $N^2$-dimethylethane-1,2-diamine]indium (TMION), dimethyl[$N^1$-(tert-butyl)-$N^2$, $N^2$-dimethylethane-1,2-diamine]indium (DMION), [dimethylbutyamino]trimethylindium (DATI).

[c] N/D: Not detected (in the reference).

[d] N/S: No report (No data).

[e] Not shown in the reference, evaluated by the authors of this manuscript.

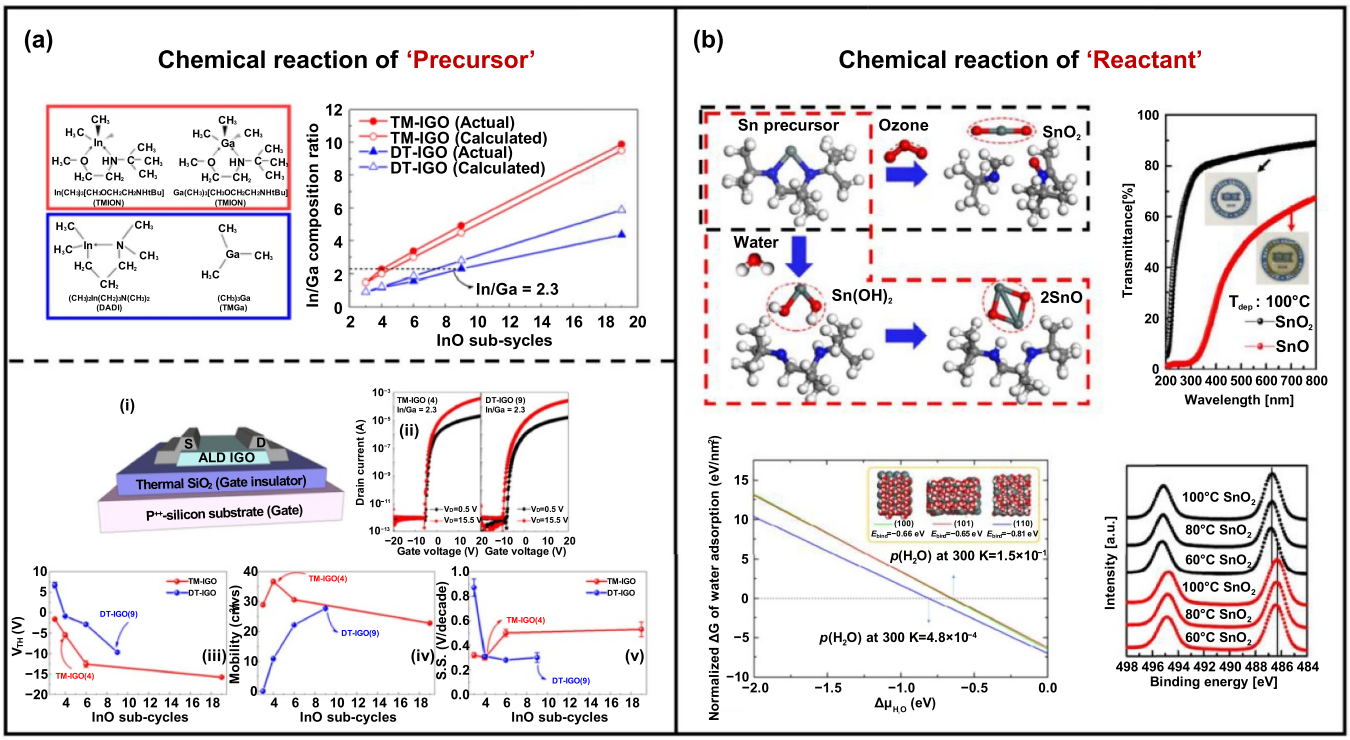


**Figure 5.** Description of ALD benefit 3: Representative studies on how chemicals influence the properties of ALD oxide semiconductors. (a) Precursor selection in a multi-component system by studying precursor pairing in IGO-TFT. Reprinted with permission from [60]. Copyright (2021) American Chemical Society. (b) Reactant selection in oxide semiconductor based on a study of how tin oxide phases varied depending on oxidants. Reprinted with permission from [128]. Copyright (2018) American Chemical Society.

*et al* using In-EtCp as a precursor [117]. The different roles of the two oxidants led to improved results, in that $H_2O$ releases ligands or byproducts from the surface and $O_2$ oxidizes the indium. Mane *et al* also reported the importance of reactants in a study of ALD-$In_2O_3$ using TMIn with various reactants [112]. These studies imply that the oxidizing power of the precursor is important, but the generated byproducts are also important because they may degrade performance depending on the oxidant used.

*2.3.2. Importance of precursor chemical reaction in a multi-component oxide semiconductor.* Figure 5(a) shows a study of IGO-TFT with paired indium and gallium precursors by Hong *et al* [60]. In the study, two different precursor pairings were compared: the first pair were structurally identical precursors, $In(CH_3)_3[CH_3OCH_2CH_2NHtBu]$ (TMION) and $Ga(CH_3)_3[CH_3–OCH_2CH_2NHtBu]$) (TMGON), referred to as TM-IGO, and the second pair had structurally different precursors, $(CH_3)_2In(CH_2)_3N(CH_3)_2$ (DADI) and $(CH_3)_3Ga$ (TMGa), which are referred to as DT-IGO. With the DT-IGO, increasing discrepancies appeared between the experimental GPC of the IGO and the calculated GPC of IGO, from the GPC of each bilayer ($In_2O_3$ and $Ga_2O_3$) and between the metal ratios as the number of IGO super-cycles increased. In contrast, with TM-IGO the discrepancies did not increase. The DT-IGO TFT exhibited a larger number of oxygen defects, which resulted in a negative position of $V_{TH}$ even at a similar metal ratio to TM-IGO (−5.5 V in TM-IGO and −9.7 V in DT-IGO). Also, depending on the precursor pair (TM-IGO and DT-IGO), the shift in electrical properties, such as $V_{TH}$, $\mu_{FE}$, and SS, as a function of the $InO_x$ sub-cycles were different. This was attributed to differences in the crystal structure, grain boundaries, metal/oxygen ratio, and oxygen bonding states. This clearly indicates that the continuous change in surface-chemistry significantly influenced to the deposition process of the multi-component system, which resulted in varied film/device properties. This effect can be minimized when the proper precursor pairs are selected. Sheng *et al* reported another study which revealed the importance of precursor chemistry in multi-component oxide semiconductors [129]. In the study, IGO film deposition was carried out using DADI and TMGa with $H_2O_2$ as a reactant. Using TMGa and $H_2O_2$, a $Ga_2O_3$ binary system could not be fabricated. Density functional theory (DFT) calculations revealed that this was because TMGa was chemisorbed on the In–$O_x$ surface, since the energy barrier to chemisorption on Si–$O_x$ was too high. A similar study was presented by Kim *et al* [69]. These authors reported that the incubation cycles (∼30 cycles) of DEZ on a Si surface decreased and exhibited no incubation cycles on $SnO_2$ substrates. This resulted from the strong oxidizing power of $SiO_2$, which led them to inject ozone to oxidize both the adsorbed Zn precursor and the bare Si substrate. Based on this behavior, the required ozone feeding time was decreased from 4.5 s to 0.25 s for the ZTO film depositions.

Precursor selection is also important in terms of doping efficiency for multi-component systems. Lee *et al* suggested more controlled Al doping could be achieved when dimethylaluminum isopropoxide (DMAI) was selected rather

than TMA for IAO deposition [64]. Using DFT calculations, they suggested two reasons for this: (a) the smaller molecular size of TMA leads to higher Al coverage on the surface and hinders the deposition of the next indium molecules, and (b) highly reactive TMA could take In from the surface like an etching process, while less reactive DMAI could not. For these reasons, by using DMAI precursors, Al content could be precisely controlled even at the sub-nanometer scale.

*2.3.3. Importance of the other variants in chemical reaction in the oxide semiconductor.* Figure 5(b) presents a study of ALD-$SnO_x$ using N,N′-*tert*-butyl-1,1-dimethylethylenediamine stannylene(II) precursor and two different reactants, $H_2O$ and $O_3$, by Lee *et al* [128]. The ALD behaviors of SnO using $H_2O$ and $SnO_2$ using $O_3$ as reactants were studied. Interestingly, both the fabricated film properties and phases were different, and different GPC and film growth temperatures were observed as well. Unlike the $O_3$-deposited $SnO_2$, which had a wide ALD window of 80 °C–250 °C with a GPC of about 1.2 Å/cycle, $H_2O$-deposited SnO had a narrow ALD window, below 150 °C, and GPC decreased with increasing growth temperature. This was attributed to the drop in $H_2O$ adsorption rate when the growth temperature increased, which was confirmed by DFT calculations. Also, the combination of two different oxidants can enhance ALD growth behavior and film properties.

Various process conditions also had an influence on the fabricated film properties. Lee *et al* reported a case study on how $In_2O_3$ growth depended on the growth temperature [42]. It is well known that the thermally stable crystal structure of $In_2O_3$ is a cubic bixbyite structure, while the rhombohedral structure is a metastable phase. However, the authors of the study suggested that a rhombohedral $In_2O_3$ structure was fabricated at temperatures below 150 °C due to the low decomposition temperature and interface-related crystal growth. Growth temperature also influenced the metal–oxygen ratio and impurity levels. A vertical temperature-gradient ZnO-TFT was fabricated and evaluated by Che *et al* [50]. At 100 °C, lower carrier concentrations and Hall mobility were revealed, compared to a ZnO film fabricated at 200 °C. These authors deposited ZnO front-channels at 200 °C and end on back-channels at 100 °C, and the resulting TFT exhibited enhanced mobility and stability. This was attributed to the degraded crystallinity and equalized carrier concentration, induced by combining a ZnO film in temperature-gradient conditions. Process temperature also influences the fabrication of multi-component oxide semiconductors. Half-reactions of indium precursor on the Si–OH surface varied depending on the growth temperature, which influenced the reaction site (–OH) density of subsequent zinc precursors, as studied by Sheng *et al* [122]. This led to a discrepancy between the theoretical GPC and experimental GPC of IZO, and associated differences in mobility and stability depending on temperature. Dosing sequence and purge times can also be variables. Chen *et al* noted the importance of purge time on the electrical performances of ZnO TFTs [130]. In ZnO-TFTs, TFTs fabricated with purge times greater than 20 s exhibited higher stability than the lower purge time sets. This is because oxygen vacancies and impurities in ZnO gradually decreased with increasing purge time (5–30 s).

### 2.4. Insulator and interface engineering

Instability under gate bias temperature stress conditions is especially important in the display and semiconductor fields because this instability leads to non-uniformity in display products or malfunctions in memory devices. Hydrogen and oxygen species are important factors which determine instability and the electrical characteristics of oxide-based TFTs [131–136]. These species can be transferred from the insulator into the active layer during the device fabrication process, because the insulator (e.g., buffer layer, gate insulator, passivation layer, and interlayer dielectric) deposited by conventional CVD process has a fairly large amount of hydrogen or oxygen [137, 138]. However, because the ALD process can control single atomic layers, it is relatively easy to control the amount of hydrogen or oxygen species in the insulator via process parameters [139]. In addition, ALD allows the fabrication of functional insulation materials because it gives us the freedom of an *in-situ* process for depositing two different insulation materials. In this paragraph, we discuss the advantages of ALD-derived insulation materials and the relationship between the insulator deposition process and the instability characteristics of oxide-based TFTs.

*2.4.1. Functional insulators.* Hydrogen is considered a source for n-type donors in oxide semiconductors because hydrogen has two types of donor-like states: interstitial hydrogen ($H_i^+$) bonded to an oxygen atom and substitutional hydrogen ($H_O^+$) located at an oxygen vacancy [134, 140, 141]. In addition, hydrogen can exist as bi-stability acceptor-like centers, which can degrade device stability [134, 136]. Therefore, to ensure adequate electrical characteristics and the stability of the device it is important to prevent hydrogen from incorporating into the active layer.

Figure 6(a) shows functional gate insulators made using ALD-derived $SiO_2$ and $Al_2O_3$ [76]. The hydrogen gas permeability of each material was determined using a constant-volume/variable pressure system (time-lag). The measured hydrogen permeability of $SiO_2$ was higher than that of $Al_2O_3$ ($SiO_2$: $4.46 \times 10^{-11}$ $cm^3$ cm/cm · Hg·$cm^2$·s, $Al_2O_3$: $7.18 \times 10^{-12}$ $cm^3$ cm/cm · Hg·$cm^2$·s). Based on this insight, an $Al_2O_3/SiO_2$ stacked gate insulator was deposited using an ALD *in-situ* process on the active layer in a top-gate bottom-contact structure, to effectively prevent hydrogen incorporation into the active layer. The ability to prevent hydrogen incorporation was tested by annealing at 300 °C for 12 h in a forming gas (90% $N_2$ + 10% $H_2$) ambient (hydrogen annealing, hereafter). The device with a $SiO_2$ gate insulator revealed a negative $V_{TH}$ shift of −0.97 V and an increased SS of 0.07 V/decade after hydrogen annealing. However, the device with the $Al_2O_3/SiO_2$ functional gate insulator showed negligible $\Delta V_{TH}$ and ΔSS values of −0.15 V and 0.01 V/decade, respectively. These results mean that incorporated hydrogen species were blocked by the $Al_2O_3$ layer. To evaluate the

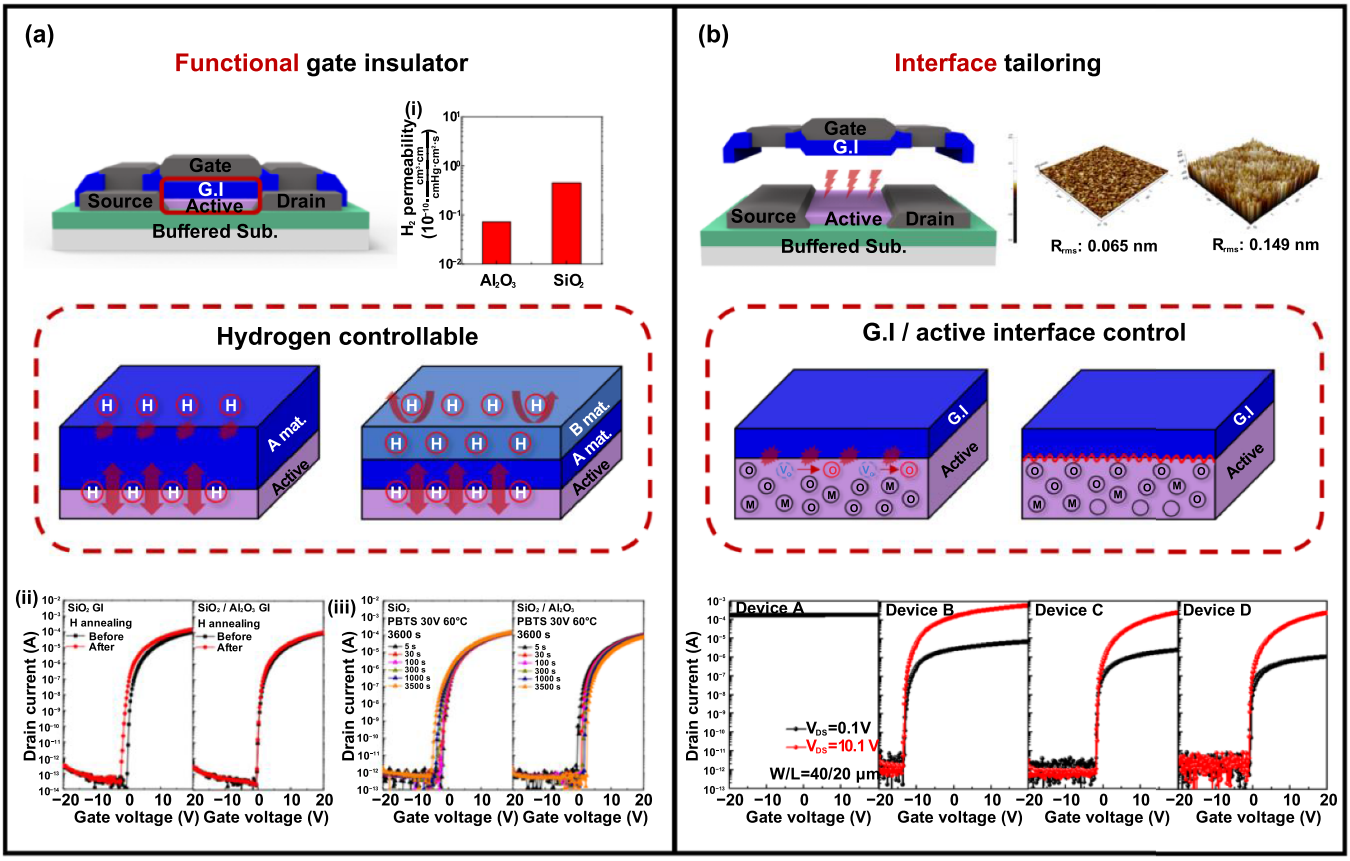


**Figure 6.** Description of ALD benefit 4: insulator and interface engineering. (a) Schematic of a functional gate insulator on the top-gate bottom-contact IGZO TFT to prevent hydrogen incorporation into the active layer. Exploiting the difference in hydrogen permeability of the $Al_2O_3$ and $SiO_2$ materials, a functional gate insulator was fabricated using an $Al_2O_3/SiO_2$ stack. The devices with conventional and functional gate insulators were evaluated for PBTS stability. © [2021] IEEE. Reprinted, with permission, from [76]. (b) A schematic of interface tailoring achieved by controlling gate insulator deposition conditions of the top-gate bottom-contact IZO TFT. The devices show completely different electrical characteristics depending on plasma power during the gate insulator deposition by PEALD. © [2022] IEEE. Reprinted, with permission, from [63].

effects of incorporated hydrogen on PBTS instability, these devices were stressed at a gate voltage of 30 V at a temperature of 60 °C. The device with the $SiO_2$ gate insulator showed an abnormal negative $V_{TH}$ shift of −2.80 V and an increased SS of 0.09 V/decade after the PBTS test, while the device with the $Al_2O_3/SiO_2$ functional gate insulator showed a typical positive $V_{TH}$ shift of 2.32 V and no change in SS. Considering the hydrogen permeability of $SiO_2$ and $Al_2O_3$, more hydrogen was included in the $SiO_2$ gate insulator compared to the $Al_2O_3/SiO_2$ functional gate insulator. Therefore, the abnormal behavior of the device with the $SiO_2$ gate insulator resulted from hydrogen diffusion into the active layer, or hydrogen accumulation at the gate insulator interface.

The ability to prevent hydrogen incorporation using ALD-derived functional insulators was also studied using a passivation layer. Lee *et al* reported chemical hydrogen trapping using chemical bonding modulation in the $Al_2O_3$ grown by ALD using $H_2O$ and $O_3$ reactants [142]. The $Al_2O_3$ was used as a passivation layer in the bottom-gate top-contact structure. $V_{TH}$ negatively shifted more than −10 V after the $H_2O$-grown $Al_2O_3$ passivation layer was applied. This effect is related to the incorporation of −OH groups formed by the decomposition of the $H_2O$ reactant during the deposition process. In the device with an $O_3$-grown $Al_2O_3$ passivation layer, oxygen radicals filled the oxygen vacancies during passivation layer deposition, leading to a positive $V_{TH}$ shift of about 6 V. In addition, after hydrogen plasma treatment, the device with the $Al_2O_3$ deposited using the $H_2O$ reactant lost its switching properties, while the device with the $Al_2O_3$ grown by $O_3$ reactant showed no significant changes in electrical parameters. The cause of this effect was associated with the different chemical bonding states of carbon impurities, depending on reactant species. The main carbon bonding status of the $H_2O$ reactant-grown $Al_2O_3$ film was C–OH, whereas for the $O_3$ reactant-grown $Al_2O_3$ film it was C–O. For the $Al_2O_3$ film grown using $H_2O$ reactants, hydrogen atoms were subtracted from the C–OH bonds after the hydrogen plasma treatment, resulting in hydrogen molecules diffusing into the bottom active layer. However, when hydrogen was incorporated into $Al_2O_3$ films deposited using the $O_3$ reactant, it reacted with the C–O bond to form C–OH. A bi-layer $Al_2O_3$ consisting of $Al_2O_3$–$O_3$/$Al_2O_3$–$H_2O$ was applied as a passivation layer to ensure appropriate electrical characteristics in the device. Compared to the $O_3$-grown $Al_2O_3$ passivation layer,

the bi-layer $Al_2O_3$ showed improved SS and $\mu_{FE}$ values. In addition, the device with the bi-layer $Al_2O_3$ passivation layer showed a slightly negative $V_{TH}$ shift of 0.3 V, even with the hydrogen plasma treatment.

*2.4.2. Interface tailoring.* Device instability is mainly affected by the gate insulator/active layer interface because the activation energy of charge trapping at the interface is relatively low. Because the gate insulator is deposited on the active layer in the top-gate bottom-contact structure, the interface between the gate insulator/active layer is easily altered by changing gate insulator deposition conditions. Figure 6(b) shows how the electrical characteristics of the IZO top-gate bottom-contact TFTs varied with different plasma reactants ($O_2^*$ and $N_2O^*$) or plasma power during gate insulator deposition by plasma enhanced atomic layer deposition (PEALD) [63]. The $O_2$ plasma power was fixed at 100 W, while the $N_2O$ plasma power varied from 100 W to 200 W. The device with an $O_2$ plasma reactant gate insulator lost its switching characteristics, while the $N_2O$ plasma reactant produced the active semiconducting layer during gate insulator deposition. $V_{TH}$ positively shifted from $-12.39 \pm 0.02$ V to $-0.30 \pm 0.13$ V as $N_2O$ plasma power increased from 100 W to 200 W during the gate insulator deposition. This result means that periodic $N_2O$ plasma exposure can suppress carrier concentration in the active layer, and the degree of carrier concentration changes with plasma power. In addition, the devices showed comparable SS values at $N_2O$ plasma powers of 100 W and 150 W during the gate insulator deposition, while the 200 W plasma power resulted in SS degradation (100 W: $0.34 \pm 0.05$ V/decade, 150 W: $0.23 \pm 0.01$ V/decade, 200 W: $0.40 \pm 0.04$ V/decade). Because the SS is closely related to the interface trap density between the gate insulator and active layer, this result implies that the oxygen-related defects at the interface can be controlled via periodic $N_2O$ plasma exposure power. The devices were stressed at a gate voltage of $\pm 20$ V at a temperature of 60 °C to evaluate how variation in the interface trap density between the gate insulator and the active layer affected the PBTS/NBTS instability. There was an abnormal $V_{TH}$ shift under PBTS/NBTS instability for the device with an $N_2O$ plasma power of 100 W during the gate insulator deposition. The abnormal $V_{TH}$ shift behavior could be induced by further carrier injection from the mid and/or back channel into the front channel. However, a reasonable trend was observed in devices with $N_2O$ plasma powers of 150 W and 200 W, and the degree of $V_{TH}$ shift corresponds to the SS value. It is evident that device instability was easily affected by the interface trap density.

In addition to plasma power, plasma exposure time during gate insulator deposition by the PEALD process is a key factor controlling the interface between the gate insulator and active layer and the hydrogen content in the gate insulator. Cho *et al* reported the effects of $O_2$ plasma exposure time during gate insulator deposition on the electrical characteristics of an Al:ITZO top-gate bottom-contact TFTs [139]. The devices showed a positive $V_{TH}$ shift from $-6.38$ to 1.69 V and a decrease in mobility from 46.50 to 35.52 $cm^2\ V^{-1}\ s^{-1}$ as $O_2$ plasma time increased from 0.3 s to 4.0 s during gate insulator deposition. Furthermore, the hysteresis was negligible for $O_2$ plasma times of 0.3 s and 2.0 s, while it obviously increased at a plasma time of 4.0 s. Because the electron concentration is dependent on oxygen vacancies, this result implies that the oxygen vacancies decreased with increasing $O_2$ plasma time. However, at 4.0 s the excess $O_2$ plasma time degraded the interface quality between the gate insulator and active layer, leading to increased hysteresis voltage. The device stability dramatically changed with $O_2$ plasma time during the PEALD gate insulator deposition. The devices showed a U-shaped negative to positive $V_{TH}$ shift for PBTS time with increasing $O_2$ plasma time, bounded by the plasma exposure time of 2.0 s. The amount of hydrogen in the gate insulator increased with decreasing $O_2$ plasma time. Therefore, the negative $V_{TH}$ shift in the short $O_2$ plasma time originated from the hydrogen migration effect, from the gate insulator to the active layer, during the PBTS. The interface quality between the gate insulator and active layer degraded during the long $O_2$ plasma time during gate insulator deposition. PBTS instability is caused by the electron-trapping mechanism, and the interface between the gate insulator and active layer acts as an electron-trapping center. For this reason, a more positive $V_{TH}$ shift after PBTS instability with $O_2$ plasma time is associated with an increase in interface trap density.

## 3. Challenging issues in ALD-oxide semiconductor TFTs

Moore's law is a techno-economic concept that suggests it is possible to double the performance and capabilities of digital electronics approximately every 2 years, however the devices must be scaled down more and more to meet Moore's law [143]. The leap forward in device scale-down is achieved by minimizing device dimensions and high-density integration. The era of device dimensions beyond the 3 nm technology node has arrived. However, short-channel effects are an obstacle to further scaling device length dimensions with a high driving current. There are two ways to prevent short channel effects: (a) using a thinner channel and (b) modulating device structures with multiple channels in a limited space. These approaches are challenging in oxide-based TFTs because device performance generally rapidly decreases below a critical thickness, and advanced technology is necessary for 3D device structures. In addition to dimensional scale down, it will be necessary to realize oxide-based bi-polar devices (e.g., complementary metal–oxide–semiconductor (CMOS)) for high-density integration. However, this is not an easy task because of the lack of comparable p-type oxide semiconductor candidates for n-type TFTs. In this section, we describe how to overcome the challenging issues associated with oxide semiconductors.

### 3.1. Device scaling down

Figure 7(a) shows a schematic of a scaled-down device and the goals of the specifications. A decrease in active channel

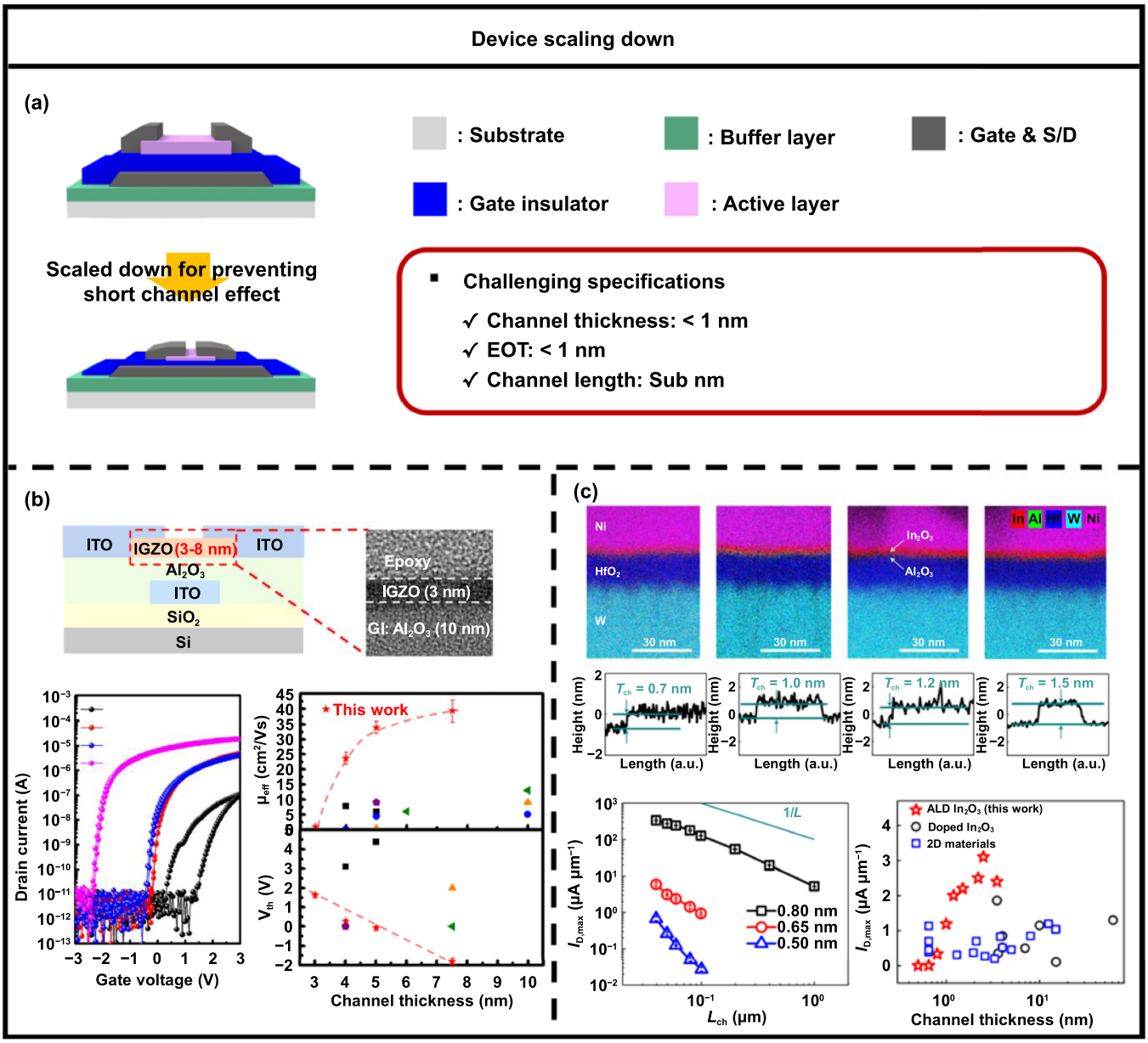


**Figure 7.** Challenging issues 1: device scaling down. (a) Schematic of the scaled device and challenging specifications. (b) TEM images of $Al_2O_3$/IGZO (10 nm/3 nm) stacked film, summary of key electrical parameters of IGZO TFT with channel thickness, and device performance degradation factors of ultra-thin IGZO TFT. (c) high angle annular dark field (HAADF) -scanning transmission electron microscopy (STEM) cross-sectional image with EDX elemental mapping, AFM measurements of $In_2O_3$ TFT, variations in on-current as a function of channel length and thickness, and comparison of on-current for $In_2O_3$ with other ultrathin semiconductors. Reprinted by permission from Springer Nature Customer Service Centre GmbH: Springer Nature, Nature Electronics [46], Copyright (2022).

layer thickness is challenging in oxide-based TFTs because the device performance degrades with channel thickness due to the decrease in the number of carriers. Many groups have investigated the limit of active layer thickness in oxide-based TFTs. The ALD process is essential for depositing ultra-thin films because the layer-by-layer self-limited growth mechanism provides smooth surfaces and film uniformity. Figure 7(b) presents a TEM image of the IGZO/$Al_2O_3$ interface region and summarizes the key electrical parameters of the IGZO TFTs, which varies from 3 to 7.5 nm [144]. As shown in the TEM image, there is a clear interface between the IGZO/$Al_2O_3$ layers, and sub-nanometer thickness can be controlled by the ALD process.

The carrier scattering and accumulation thickness are important factors determining electrical characteristics in the thin channel layer. First, carrier scattering in the bulk and interface alongside the constant carrier concentration can increase the interface trap density. In addition, the increased interface trap density results in inefficient charge response, and even Fermi level pinning eventually leads to degraded

SS in the 3 nm thick IGZO TFT. Second, the accumulation thickness, calculated using Gauss's law and Poisson's equation, was 6.4 nm in this experiment. Compared to the 7.5 nm thick IGZO TFT, the $\mu_{FE}$ was gradually degraded, decreasing the active layer thickness from 5 to 3 nm, because the channel could not fully form at the turn-on voltage.

As described, the performance of the 3 nm thick IGZO TFT degraded, while high $\mu_{FE}$ and on-current were required with the sub-1 nm active layer thickness. Si *et al* successfully fabricated sub-1 nm thick $In_2O_3$ TFTs with high on-current using ALD [46]. Figure 7(c) shows the properties of scaled ALD-$In_2O_3$ TFTs. The HAADF-STEM with EDX mapping images and AFM measurement of the $In_2O_3$ TFTs revealed that control of the sub-nanometer $In_2O_3$ thickness can be achieved using ALD. The maximum drain current ($I_{D,max}$) exponentially reduced the $In_2O_3$ thickness from 0.8 to 0.5 nm due to quantum confinement of the band structure of the $In_2O_3$ film. Although below 1 nm the on-state performances rapidly degraded, they had $I_{D,max}$ values comparable to state-of-the-art high-performance transistors with an ultrathin channel of 2D material and a doped $In_2O_3$ oxide semiconductor. In addition to the excellent electrical characteristics of the ultra-thin $In_2O_3$ TFTs, it is important to determine why $In_2O_3$ is able to make sub-1 nm thick atomic layer thin transistors. For this purpose, a charge neutrality level (CNL) and trap neutral level (TNL) model were applied to explain the properties of the ultra-thin $In_2O_3$ film [44]. The CNL in bulk $In_2O_3$ was located about 0.4 eV above the conduction band edge ($E_C$), and as a consequence the thick $In_2O_3$ behaves like a conducting oxide. For this reason, the Fermi level is pinned above $E_C$ for the metal/$In_2O_3$ contact, leading to low contact resistance. Similar to CNL, the TNL at the $In_2O_3$/dielectric interface also aligns above $E_C$ in the thick $In_2O_3$. However, the TNL in $In_2O_3$ moves deeply below $E_C$ for thicknesses less than 1 nm. The controlled CNL and TNL alignment in the ultra-thin $In_2O_3$ can be understood in terms of the quantum confinement effect, like layer-dependent band structures in 2D van der Waals materials.

Starting with the excellent electrical properties of the scaled ALD-$In_2O_3$ TFTs, the same groups reported a quantitative amount of defects, stability, and different active layer material. Wang *et al* showed high-quality scaled ALD-$In_2O_3$ by *C*–*V* measurement in a MOS capacitor [145]. The interface and bulk traps in the MOS capacitor were calculated by $G_p/\omega$ versus $\omega$ curves using T-CAD simulations of the *C*–*V* and *G*–*V* characteristics. The results indicated that high n-type doping concentration and subgap density of states attributed to the CNL alignment of the $In_2O_3$ material. Charnas *et al* have reported that $V_{TH}$ engineering via $O_2$ plasma treatment improved the stability of the $In_2O_3$ TFTs [146]. The treated device showed a positive $V_{TH}$ shift and improved P/NBS stability compared to the untreated device. In addition to the $In_2O_3$ material, Zhang *et al* reported an ITO active channel layer with a channel thickness of 2.1 nm [66]. Combining studies of experiments and simulation, the Sn concentration was determined to act as an obstacle to electron transport through the conducting $In_2O_3$ pathway. Therefore, having a proper Sn concentration is important because a high Sn concentration causes the degradation of device performance.

As described above, although extreme scaling of oxide semiconductors appears promising, further study is necessary to improve electrical characteristics and stability below the critical active layer thickness. In addition, contact resistance issues in the extremely scaled devices might be improved by proper methods, such as changing the S/D materials or employing a localized carrier doping process in the contact region of the active layer, to modulate the work function between the active layer and S/D electrode [19, 20, 147–149].

### 3.2. Device structure modulation

To suppress the short channel effects in a high-density device, the device architecture needs to be changed from planar to Fin-FET, GAA, CAA, or vertical structures, as shown in figure 8. Because these structures have a 3D channel, the conventional PVD process inevitably results in conformality and step coverage difficulties, and therefore an all-ALD process becomes necessary. As shown in figure 8(a), the Fin-FET is the preferred device structure beyond the 32 nm technology node because it offers better electrostatic control of the channel, compared to a planar structure [150]. However, to further scale the device, the GAA- (figure 8(b)) and CAA-FETs (figure 8(c)) are promising candidates to replace the Fin-FET because they offer better controllability of channels via a fully surrounding gate. The electrode etch process is an important factor for stable operation in the CAA-FETs. Chen *et al* have reported on the asymmetric characteristics of a CAA-IGZO FET. The CAA-IGZO FET was measured using a normal and reversed source/drain contact [30]. The normal source/drain contact has a great impact on device characteristics, such as the short channel effect and drain-induced barrier lowering. This is mainly caused by different etch processes for the source (bottom) and drain (top) electrodes, which does not affect a conventional planar structure.

Meanwhile, the vertical TFT has been actively investigated in an effort to reduce both short channel effects and the footprint of devices. As shown in figure 8(d), a vertical channel is formed at the sidewall of the spacer, and the spacer is especially important in the vertical TFT structure. The channel length can be defined by spacer thickness, which illustrates the ease of controlling the channel dimension without a special photolithography facility. However, the unavoidable poor roughness of the sidewall of the spacer or impurities due to the dry etch process during device fabrication, will degrade electrical characteristics. Lee *et al* have reported the electrical characteristics of vertical $In_2O_3$ TFTs while controlling the sidewall of the spacer [151]. To improve the electrical characteristics of the device, the sidewall of a spacer damaged by dry etching was coated with 3 nm thick $SiO_2$. In addition, a high-resolution photolithography system was adopted for the steeper taper angle. Compared to the reference device, using high-resolution photography the $SiO_2$-coated devices showed improved SS (0.25 $\rightarrow$ 0.12 V/decade) and $\mu_{sat}$ (13.87 $\rightarrow$ 23.69 $cm^2\ V^{-1}\ s^{-1}$), respectively.

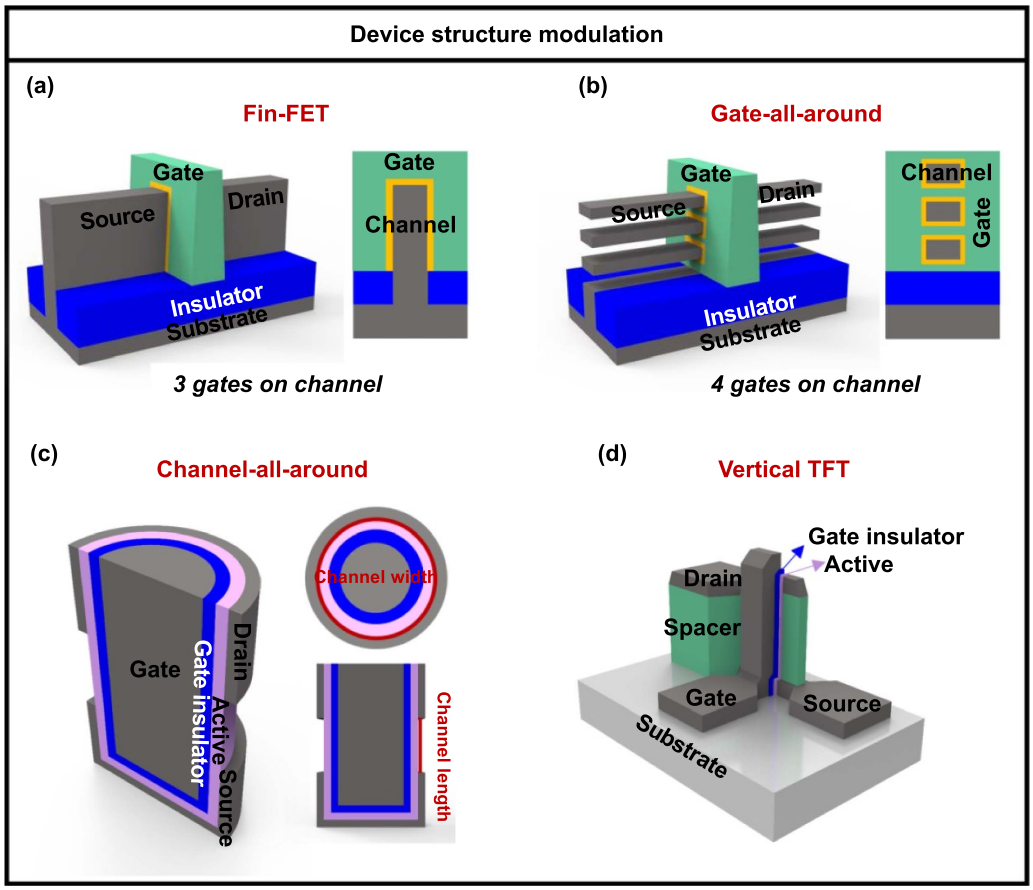


**Figure 8.** Challenging issues 2: device structure modulation. Schematic of (a) Fin-FET, (b) gate-all-around (GAA), (c) channel-all-around (CAA), and (d) vertical TFT.

As described above, the ALD-derived metal and insulator features are essential to the complex 3D structures of high-density devices, and the ALD process ensures excellent step coverage and conformality. The thin metal and insulator coatings can also passivate damaged films and contribute to improved contact resistance between the active layer and S/D electrode, and interface quality between the active layer and insulator.

### 3.3. P-type oxide semiconductors

While oxide semiconductors have been intensively studied and have reached maturity, the development of 'p-type' oxide semiconductors is far behind. This is because of the inherent issues in the band structure of oxide semiconductors themselves, which make it difficult to realize comparable p-type electrical performance. Tortuous conduction path is prepared for hole carrier in valence band maximum (VBM) by highly localized and anisotropic oxygen orbitals [153]. Also, problems with hole carrier generation through the metal vacancies leads to inferior hole transport behavior, such as low mobility and high off-current.

However, with the steady demand for low-power consumption and higher levels of integration, CMOS inverter fabrication is desirable over unipolar devices [154–157]. Subsequently, studies to overcome the poor electrical performance of p-type oxide semiconductor-based TFTs are still on-going. Tin, copper, and nickel-based oxides are promising p-type materials that could theoretically exhibit high Hall mobility due to the relatively low formation energy of metal vacancies, and delocalized VBM from orbital hybridization. Recently, ALD-based p-type oxide semiconductors have been reported by several academic groups. Accordingly, we will introduce representative studies in copper-based and tin-based oxide semiconductors, respectively.

Figure 9(a) is a report on the effects of post-processing on the $CuO_x$ phase and electrical performances, by Maeng *et al* [158]. From 200 °C to 500 °C, the oxidation state of Cu is transformed ($Cu_2O$ to CuO), and crystallinity is enhanced over 400 °C. This film transition influenced the TFT performance, as shown in figure 9(a). The optimized device was annealed at 300 °C and showed high mobility (5.64 $cm^2\ V^{-1}\ s^{-1}$) and an on/off ratio of $1.79 \times 10^5$. During the annealing process, non-stoichiometric defect states were largely compensated and improved electrical characteristics were observed. But, when the post-annealing process was increased to 400 °C, a phase transition occurred from $Cu_2O$ to CuO, which led to subsequent defect creation and deterioration of mobility. Kwon *et al* also reported ALD-based copper oxides for the phase-controlled deposition of $CuO_x$ ($0 \leqslant x < 1$) and improved TFT performance [152]. These authors studied how the phase transition depends on the number of Cu deposition steps, using a Cu

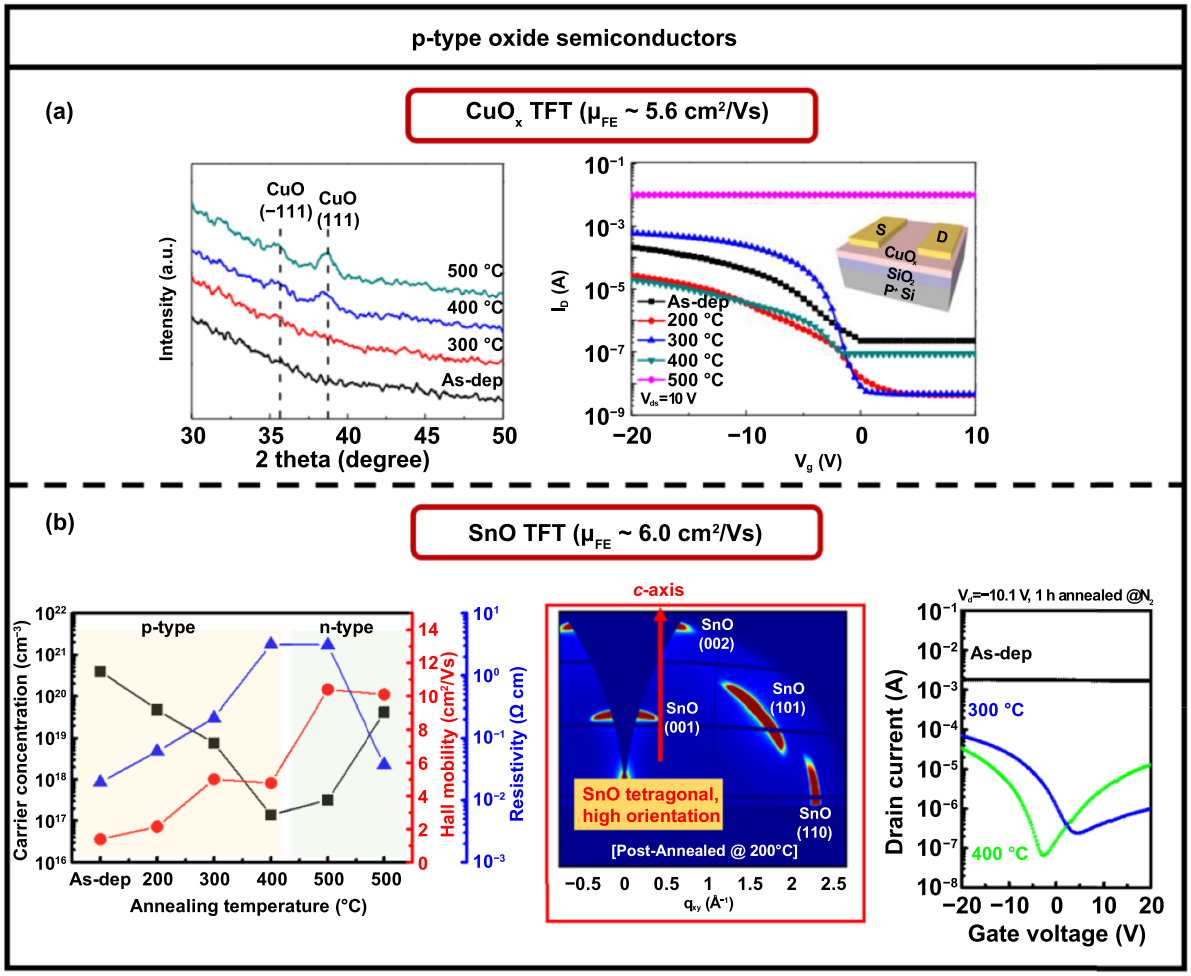


**Figure 9.** Representative studies of ALD fabricated p-type oxide semiconductors. Phase transition depends on the fabrication process and electrical characteristics. (a) ALD-$CuO_x$ TFT evaluation ($\mu_{FE} = 5.6$ cm$^2$ V s$^{-1}$). Reprinted from [158], Copyright (2016), with permission from Elsevier. (b) ALD-SnO TFT evaluation ($\mu_{FE} = 6.0$ cm$^2$ V s$^{-1}$).

precursor and $H_2$ plasma, with fixed oxidation cycles using ozone. With an increasing number of Cu deposition steps in 1 super-cycle, the fabricated $CuO_x$ film exhibited a transition from CuO ($CuO_{0.9}$) to $Cu_2O$ ($CuO_{0.6}$). This controlled cupric oxide phase exhibited highly varied film properties and electrical performances.

Napari *et al* demonstrated the importance of an $Al_2O_3$ passivation layer on a $Cu_2O$ TFT [159]. After fabrication of the ALD deposited polycrystalline $Cu_2O$ channel based TFT with $Al_2O_3$ passivation, $\mu_{FE}$ was still low but switching performances such as on/off ratio were greatly enhanced (30–5000). XPS and TEM analysis showed that a reduction in the $CuO_x$ back-channel region occurred and a 1–2 nm $CuAlO_2$ layer was formed. Also, the high negative fixed charge density of the $Al_2O_3$ layer could relieve the electrons in the $Cu_2O$ channel. Those two effects directly influenced TFT performance and resulted in improved performances.

In tin-based oxide semiconductors, the phase transition is critical to device performance. SnO is a promising p-type material, while $SnO_2$ is a super-conductive n-type material. Figure 9(b) shows a study of the two-step crystallization of SnO and the interrelation between phase-control and the electrical performance of SnO-TFTs by Kim *et al* [160]. Highly *c*-axis aligned SnO was fabricated under optimized conditions by screening the growth temperature during ALD and the post-annealing process (100 °C and 300 °C, respectively). Densification occurred in as-deposited to 300 °C annealed films, and the following release of defects led to a high mobility (6.0 cm$^2$ V$^{-1}$ s$^{-1}$) and stability of the TFT. At an annealing temperature of over 400 °C, a phase transition from SnO to $SnO_2$ was revealed, and identical SnO-based TFTs exhibited ambipolar characteristics. This study indicates that controlled ALD process conditions, and high density and *c*-axis oriented SnO films, could be achieved, which are valuable results in the field of p-type oxide semiconductors. Improved electrical performance by defect engineering was reported by Kim *et al* [161]. SnO grown by ALD exhibited enhanced switching performances when growth temperature was optimized to 210 °C. SnO crystallinity largely increased with the increase in growth temperature (150 °C–210 °C). A post annealing process (250 °C) and $Al_2O_3$ passivation process led to enhanced defect density and carrier concentration near the back-channel

region and resulted in a very high on/off ratio ($2 \times 10^6$) and subthreshold swing (1.8 V/decade).

Interface engineering is also effective approach for p-type oxide semiconductors. Jang *et al* reported that ALD deposited SnO TFT with an $Al_2O_3$ interface layer improved hysteresis from 4 V to 0.2 V [162]. This optimized hysteresis was extracted from an inverted staggered TFT with a 15 nm $Al_2O_3$ interfacial layer between the SnO channel and $SiO_2$ gate insulator. Time-of-flight secondary ion mass spectrometry (TOF-SIMS) and DFT calculations revealed that the $Al_2O_3$ could successfully block Sn diffusion into $SiO_2$ which caused the degraded hysteresis in the original TFT, by the creation of substitutional defects ($Sn_{si}$). Although the field of p-type oxide semiconductors is still developing, those studies illustrate the future possibilities.

## 4. Outlook

Oxide semiconductors have received tremendous attention since the report of a-IGZO. Oxide semiconductors are currently being used in mass production by PVD deposition, because they provide multiple, advantages, including high electrical properties, large-area uniformity, and low process temperature. Furthermore, Si-based non-display fields have almost reached the limit of scaling down, and oxide semiconductors with very low off-currents are attracting more attention as a new material to break through this barrier. Their application in these non-display fields, and their ability to increase resolution in displays, require the deposition of oxide semiconductors with 3D structures and higher electrical properties. Therefore, beyond the conventional PVD deposition method, an ALD deposition method is emerging which provides advantages such as uniform 3D structures, thickness control at the nanometer-scale, the control of fine composition, and high-quality films with high electrical performance.

ALD based oxide semiconductors have attracted attention as active materials for TFTs, and the number of such studies has dramatically increased recently. In this review, the authors have explained the historical background of suggested the value of ALD for the development and application of oxide semiconductors, as follows.

- *In-situ* composition control in vertical distribution: ALD enables the development of various oxide semiconductors through (a) composition control for multi-component oxide semiconductors and (b) gradient distribution of cation composition through cycle design. The metal cations constituting the multi-component oxide semiconductor can each play different roles (as carrier suppressors, carrier generators, and structure stabilizers), and their electrical properties are controlled by their distribution.
- Vertical structure engineering: ALD is very suitable for designing vertical-channel structures with enhanced interface characteristics, because it enables nano-scale control and *in-situ* processing for dissimilar material deposition. Based on the ALD sequence, superlattice formation is possible, using nano-laminates of semiconductors and insulator, and dual channel modulation is possible by forming heterogeneous junctions between oxide semiconductors of different compositions.
- Chemical reaction and film properties: Since the ALD method is based on a self-limiting chemical reaction, the precursor and reactant inevitably affect the characteristics of the thin film. Therefore, in ALD, it is important to select an appropriate precursor and a reactant, and different properties can be realized even with the same material.
- Insulator and interface engineering: The interface between a semiconductor and insulator is closely correlated with electrical characteristics and reliability in oxide semiconductor based TFTs. ALD is an optimal process for improving the film quality of the interface between insulators and semiconductors and controlling the diffusion of impurities, such as hydrogen and carbon, in insulators. Furthermore, studies on the application of functional insulators and interface tailoring processes based on ALD are actively in progress.

Challenging issues remain that prevent the expansion of oxide semiconductors and their use in metaverse AR/VR, DRAM, 3D-NAND and logic. Recent studies have indicated that ALD is a valuable method for future applications in industry, as it provides exquisite control of thickness, stoichiometry, and phase. The scaling down of devices requires thinner active materials, down to sub-nanometer thicknesses. ALD-based indium oxide can be used to drive device thickness down to 1 nm, and it will be necessary to further research this method as an ultra-thin active layer for scaling down. The fabrication of 3D-structured devices such as GAA-TFT, CAA-TFT, and V-TFT is challenging, but will broaden the industrial applications of ALD oxide-semiconductors. When applied as an active layer in a 3D structure, they can increase the degree of integration, and monolithic 3D integration, by stacking TFTs in the vertical direction. Also, achieving non-comparable paired p-type oxide semiconductors is another task for the scalability of oxide semiconductors, which are basically n-type characteristics in CMOS inverters. The commercialization of ALD-oxide semiconductors is still on-going. We believe that the suggested benefits of ALD for oxide semiconductors will motivate efforts to address the remaining challenges in 3D-structured, very thin devices, CMOS inverters, and future applications.

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