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ABSTRACT

We investigate the low-frequency noise characteristics of indium–gallium–zinc oxide ferroelectric thin-film transistors (FeTFTs) with a metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structure. MFMIS FeTFTs are fabricated with different metal-to-FE area ratios (A_M/A_F's). It is revealed that the noise generation mechanism differs depending on the operation region [low and high drain current (I_D) regions] and A_M/A_F. Excess noise in the low I_D region is observed in the MFMIS FeTFTs with A_M/A_F's of 4 and 6 due to carrier mobility fluctuations. In the high I_D region, the carrier number fluctuation generates the $1/f$ noise of the devices regardless of the A_M/A_F.

Electronic integrated circuits (ICs) have advanced their performance through the continuous dimensional scaling of transistors. Following Moore's law, complementary metal–oxide–semiconductor technology doubles the number of transistors in logic and memory circuits every 2 years.[1,2] With the emergence of the Internet of Things, the functional requirements of ICs have expanded to a wider range of applications, such as biomedical electronics, sensor technology, communication, neuromorphic computing, and quantum computing. Accordingly, the paradigm in the semiconductor business is shifting from "more Moore" to "more than Moore."[3–5]

In the emerging more than Moore applications, ferroelectric thin-film transistors (FeTFTs) are gaining significant technological attention owing to their fast switching speed, low voltage operation, and low fabrication temperature.[6–10] FeTFTs have exhibited excellent performance as chemical sensor platforms[6] and artificial synapses in neuromorphic computing.[7,9] Accordingly, extensive efforts have been made to improve the FeTFTs performance. From a material engineering perspective, various thermal or plasma treatments have been proposed to improve the ferroelectricity in FeTFTs.[11,12] From a structural perspective, various stack structures have been proposed. The most widely used stack is the metal–ferroelectric–insulator–semiconductor (MFIS) structure. However, it suffers from poor reliability and endurance due to the thermal budget and excessive field applied to the FE–insulator interface.[13] To circumvent these problems, a metal–FE–metal–insulator–semiconductor (MFMIS) structure has been proposed.[14,15] In the MFMIS stack, the capacitance ratio between the MFM and MIS could be controlled by changing the metal-to-FE area ratio (A_M/A_F). Thus, low-power operations and improvements in the reliability and endurance can be achieved.

Low-frequency noise (LFN) plays a vital role when MFMIS FeTFTs are integrated for the purpose of diverse applications. The LFN determines the noise level of the signal in sensor applications and, thus, defines the lowest detectable signal.[16,17] In neuromorphic computing, $1/f$ noise and random telegraph noise significantly affect the learning accuracy of neural networks.[18–20] Therefore, it is crucial to understand the LFN characteristics of the MFMIS FeTFTs.

In particular, the effects of phonon scattering caused by polarization on the LFN characteristics should be demonstrated. However, despite their relevance and significance, none of these features are investigated in MFMIS FeTFTs.

In this Letter, based on the above discussion, we fabricate MFMIS FeTFTs with hafnium zirconium oxide (HZO) as an FE layer and indium–gallium–zinc oxide (IGZO) as a conductive channel. Subsequently, the LFN characteristics of the fabricated FeTFTs are investigated. The power spectral densities (PSDs) of FeTFTs with different A_M/A_F's are measured under various bias conditions. The noise-generation mechanisms in each device are demonstrated through a rigorous analysis.

Figures 1(a) and 1(b) show the schematic cross section of the fabricated MFMIS FeTFTs and the corresponding transmission electron microscopy (TEM) image, respectively. The FeTFTs were fabricated on a buffer oxide (SiO_2, 300 nm). A 35 nm of Mo is deposited as a bottom gate (BG) via DC sputtering process and patterned by dry etching. Subsequently, the FE layer (HZO, 7.5 nm) and a floating gate (FG, TiN, 25 nm) were deposited by thermal atomic layer deposition (ALD) and plasma-enhanced ALD, respectively. Thermal annealing was then performed at 500 °C for 30 s under N_2 ambient conditions to induce ferroelectricity in HZO. A dielectric layer (ZrO_2, 8 nm) was deposited by thermal ALD. Amorphous IGZO was deposited via radio frequency sputtering as a conductive channel and then patterned by wet etching with a diluted HCl solution. Mo was deposited as the source and drain by DC sputtering and etched using an SC-1 solution. Finally, the FeTFTs are annealed at 350 °C for 1 h under O_2 ambient conditions to stabilize the IGZO channel. The channel width (W)/length (L) of the device used in this study is 20/20 μm. Note that the A_M (area of TiN gate) is fixed, and the A_F (area of HZO) is modulated by changing the bottom gate area. As shown in Fig. 1(c), the ferroelectricity of HZO is investigated using positive-up-negative-down (PUND) measurements in the MFM stack with a frequency (f) of 100 kHz. Figure 1(d) shows the polarization vs voltage of the HZO, exhibiting a remnant polarization of 21.1 μC/cm^2. For electrical and LFN measurements, a semiconductor device parameter analyzer (Agilent, B1500A), a low-noise current preamplifier (Stanford Research System, SR560), and a dynamic signal analyzer (Keysight, 35670A) were used.

Figure 2(a) shows the double-sweep transfer characteristics (I_D–V_{BG}) of the fabricated FeTFTs with different A_M/A_F's. The bottom gate bias (V_{BG}) is swept from –4.5 to 4.5 V at a fixed drain-to-source bias (V_{DS}) of 0.1 V. In all the cases, the devices exhibit anticlockwise hysteresis originating from the polarization of HZO. With an increase in A_M/A_F from 2 to 6, the memory window at 10 nA is increased from 0.34 to 2.05 V. This is because a higher voltage is applied to HZO with an increase in A_M/A_F.

Figure 2(b) shows the drain current (I_D) PSD (S_{ID}) vs f of the FeTFTs with different A_M/A_F's. The PSD is measured at the erase state [high threshold voltage (V_{th}) state] to avoid the V_{th} shift during the PSD measurement. The V_{BG} is changed to generate the I_D that ranges from 10 nA to 1 μA in each device. Note that the two orders of the current range are enough to verify the noise source of the devices. In this study, the PSD is measured in the f range of 10 and 1.60×10^3 Hz. It took a total of 20 s to obtain the PSD in each bias condition. The PSD result shown is the average of 200 times PSD measurements, with one PSD measured for 0.1 s. In the measured f ranges, the devices exhibit $1/f^{\gamma}$ noise behavior ($\gamma = -\ln S_{ID}/\ln f$). It has been reported that the $1/f$ noise in TFTs originates from the random fluctuation of the carrier number owing to the trapping/de-trapping process to/from the defects inside the gate oxide. Such behavior can be explained by the carrier number fluctuation (CNF) model. The CNF model is expressed as follows:[21]

$$\frac{S_{ID}}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 \frac{q^2 k_B T N_T \lambda}{W L C_{ox}{}^2 f}, \tag{1}$$

where g_m is the transconductance, q is the electron charge, k_B is the Boltzmann constant, T is the temperature, N_T is the volume trap density, λ is the tunneling attenuation coefficient, and C_{ox} is the gate oxide capacitance per unit area. To verify the explanation of the LFN characteristics of the FeTFTs by the CNF model, the PSD is measured at various V_{BG}s. Figures 3(a)–3(c) show the I_D normalized PSD ($S_{ID}/I_D{}^2$) of

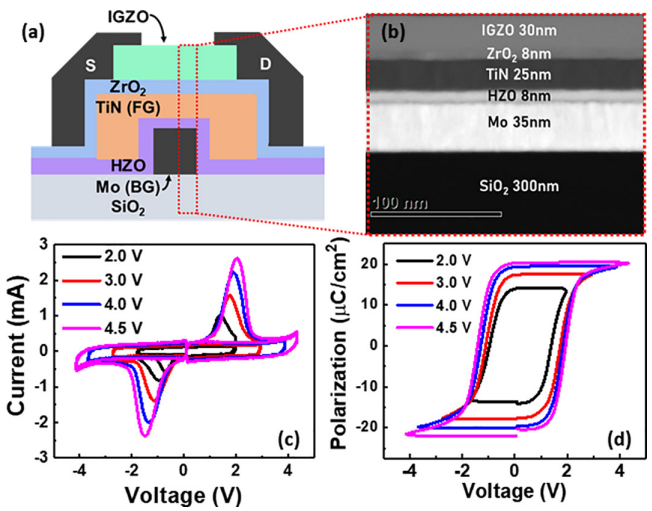

FIG. 1. (a) Schematic cross section of MFMIS FeTFT. (b) TEM image of the gate stack. (c) Current vs voltage curves in PUND measurement at different bias conditions. (d) Polarization vs voltage curves at different bias conditions.

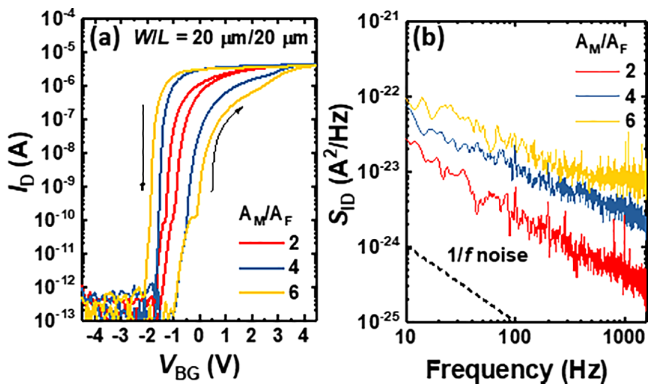

FIG. 2. (a) I_D–V_{BG} of the FeTFTs with A_M/A_F's of 2, 4, and 6. (b) S_{ID} vs f of the FeTFTs with A_M/A_F's of 2, 4, and 6. The PSD of the FeTFTs with A_M/A_F's of 2, 4, and 6 is measured at I_D of 20.3, 18.7, and 24.1 nA, respectively.

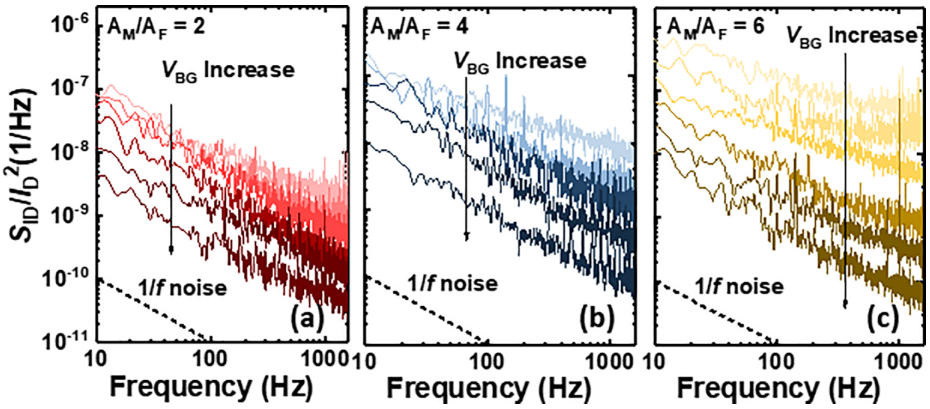

FIG. 3. S_{ID}/I_D^2 and $(g_m/I_D)2$ vs frequency of the FeTFTs with A_M/A_F's of (a) 2, (b) 4, and (c) 6, respectively. V_{DS} is fixed at 0.1 V, and V_{BG} is changed to generate the I_Ds ranging from 20 nA to 1 μA.

the FeTFTs with A_M/A_F of 2, 4, and 6. Note that V_{DS} is fixed at 0.1 V, and V_{BG} is changed to generate I_Ds ranging from 20 nA to 1 μA.

It is necessary to investigate the correlation between S_{ID}/I_D^2 and $(g_m/I_D)^2$ to verify the origin of 1/*f* noise. Figures 4(a)–4(c) show S_{ID}/I_D^2 sampled at 10 Hz and $(g_m/I_D)^2$ vs I_D of the FeTFTs with A_M/A_F's of 2, 4, and 6, respectively. Note that the different values of the constant are multiplied by $(g_m/I_D)^2$ in each device for fitting. In the case of the FeTFT with an A_M/A_F of 2, S_{ID}/I_D^2 and $(g_m/I_D)^2$ exhibit the same tendency as I_D in all operating regions, demonstrating that the 1/*f* noise of the device stems from the CNF. However, in FeTFTs with A_M/A_F's of 4 and 6, the deviation of S_{ID}/I_D^2 to $(g_m/I_D)^2$ is observed in the low I_D region, as indicated by the ellipses in Figs. 4(b) and 4(c). Note that the five devices for each case are measured and the results were reproducible. The deviation of S_{ID}/I_D^2 and $(g_m/I_D)2$ could be explained by the correlated mobility fluctuation (CMF) model by

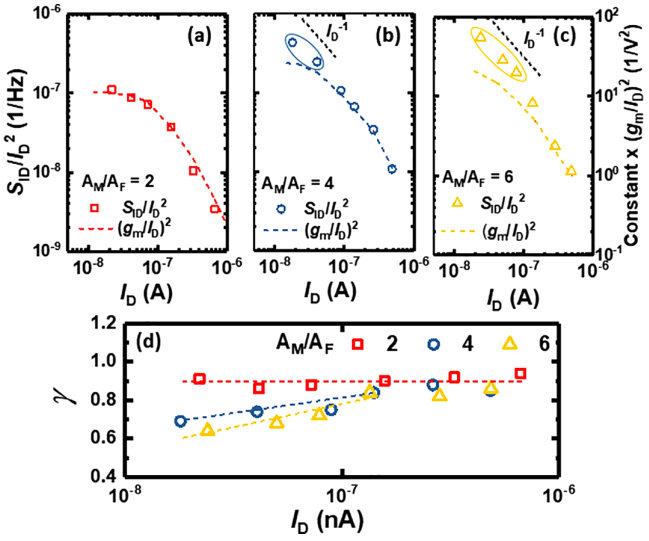

FIG. 4. S_{ID}/I_D^2 sampled at 10 Hz and $(g_m/I_D)2$ vs I_D of the FeTFTs with A_M/A_F's of (a) 2, (b) 4, and (c) 6, respectively. The deviation of S_{ID}/I_D^2 to $(g_m/I_D)2$ is noted by the ellipses in Figs. 4(b) and 4(c). (d) γ vs I_D of the FeTFTs with A_M/A_F's of 2, 4, and 6.

multiplying $(1 \pm \alpha\mu_{eff} C_{ox} \frac{I_D}{g_m})^2$ to Eq. (1), where α is the scattering parameter that reflects how a variation in the oxide charge couples to the mobility and μ_{eff} is the effective mobility.[21] According to the CMF model, the trapped carriers at the defects in gate oxide additionally fluctuate the carrier mobility through the Coulombic force. However, the CMF model cannot be used to explain the LFN characteristics of the devices. Because the CMF term is proportional to I_D/g_m, the model can account for the deviation of S_{ID}/I_D^2 and $(g_m/I_D)^2$ in the high I_D region. However, as shown in Figs. 4(b) and 4(c), the deviation is observed in the low I_D region.

In IGZO TFTs, 1/*f* noise is not only attributed to the CNF at the gate oxide-conductive channel interface but also to the bulk carrier mobility fluctuation (BMF) in the IGZO channel.[22,23] When the TFT operates in the low I_D region and a conductive channel is formed broadly across the channel, bulk conduction plays a significant role.[23] In particular, the remote phonon scattering should be considered when the charge density in the conductive channel is low.[24] When HZO is polarized, the carrier mobility at the bulk of conductive channel fluctuates significantly owing to the remote phonon scattering. This is because the soft bonds in polarized FE materials, related to low-energy optical phonons, fluctuate carrier mobility.[25] When the BMF is dominant, S_{ID}/I_D^2 is expressed as follows:[17]

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H \mu_{eff} 2kT}{fL^2 I}, \tag{2}$$

where α_H is Hooge's parameter that represents the magnitude of mobility scattering. According to (2), the S_{ID}/I_D^2 decreases with a power of −1 in the log–log plot of S_{ID}/I_D^2 vs I_D, which is the case in the FeTFTs with A_M/A_F's of 4 and 6 operating in the low I_D regions [Figs. 4(b) and 4(c)]. The polarization of HZO in the FeTFT increases with A_M/A_F, which can be confirmed by the increase in the memory window of FeTFTs [Fig. 2(a)]. Thus, a greater mobility fluctuation is induced in the low I_D region in the cases of the FeTFTs with larger A_M/A_F's, increasing the 1/*f* noise. However, as the I_D increases, the number of electrons at the IGZO channel increases, screening the remote phonon scattering.[24] This is why the noise generation mechanism is changed from BMF to CNF with an increase in I_D, even in the FeTFTs with larger A_M/A_F's.

One might speculate that the remote phonon scattering would be screened by the FG (TiN), and thus, the impact of remote phonon

scattering in the devices should be insignificant. However, recent studies reported that the phonon scattering could be enhanced by the presence of a metal gate.[24] The boundary condition for electric potential at the channel–barrier interface can characterize the effect of the gate and the oxide on the channel. In this instance, the effects of the metal gate on the phonon scattering at a distance can be explained as follows: Scattering of electrons in the channel is caused by vibrational modes of the dielectric involving ionic displacements that generate large oscillating electric dipole fields. When a metal is present behind a thin dielectric, electrons respond quickly to the electric field generated by vibration. This generates a new field coming from image charges with the opposite sign. The modes whose dynamic dipole moments are aligned along the surface normal, which is the case for the device in this study, generate identical image dipoles, i.e., the total dipole moments are doubled, increasing scattering and thus reducing mobility.[24,26]

The transition of the dominant noise source from carrier mobility fluctuation to CNF can be further confirmed by the different behavior of γ in relation to I_D. Figure 4(d) shows the γ vs I_D of the FeTFTs with A_M/A_F's of 2, 4, and 6. The γ of the FeTFT with A_M/A_F of 2 has the same value regardless of the change in I_D. However, the γ value of the FeTFTs with A_M/A_F's of 4 and 6 changes with respect to I_D. In the low I_D region, the γ value is much smaller than one. This is because the scattering rate of mobility fluctuation is more significant at the higher frequency.[27] However, as the dominant noise generation mechanism is changed to CNF with an increase in I_D, the γ value increases and approaches that of the FeFET with A_M/A_F of 2.

In this study, we fabricated IGZO FeTFTs with an MFMIS structure and investigated the LFN characteristics of the devices with different A_M/A_F's. It was shown that the noise generation mechanisms differ depending on the A_M/A_F and I_D regions. In the low I_D regions, excess noise generated by the polarized HZO is observed in the FeTFTs with larger A_M/A_F's owing to the increased mobility fluctuation caused by remote phonon scattering. In the high I_D regions, $1/f$ noise is generated from the CNF regardless of the A_M/A_F. Considering that the ferroelectric TFTs with IGZO channels are seen as promising for new technologies in the future computing paradigm, understanding the LFN characteristics of this emerging devices should be crucial for its practical implementation.[28–32] We believe that the results in this study based on their extensive understanding of electronics and applied physics paves the way for the further development for ferroelectric-based TFTs.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

W. Shin and E. C. Park contributed equally to this work. **Wonjun Shin:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Writing – original draft (equal). **Eun Chan Park:** Conceptualization (equal); Formal analysis (equal); Methodology (lead). **Ryun-Han Koo:** Data curation (equal). **Dongseok Kwon:** Investigation (equal). **Daewoong Kwon:** Formal analysis (equal); Funding acquisition (equal); Supervision (equal). **Jong-Ho Lee:** Resources (equal); Supervision (equal); Writing – original draft (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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