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A Two-Way Wideband Active SiGe BiCMOS Power Divider/Combiner for Reconfigurable Phased Arrays With Controllable Beam Width

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ABSTRACT This paper proposes a reconfigurable two-way wideband active power divider/combiner based on bi-directional amplifier and absorptive series-shunt switch techniques. A multi-octave operational bandwidth and flat gain response with bi-directional operation are simultaneously achieved using bi-directional distributed amplifiers (BDAs). The reconfigurable functionality and fast mode selection are obtained by using the absorptive series-shunt switches. The proposed power divider/combiner provides four different operational states depending on the control inputs for the BDAs and the series-shunt switches. The dual-path mode supports both divider and combiner operations, and the measured gain is greater than 7.8 dB and the isolation between output ports is better than 23 dB over the 3-dB bandwidth of 2-23 GHz. The measured noise figure (NF) of the dual-path mode is below 10 dB, while maximum amplitude and phase imbalances are 0.2 dB and 1.8 degrees, respectively. The single-path mode shows a measured gain of $>$ 7.8 dB, and a port-to-port isolation $>$ 35 dB. The measured NF is below 12 dB from 8 to 26 GHz. In addition, the proposed circuit shows the maximum output 1-dB compression point (OP1dB) of 4.6 dBm, and good matching characteristics, with a DC power consumption of 120 mW. The chip area of the reconfigurable two-way SiGe bi-directional active power divider/combiner is 1.43 mm $\times$ 0.92 mm.

INDEX TERMS Active power divider/combiner, bi-directional amplifier (BDA), octave bandwidth, phased array antenna, reconfigurable, SiGe, SiGe BiCMOS, wideband.

I. INTRODUCTION

Wideband reconfigurable power dividers and combiners are key components in a variety of applications, including high-efficiency power amplifiers, switched multi-beam systems, and reconfigurable phased array antennas [1]–[4]. In large-scale wideband reconfigurable phased array antennas, power dividing and combining functions are required to: 1) distribute power to each transmit/receive (T/R) module for beam forming, or 2) add up the incoming signal from each antenna for subsequent signal processing. In addition, low phase/amplitude imbalances during the power dividing and combining are important requirements for simplifying complex phase/amplitude calibrations and reducing tracking errors. Furthermore, since the physical distance between the antennas is determined by the operating frequency, the beam width and effective radiated power (ERP) in conventional wideband phased array antennas exhibit different characteristics depending on the required frequency range, as shown in Fig. 1 (a). Therefore, recent high-level and large-scale wideband phased array systems require that arrays need to be instantly reconfigured for the optimizing functionality and tuning of other parameters such as ERP and beam-shaping. To realize these requirements, reconfigurable active power dividers and combiners can be a practical solution. By selectively turning 'on' or 'off' the antenna array elements for a given operating frequency, the beam width and the ERP can remain constant over a wide operational frequency. In addition, they should provide positive and flat gain response, which helps reduce the total system complexity by

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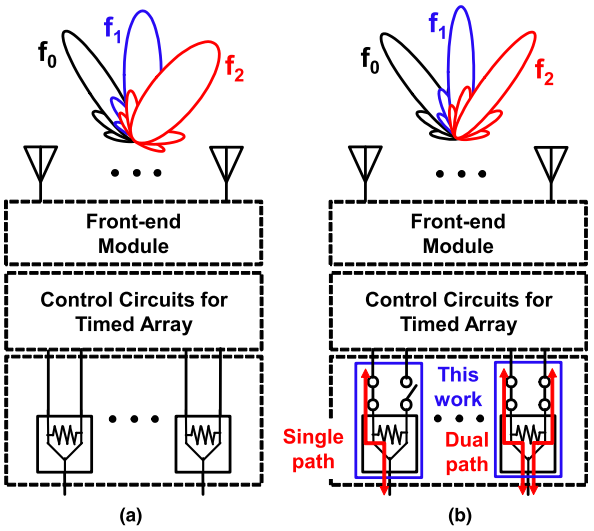

FIGURE 1. (a) The conventional multi-channel wideband phased array antennas. (b) The reconfigurable wideband phased array antennas with the proposed two-way reconfigurable power divider/combiner circuits.

eliminating additional equalizers and loss compensation amplifiers. Considering the high level of integration, the need to support bi-directional operation, wide bandwidth, and compact chip size are all important concerns. Reconfigurable wideband phased array antennas [5], [6] using active power divider/combiner circuits are shown in Fig. 1 (b). The advantage of this system includes scalability, wide bandwidth, bi-directional operation, and reconfigurable functionality.

To address the reconfigurable functionalities with power dividing and combining operations, both passive and active-based power dividers and combiners have been proposed in the literature [7]–[17]. The passive-based reconfigurable power dividers and combiners successfully provide multi-path modes using couplers, capacitors, and single-pole double-throw (SPDT) switches [7]–[11]. In addition, they have the benefits of zero power consumption, high linearity, and proper port-to-port isolation. However, they suffer from fundamental limitations such as narrow bandwidth, high insertion loss, and large chip size due to quarter-wave transformers and a large number of passive switches. Therefore, they may not be suitable for large scale wideband reconfigurable phased array antennas. From a system perspective, the additional amplifiers require for the compensation of insertion loss associated with the passive-based power dividers and combiners increase the total system complexity and chip size.

To overcome the drawbacks of passive-based designs, active-based wideband power divider/combiner circuits have been demonstrated [12]–[16]. A distributed amplifier (DA) and an interleave techniques have been proposed for active power dividers and combiners [12]–[14]. Since they support uni-directional operation only, however, designers should place the same circuit for every transmitter and receiver in the signal paths. As a result, the overall system requires lager chip area and complex digital circuitry. The BDA technique has been introduced to provide bi-directional capability and wide operational bandwidth [15], [16]. However, these previous designs are not suitable for beam-shaping and ERP control in reconfigurable wideband phased array antennas, since they cannot provide reconfigurable functionality. The wideband reconfigurable active divider/combiner circuit using the DA technique has been designed [6]. Since they used GaAs platform, however, it is hard to integrate digital control circuits within a single chip, which led to an increase in system complexity, size, and manufacturing cost.

In the present paper, we propose a two-way reconfigurable active power divider/combiner in order to overcome the limitations associated with the previous active- and passive-based designs. The proposed two-way reconfigurable wideband power divider/combiner supports three different operation modes: dual-path, single-path and full OFF modes as shown in Fig. 1 (b). In addition, it can provide high speed mode selection by the series-shunt switches. In Section II, we describe the design of the BDA structure. Section III provides the configuration and the optimization of the proposed power divider and combiner with BDAs and series-shunt switches. The measured results are presented in Section IV. Finally, we will summarize the paper in Section V.

II. DESIGN OF BDA STRUCTURE

While the BDA core structure was previously discussed in [18], [19], to illustrate the operation and the key points, a brief description is included here.

The schematic of the BDA core structure is shown in Fig. 2 (a), where the BDA core is composed of two cascode pairs (Q_1/Q_2 and Q_3/Q_4) for bi-directional operation [18], [19]. The base terminal of Q_1 is connected to the collector terminal of Q_3 through C_1, and Q_2 and Q_4 have the same connection for the opposite direction. For the forward

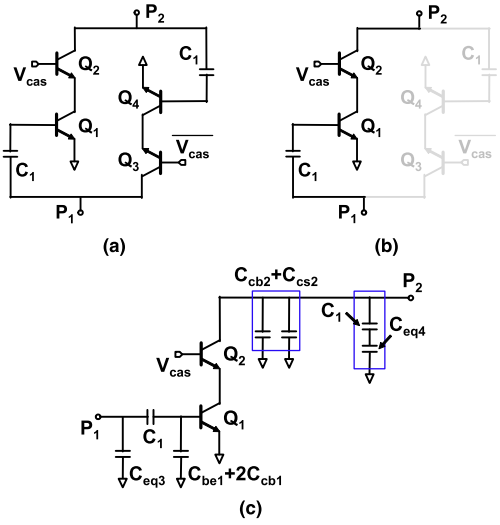

FIGURE 2. (a) Schematic of the BDA core. (b) Simplified circuit schematic of BDA for the P_1-to-P_2 mode (forward operation). (c) Simplified equivalent circuit of the forward operation.

operation from P_1 to P_2, the base terminals of Q_2 and Q_3 are ON and OFF, respectively [Fig. 2 (b)] and the BDA core becomes a single cascode structure that has benefits of wide bandwidth and good reverse isolation by minimizing the Miller effect. The series capacitor, C_1 is used in the BDA core for two main purposes. First, it provides a DC open between the base terminal of Q_1 and Q_4 and the collector terminals of Q_2 and Q_3. Based on the proposed BDA circuit configuration, V_{cas}, can be used as a control signal in order to achieve high-speed mode selection for the forward and the backward operations compared to [17]. Second, by adjusting the C_1 capacitance, the optimum total capacitance at input and output nodes of the BDA core can be obtained. Therefore, the capacitance value of C_1 should be carefully selected to satisfy the system requirements. In addition, since the device size is related to power handling (linearity) capability, operational bandwidth, and power gain, the device size should also be chosen based on the specifications of the system.

The simplified equivalent circuit in the forward operation mode is shown in Fig. 2 (c). The total capacitance at the input (P_1) and the output (P_2) nodes can be calculated as in [19]. In the present design, all transistors have the same size of 0.12 μm $\times$ 8.0 μm and C_1 has the capacitance of 123.8 fF for wideband operational bandwidth and moderate power gain. The total capacitances of forward operation are 88.7 and 71.8 fF for the input and the output nodes, respectively. The total capacitances for backward operation can be calculated similarly. We will discuss operational bandwidth and power gain of the proposed reconfigurable two-way SiGe active power divider and combiner in Section III more in detail.

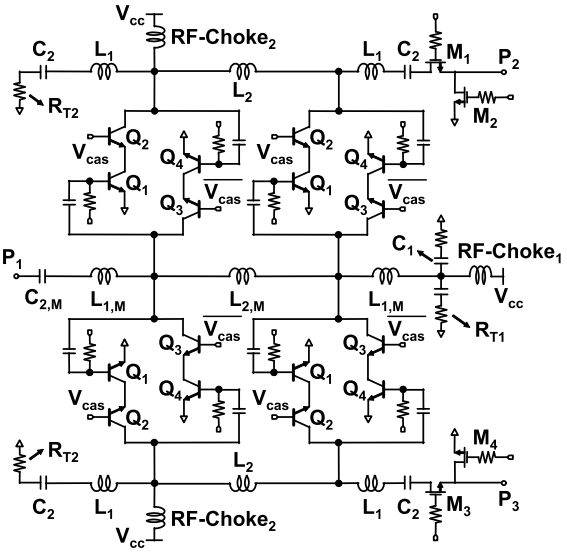

FIGURE 3. Schematic of the proposed reconfigurable two-way wideband active power divider/combiner with BDA cores and series-shunt switches.

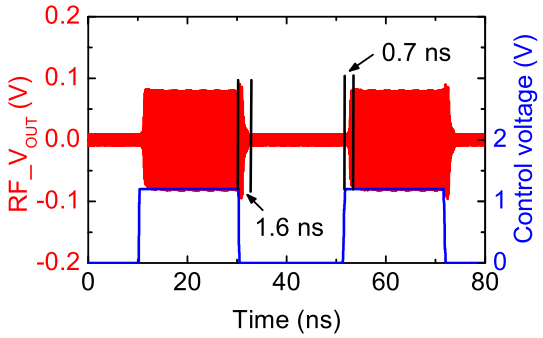

FIGURE 4. Simulated mode transition using the series-shunt switch control at 10 GHz under the −20 dBm input power.

III. PROPOSED RECONFIGURABLE TWO-WAY ACTIVE POWER DIVIDER/COMBINER

A. RECONFIGURABLE TWO-WAY ACTIVE POWER DIVIDER AND COMBINER

In order to achieve wide operational bandwidth, active power gain with good matching characteristics, moderate linearity, as well as high-level system integration requirement, the DA topology with internal RF-choke inductors and DC-blocking capacitors is chosen. For supporting both the power divider and the combiner operations, the BDA technique is applied to the proposed reconfigurable two-way SiGe active power divider/combiner. In addition, the series-shunt switch configuration is used to provide reconfigurable operation, as shown in Fig. 3. The input and output capacitances of the BDA cores form artificial transmission lines with lumped inductors. In principle, these artificial input and output lines are designed to have 50-Ω characteristic impedance and to achieve equal and flat group delay over the required band. In addition, in order to achieve wideband characteristics, the ends of artificial transmission lines are terminated by termination resistors (R_{T1} and R_{T2}), which absorb any backward waves. The artificial transmission line of P_1 consists of $L_{1,M}$, $L_{2,M}$, and the capacitance of two BDA cores, while for the P_2 and P_3 lines, L_1, L_2, and the capacitance of a single BDA core are used. As a result, the capacitance at the common node (P_1) is approximately doubled compared to the independent nodes (P_2 and P_3) capacitance. Therefore, the propagation velocity at the common and independent nodes can exhibits different characteristics because different capacitances and inductances were applied to achieve 50-Ω characteristic impedance. If multiple stages are used in this design to achieve desired performances (e.g., wide bandwidth, gain, and output power), the different phase characteristics will appear at the independent nodes of each stage. Therefore, it may lead to performance degradation at the high-frequency range. The proposed reconfigurable two-way active power divider/combiner used only a two-stage BDA structure to achieve the desired frequency range of 2 - 20 GHz with moderate gain and output power. In addition, in order to match the propagation velocity at the input and the output nodes as closely as possible, while maintaining flat gain response and good matching characteristics, the inductances at the common and independent nodes were carefully selected in this design.

Two series-shunt switch pairs (M_1/M_2 and M_3/M_4) are added to the circuit to support the reconfigurable operation of the dual-path or the single-path modes (see Fig. 1). The series transistors of M_1 and M_3 are added to select required signal path, while the shunt transistors of M_2 and M_4 are used for providing good isolation performance. To improve the insertion loss of series-shunt switches, the floating body and the N-well techniques are applied [20]. Nevertheless, the insertion loss of the series-shunt switches can lead to a decrease in gain and output power in the dual-path mode (power combiner/divider modes). In addition, a potential concern is that the leakage signal at OFF state can be propagated to other signal paths due to imperfect switch isolation characteristics. However, the series-shunt switches provide the key benefit of high-speed mode change for the dual-path mode and the single-path mode selection. As shown in Fig. 4, it takes only 0.7 and 1.6 ns to switch the operation mode. Therefore, it can support competitive switching time compared to commercial switches without requiring additional components and chip area [21].

For providing DC biasing and AC open, internal RF-Choke$_1$ and RF-Choke$_2$ are integrated into the proposed circuit. In addition, the DC-blocking capacitors (C_1, C_2, and $C_{2,M}$) are used at the common, the independent and the termination ports. While most amplifiers based on a DA structure use external bias tees for DC biasing [22], [23], this approach limits practical usefulness and reduces system integration levels. Therefore, the internal DC biasing of the proposed circuit not only provides high-level integration, but also supplies DC biasing path from the power supply.

To obtain the desired bandwidth and provide wideband matching characteristics, the capacitance and inductance should be carefully chosen because the operational bandwidth of the proposed reconfigurable two-way active power divider/combiner is determined by the 3-dB cut-off frequency (f_c) of the transmission line, given as:

$$f_{c,input,output} = \frac{1}{\pi\sqrt{L_{input,output}C_{parasitic,input,output}}} \quad (1)$$

In addition, the characteristic impedances of artificial transmission line for P_1, P_2, and P_3 can be calculated as follows:

$$Z_o = \sqrt{\frac{L_1}{C_{par,BDAs} + C_{par,INDs,Lines}}}, \quad \text{for } P_2 \text{ and } P_3 \quad (2)$$

$$Z_o = \sqrt{\frac{L_{1,M}}{2 \times C_{par,BDAs} + C_{par,INDs,Lines}}}, \quad \text{for } P_1 \quad (3)$$

Other important specifications of the proposed circuit, such as maximum output power and gain, are related to the size of the transistors and the number of gain stages [24]. Large transistors are required to achieve enough gain and output power. However, large transistors will reduce the bandwidth of the circuit based on (5), since large parasitic capacitance is associated with a large transistor. On the other hand, many gain stages with small transistors can increase gain, output power, and bandwidth of the circuit. However, there is an upper bound for the gain even if an infinite number of gain stages are cascaded, due to the input and the output resistances of the transistors and the series loss of on-chip inductors [25]. In the proposed circuit, the SiGe HBTs with the 0.12 x 8.0 μm^2 are chosen to achieve the requirements of reasonable gain (> 7 dB) and output power (0 dBm) for the 2-20 GHz bandwidth. Once the device size in the two-stage DA topology is determined, the bandwidth of the proposed circuit is limited by the cut-off frequency of the P_1 line, because its parasitic capacitance is approximately twice as large as the P_2 and P_3 lines. Figure 5 shows the calculated characteristic impedances and cut-off frequencies of the P_1 line with varied inductance ($L_{1,m}$) and capacitance of the BDA core (C_1) (See Fig. 2). In case of $L_{2,m}$, the twice the inductance of $L_{1,m}$ was selected for calculations. Based on the calculation results, the capacitance of C_1 should be carefully chosen for the desired operational bandwidth and the matching characteristics. In the proposed design, C_1 of 123.8 fF was selected to provide the optimal bandwidth for two gain stages.

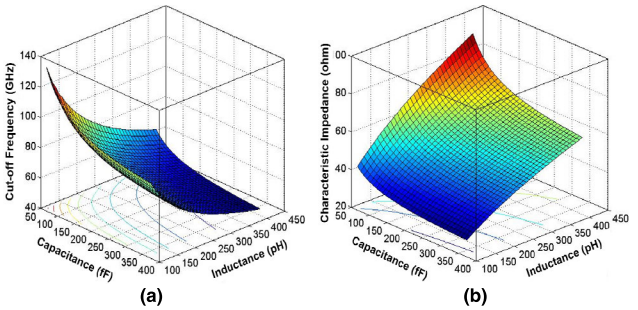

FIGURE 5. Simulated (a) cut-off frequency and (b) characteristic impedance of the P_1 line with varying capacitance of C_1 and inductance ($L_{1,m}$) under the fixed transistor size.

B. DUAL-PATH MODE (POWER DIVIDER/COMBINER MODE)

Figure 6 shows the equivalent circuit of dual-path mode depending on the power divider or combiner operation. For the dual-path mode, the switching transistors of M_1 and M_3 turn ON while M_2 and M_4 turn OFF. The cascode transistor of Q_2 and Q_3 are ON and OFF, respectively, for the power divider operation and the signal can be amplified through the BDA cores from P_1 to both P_2 and P_3, respectively (Fig. 3). Therefore, the power loss associated with the ideal 3 dB power division and lossy passive structures is compensated for active phased array antennas. The equivalent circuit under the power divider operation is shown in Fig. 6 (a). Since the cascode configuration provides good reverse isolation and the opposite Q_3 and Q_4 branch is turned off, the reverse signal can be effectively suppressed [26], which improves the port-to-port isolation. For the combiner mode, the cascode transistor Q_3 turns ON and Q_2 turns OFF, while maintaining Q_1 and Q_4 are ON-states, as shown in Fig. 6 (b). The transistors in the series-shunt switches show the same operation for both the power divider and the power combiner modes.

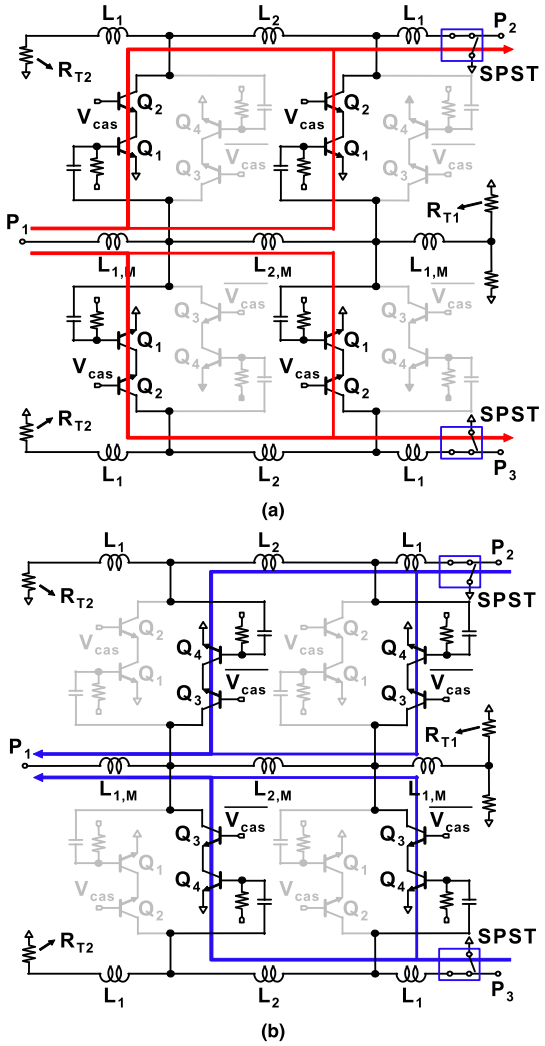

FIGURE 6. Equivalent circuit of the dual-path mode in bi-directional operation (a) from P_1 to P_2/P_3 (a divider mode) and (b) from P_2/P_3 to P_1 (a combiner mode).

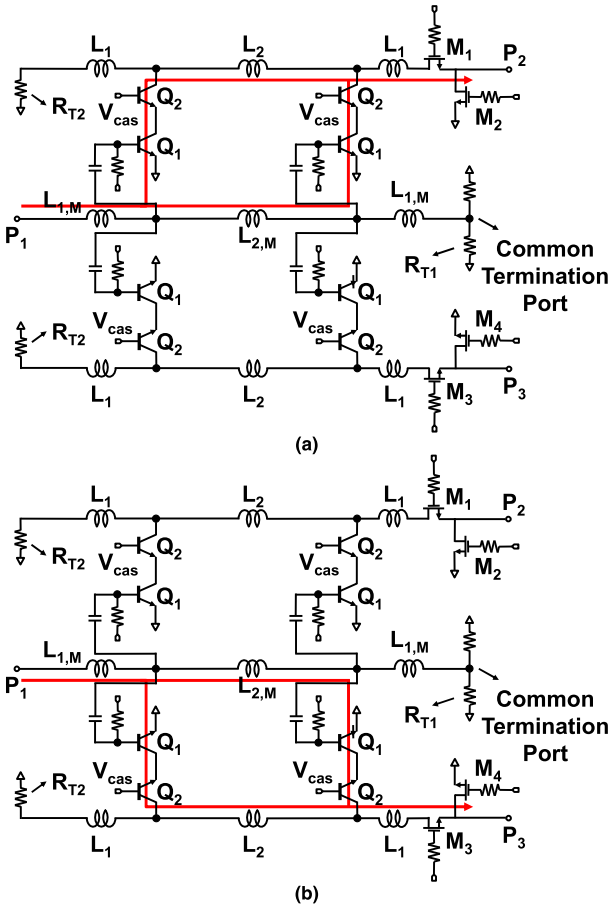

FIGURE 7. Equivalent circuit of the single-path mode under the power divider operation (a) from P_1 to P_2 and (b) from P_1 to P_3.

C. SINGLE-PATH MODE

The single-path modes in the power divider operation are shown in Fig. 7. For the single-path mode from P_1 to P_2, the cascode transistor Q_2 turns ON and Q_3 turns OFF, while maintaining the ON-state of Q_1 and Q_4. The series switch transistor M_1 turns ON and M_3 turns OFF for selecting the signal path of P_1 to P_2. The shunt transistor M_2 turns OFF and M_4 turns ON to improve isolation performance, thereby preventing unwanted signal from leaking, as shown in Fig. 7 (a). In Fig. 7 (b), the switching transistors M_2 and M_3 turn ON and M_1 and M_4 turn OFF while maintaining the operation of BDAs cores for the P_1 to P_3 mode.

D. PASSIVE COMPONENT DESIGN

The design of wideband circuits requires the accurate passive components, such as inductors, transmission lines, and short interconnections between transistors. In the proposed circuit, the grounded coplanar waveguides (GCPWs) are selected for interconnections due to their advantages, which can minimize unwanted signal leakage and coupling between adjacent signal lines. For the practical usefulness, RF-choke inductors and DC-blocking capacitors are integrated with the proposed circuit. While using large RF-choke inductors presents good AC open at low frequencies, due to the parasitic capacitance of the RF-choke inductors, the self-resonance frequency (SRF) of the components has to be taken into account. The simulated RF-choke inductors offer an inductance of 2.2 nH with the SRF of about 23 GHz. The other inductors, interconnections, and the GSG pads are carefully designed with an electromagnetic (EM) solver, Sonnet. From parasitic capacitance of BDA core, the theoretical inductances of L_1 and $L_{1,M}$ found to be 180 and 443 pH for 50-Ω characteristic impedance of artificial transmission lines. However, to match the propagation velocity between the common and the independent nodes as close as possible, the simulated inductances of L_1, and L_2 are 330 and 538 pH at 10 GHz, respectively, while $L_{1,M}$ and $L_{2,M}$ have the inductances of 299 and 450 pH at the same frequency, respectively. The termination resistances of R_{T1} and R_{T2} are 72.4 and 44.5 Ω for the optimized performance, respectively. A symmetric layout and topology are critical to provide the identical performance, such as

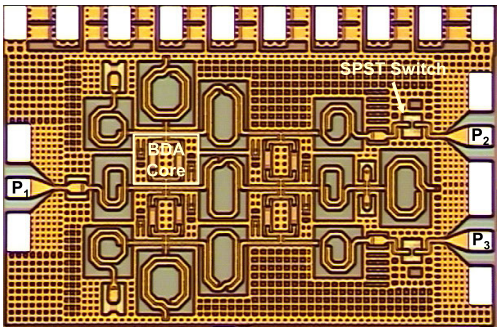

FIGURE 8. Microphotograph of the fabricated proposed reconfigurable wideband active SiGe active power divider/combiner.

phase and amplitude imbalances between the common or the independent ports depending on a required mode. Therefore, two capacitors and two resistors are connected to the common termination port (see Fig. 7) for reducing any unexpected mismatches.

IV. MEASUREMENTS

Figure 8 shows the microphotograph of the fabricated reconfigurable wideband SiGe active power divider/combiner implemented in Global Foundries 130 nm SiGe HBT BiCMOS technology (8HP). The total chip area is 1.3 mm^2 (1.43 mm $\times$ 0.92 mm), including pads. From a supply voltage of 3.0 V, the circuit draws a bias current of 40 mA, which amounts to the total DC power consumption of 120 mW for high power handling capability. The DC power consumption can be reduced by controlling bias of cascode and common emitter transistors depending on system power budget. When the bias current decreased from 40 mA to 19 mA, the small-signal gain variation is from 8 dB to 6.4 dB at 20 GHz.

A. SMALL SIGNAL MEASUREMENT

The small signal measurement of the proposed circuit was performed with on-wafer probing, and a 3-port calibration using a network analyzer (Agilent PNA E8364B) and an S-parameter test set (N4421A). The measured and simulated S-parameters of the proposed reconfigurable wideband active SiGe power divider/combiner under the dual-path mode are shown in Fig. 9. The power divider operation provides a peak small-signal gain of 10.3 dB with 3-dB bandwidth of 2-23 GHz. The input and the output return loss (S_{11}, S_{22}, and S_{33}) are better than 10 dB from 2 to 23 GHz, as shown in Fig. 9 (a). The bandwidth of the input (S_{11}) is smaller than S_{22} and S_{33}, because the parasitic capacitances of the input artificial transmission line are approximately doubled due to the two BDAs, as discussed in Section III. The power divider mode exhibits similar response for both paths (P_1 to P_2 and P_1 to P_3) due to the symmetric layout and topology. All S-parameter results show good agreement between the measurements and the simulations. The power combiner operation shows similar results to the power divider operation, as shown in Fig. 9 (b).

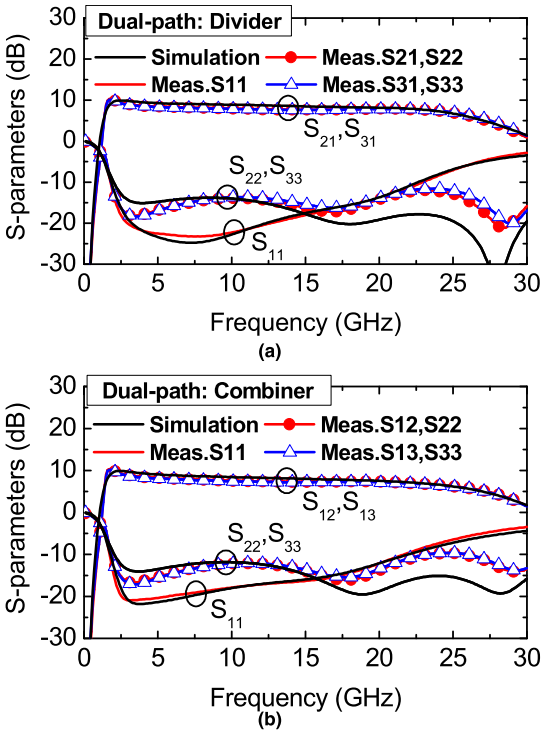

FIGURE 9. Measured and simulated S-parameters of the proposed reconfigurable wideband active SiGe power divider/combiner. (a) The single-path mode (P_1 to P_2) and (b) the single-path mode (P_1 to P_3) under the power divider operation.

The measured and the simulated S-parameters of the single-path mode under power divider operation are shown in Fig. 10 (a) and (b), depending on its operational mode. The measured gain difference between ON and OFF states is larger than 16.5 dB within 2-23 GHz for both operational modes. All of the measured results are similar to the dual-path mode under power divider operation. For the power combiner operation, the measured results are similar to the power divider operation.

The port-to-port isolation is critical for the overall circuit performance because poor isolation performance leads to undesired signal coupling between input and output ports depending on operational modes. The measured port-to- port isolation of the proposed reconfigurable power divider/combiner is presented in Fig. 11. In Fig. 11 (a), the minimum isolation between P_2 and P_3 under the dual-path mode for both the divider and the combiner operations is about 23 dB at 2 GHz. The measured port-to-port isolation under the single-path mode for the divider operation is better than 35 dB in 2-23 GHz as shown in Fig. 11 (b). The power combiner operation shows almost identical characteristics.

The measured amplitudes and phase imbalances are shown in Fig. 12. The measured amplitude imbalance of both the power divider and the combiner operations is less than 0.2 dB. In the power divider mode, the phase imbalance has slightly larger than for the power combiner mode. The phase imbalance in the power divider mode is 1.4° at 2 GHz and −1.8° at 23 GHz, respectively. The stability factor (k-factor) is greater

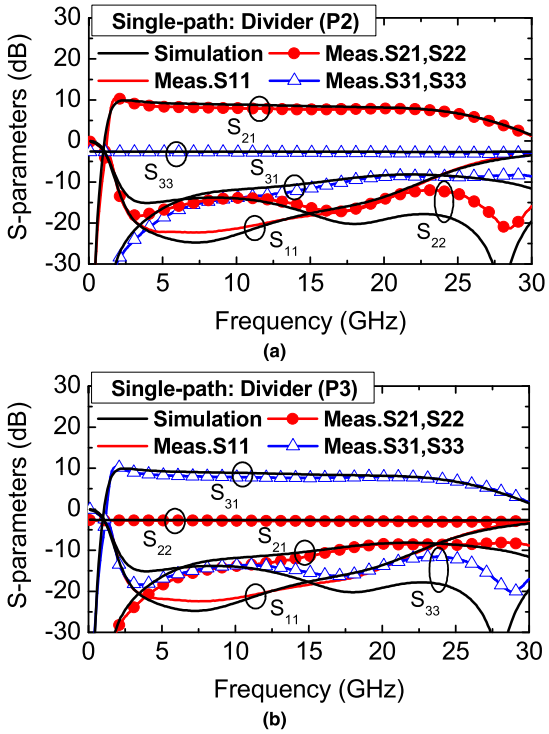

FIGURE 10. Measured and simulated S-parameters of the proposed reconfigurable wideband active SiGe power divider/combiner. (a) The power divider and (b) the power combiner operations under the dual-path mode.

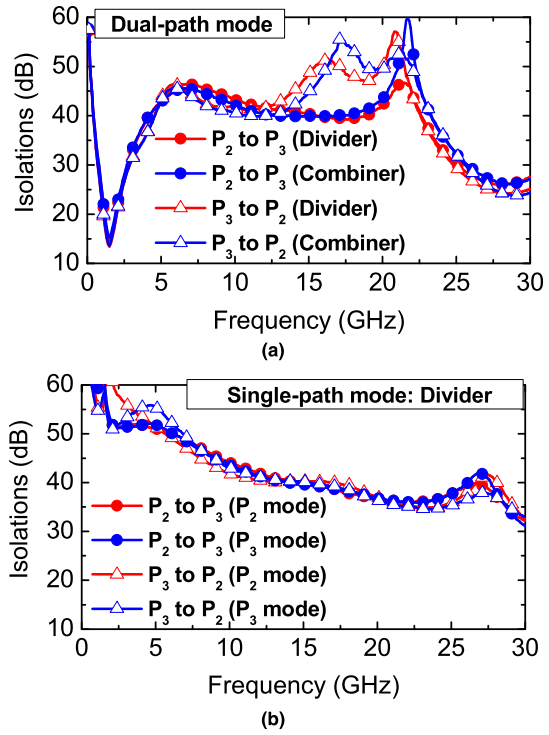

FIGURE 11. Measured isolation characteristics between P2 and P3. (a) The dual-path mode with both the power divide/combiner operations and (b) the single-path mode with the power divider operation.

than 1.95 up to 30 GHz [Fig. 12 (b)]. The single-path mode shows similar characteristics compared to the dual-path mode response.

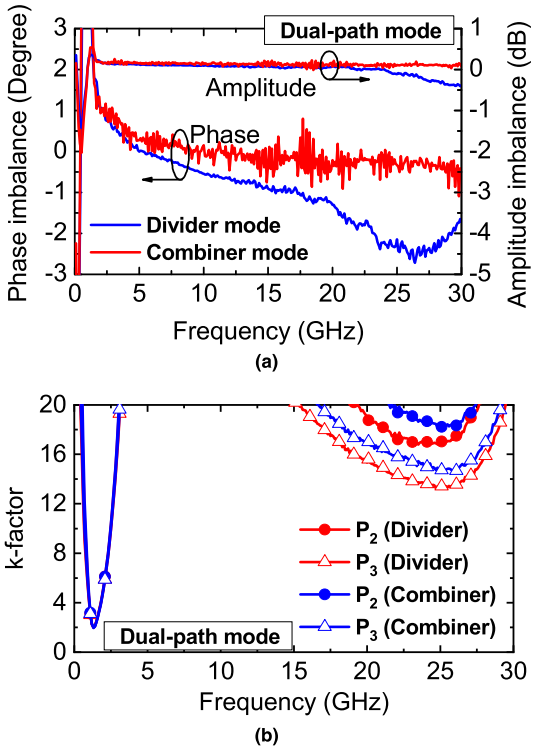

FIGURE 12. Measured (a) amplitude and phase imbalances and (b) stability factor for both the power divider and the combiner operations.

B. MEASUREMENT SETUP FOR NOISE FIGURE AND LINEARITY

The measurement setups for noise and linearity characterization are shown in Fig. 13. In order to verify the power divider operation, we used a single-port configuration as shown in Fig. 13 (a). On the other hand, we used two different measurement setups for the power combiner operation as shown in Fig. 13 (b) and (c).

1) SINGLE-PORT CONFIGURATION

The signal generator (E8257D) or the noise source (N4002A) are connected to the proposed circuit directly depending on purpose of measurement as shown in Fig 13 (a) and (b). The unused third port is terminated with 50-Ω. To confirm the NF or the output power, the PXA signal analyzer (N9030A) or the power sensor (E4413A) are connected to the output port, respectively. This measurement method is generally used for the NF and linearity measurement, but it is not sufficient to verify the actual operation of the power combiner. Therefore, we used a dual-port configuration to verify the practical power combiner operation with reconfigurable functionality.

2) DUAL-PORT CONFIGURATION

For the measurement of NF and linearity characteristics under the practical power combiner operation with reconfigurable functionality, the noise source or signal generator are con-

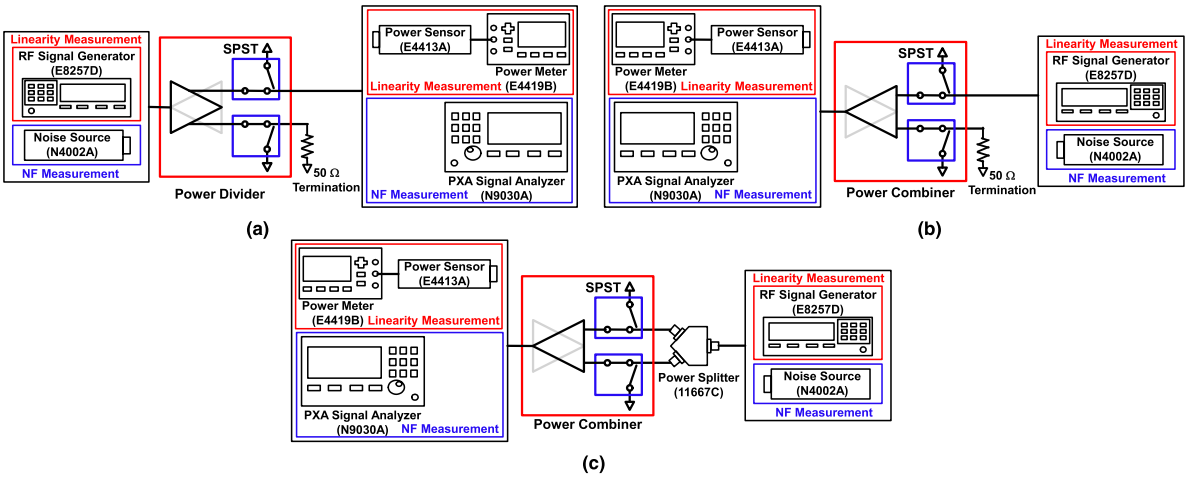

FIGURE 13. Measurement setups of (a) the single-port configuration for the power divider operation and (b) the single-port configuration and (c) the dual-port configuration for the power combiner operation.

nected to an wideband power splitter (11667C) as shown in Fig. 13 (c). Therefore, the same signal or noise waves are simultaneously driven to the two input ports of P_2 and P_3 by a signal generator or a noise source. In the reconfigurable wideband phased array antennas, since the input signals are delivered to the reconfigurable active power combiner through frond-end and control circuits from each antenna element, this measurement is a more suitable method to verify the circuit operation under the reconfigurable power combiner operation.

C. NOISE FIGURE AND LINEARITY MEASUREMENT

The measured and simulated noise figure (NF) versus frequency is presented in Fig. 14 (a) depending on the operation mode (i.e., power dividing or combining) under the single-port configuration (see Fig. 13). The minimum NF of the power divider operation is 7.7 dB at 18 GHz and the overall NF is better than 10 dB from 6 to 24 GHz. On the other hand, since the input inductance and capacitance are different depending on the operation modes (power divider and combiner modes), the optimum noise circle is changed between power divider and combiner operation. In addition, the insertion loss of the series-shunt switch increases the NF of the power combiner operation. As a result, the overall NF under the power combiner operation is larger than the power divider operation for the entire band. The overall NF of the power combiner operation is better than 12 dB from 8 to 26 GHz, with the minimum NF of about 10 dB at 12 GHz. Each signal path has similar NF characteristic for both the power divider and combiner operations.

The NF characteristics with noise combination under power combiner operation were measured using the dual-port configuration. The measured and the simulated NF from the two-input power combiner operation is shown in Fig. 14 (b). Both NF characteristics (from P_2 to P_1 and from P_3 to P_1) under the single-path mode show similar performance.

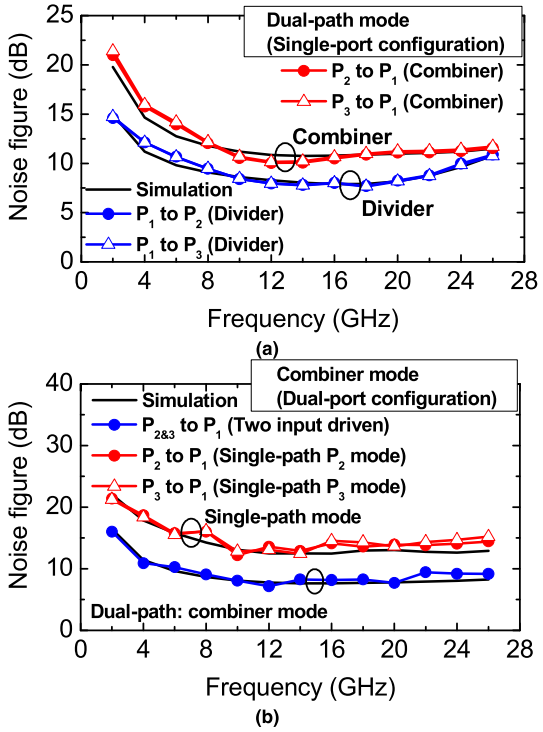

FIGURE 14. Measured P1dB and IP3 responses of the proposed reconfigurable wideband active SiGe power divider/combiner under dual-path mode using the single-port configuration. (a) The power divider and (b) the combiner operations.

However, since the series transistor is turned off and the shunt transistor is terminated to ground in unused other branch, the NF characteristic under the dual-port configuration is changed due to internal mismatch between the external power splitter and the proposed circuit. Therefore, the overall NFs under the single-path mode using the dual-port configuration are increased about 2.0 dB compared to the single-port configuration. To prevent this issue, an adaptive termination

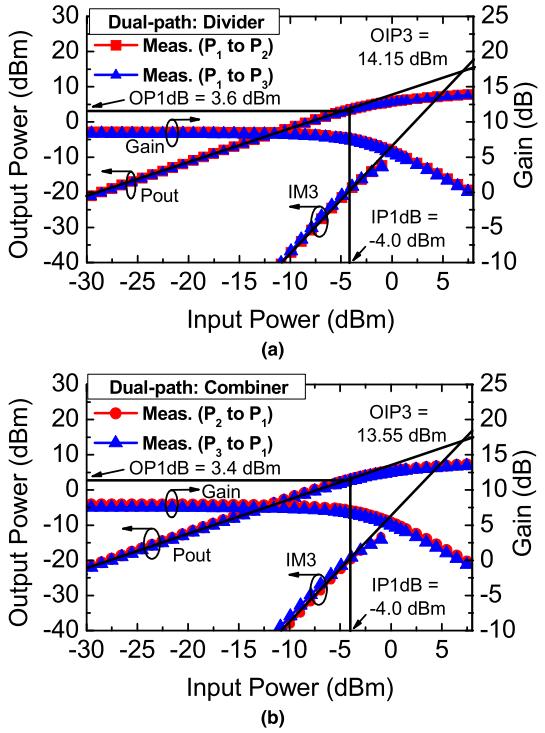

FIGURE 15. Measured large-signal responses of the power divider and combiner operations using single-port configuration. (a) The single-path mode (P_1 to P_2) and (b) the single-path mode (P_1 to P_3).

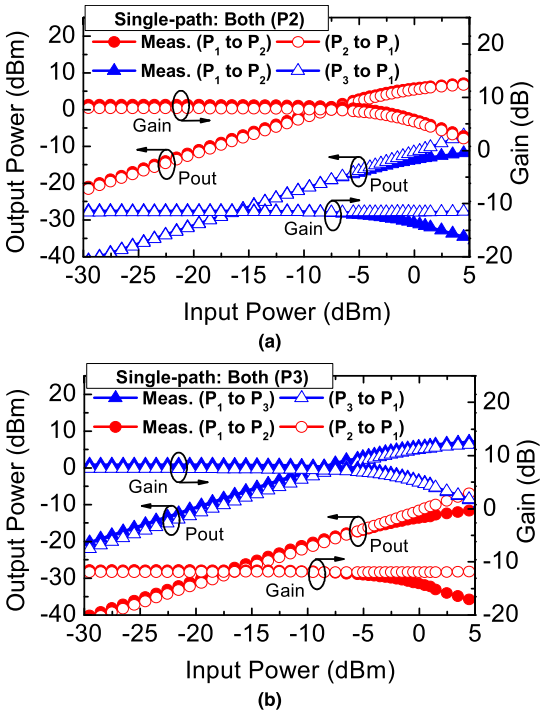

FIGURE 16. (a) Measured and simulated noise figure under dual-path mode using the single-port configuration for both the power divider and the combiner operations. (b) Measured and simulated noise figure under the dual-path and the single-path modes for the power combiner operation when two input noise sources are applied (dual-port configuration).

technique needs to be applied. In dual-path mode, the overall NF is better than about 3.0 dB compared to the single-port configuration. The NF is better than 10 dB from 6 to 26 GHz with the minimum NF of about 7.2 dB at 12 GHz.

The input and output 1-dB compression points (IP1dB and OP1dB) and output third-order intercept point (OIP3) at 12 GHz under divider and combiner operations using the single-port configuration are presented in Fig. 15. In Fig. 15 (a), the P_1 to P_2 and the P_1 to P_3 under the dual-path power divider mode show an OP1dB of 3.6 dBm and the corresponding IP1dB is −4.0 dBm. In addition, the third-order intermodulation distortion (IM3) was measured with two different signals of 50 MHz spacing. The measured OIP3 is about 14.2 dBm at 12 GHz. For the dual-path power combiner mode, all of the large-signal performance is close to the power divider operation. The measured IP1dB and OP1dB are −4.0 and 3.4 dBm, respectively, while the OIP3 is about 13.6 dBm at 12 GHz [Fig. 15 (b)].

The large-signal performance of the single-path mode under the power divider and combiner operations is shown in Fig. 16 (a) and (b). The large-signal performances in the ON state of the power divider and combiner operations are similar to the dual-path mode. For the OFF state of the power divider operation, the measured IP1dB and OP1dB for the P_2 signal path are −4.0 and −16.3 dBm, respectively. The OFF state of the P_3 signal path has similar large-signal performance compared to the P_2 signal path. However, the OFF state of the power combiner operation indicates different large-signal characteristics. Since the series transistor of the series-shunt switch is turned off, the input power delivered to the SiGe HBT in the BDA cores was significantly attenuated by the passive series-shunt switch. Therefore, the linearity of the power combiner mode in the OFF state shows a similar behavior of a passive circuit.

Figure 17 (a) shows the measured OP1dB and OIP3 versus frequency under both the power divider and the combiner operations using the single-port configuration. The proposed reconfigurable active power divider/combiner shows moderate output power for both operations. It exhibited 1.3 and 3.8 dBm OP1dB at 2 and 22 GHz under the power divider operation, respectively. The OIP3 is found to be 12.4 and 14.0 dBm at 2 and 22 GHz for the P_1 to P_2 path, respectively. The measured OP1dB and OIP3 under power combiner operation are similar to the power divider operation. The maximum OP1dB and OIP3 are 4.6 and 15.4 dBm, respectively. In Fig. 17 (b), the two sinusoidal signals of the same magnitude and phase are supplied to the input ports (P_2 and P_3) for the demonstration of the signal combination under the power combiner operation [See Fig. 13 (c)]. Since series-shunt switches are used in the proposed circuit, the leakage signals are delivered through the OFF-state series transistors under the single-path mode from either P_2 or P_3 to P_1 due to imperfect switch characteristics (See Fig. 4). Therefore, the high isolation of the series-shunt switch is

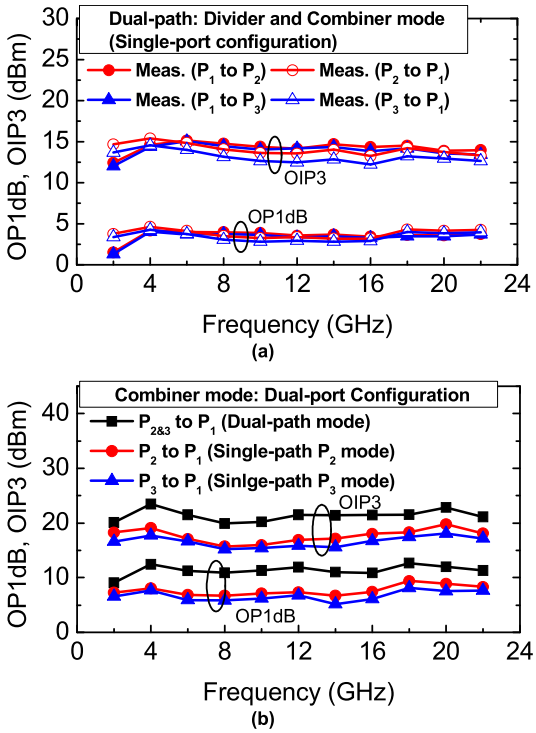

FIGURE 17. (a) Measured OP1dB and OIP3 versus frequency under the power divider and power combiner operations when the single input signal is applied (single-port configuration) and (b) Measured OP1dB and OIP3 versus frequency under the dual-path and the single-path modes for power combiner operation when two input signals are applied (dual-port configuration).

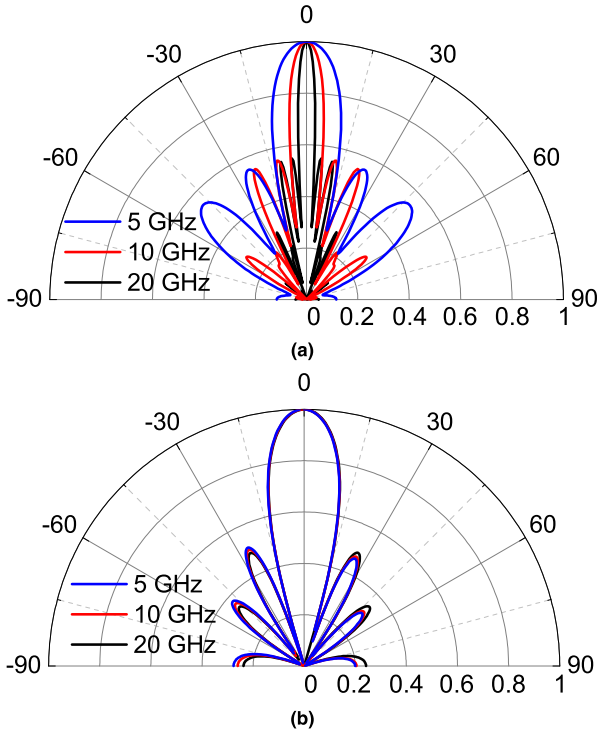

FIGURE 18. Normalized and synthesized antenna array patterns at broadside based on the measured S-parameters for 5, 10, 20 GHz with the fixed antenna spacing (7.5 mm). (a) Every antenna in the array are turned on when he proposed active power divider/combiner circuit are under the dual-path mode. (b) Antenna in the array is selectively turned on when the proposed active power divider/combiner circuits are under the single-path mode (see Fig. 1).

critical to prevent this undesirable effect because the output power under the single-path mode can be corrupted by the phase of the leakage signal. In this measurement case, the measured OP1dB and OIP3 under the single-path mode using the dual-port configuration are higher than the single-port configuration. The OP1dB and OIP3 of the P_2 to P_1 path are 9.4 and 18.3 dBm at 20 GHz in single-path mode. In the dual-path power combiner mode, the two input signals are driven to the two-stage BDAs and the amplified signals are combined at single output node. Therefore, the output power of the dual-path mode is higher than that of the single-path mode. In dual-port configuration, The OP1dB and OIP3 of the P_2 to P_1 path are 12 and 22.8 dBm at 20 GHz, respectively.

To evaluate the effects of the proposed reconfigurable active power divider and combiner on beam width and operating frequency, beam synthesis simulations were performed. An array size of 1x32 with antenna spacing of $\lambda/2$ (7.5 mm) at 20GHz was chosen to confirm beam width at 5, 10, and 20 GHz. To verify the effects of the proposed reconfigurable power dividers/combiners on the system, they were placed after the control circuits and other components used the ideal circuits (see Fig. 1). In addition, since the signal path of the OFF states in the proposed circuit is terminated to ground through the shunt transistors, the symmetry of the beam can be influenced by how the antenna elements are selected. Therefore, the 50 Ω terminations were used to the signal paths of the OFF states for more accurate simulation results. The synthesized antenna array patterns based on the measured S-parameters are shown in Fig. 18. The total of 16 proposed active power divider/combiner circuits under the dual-path mode were used to implement an 1×32 antenna array for Fig. 18 (a). As shown in Fig. 18 (a), it shows varying beam widths depending on the operating frequency. On the other hand, the proposed active power divider/combiner circuits under the single-path mode were selectively turned on to generate a constant beam width. The antenna sizes become 1×32, 1×16, or 1×8 configurations, when the operating frequencies are 20, 10, or 5 GHz, respectively. The reconfigurable wideband phased array using the proposed circuit with the single-path mode indicates a constant beam width at 5, 10, and 20 GHz as shown in Fig. 18 (b). As a result, the proposed circuit can support an adjustable beam width for different frequencies. As described above, for system integration, the OFF state of the proposed circuit should be terminated to the 50 Ω through the shunt transistors.

Table 1 presents the summary and the comparison with other recent state-of-the-art designs. The proposed reconfigurable power divider/combiner provides positive in-band flat gain with wide operational bandwidth (2-23 GHz), controllable bi-directional operation (power divider and combiner modes), and reconfigurable operation (dual-path and single-path modes) by using BDAs and series-shunt switches.

TABLE 1. Performance comparison with the state-of-the-art reconfigurable power dividers and combiners.

Reference	[12]		[14]	[16]	[6]		[10]	[11]	**This work**
Process technology	0.13 µm CMOS		90 nm CMOS	0.13 µm SiGe BiCMOS	0.2 µm GaAs PHEMT		Rogers 4003C	Rogers 6002	**0.13 µm SiGe BiCMOS**
Operation mode	divider	combiner	Divider	both	divider	combiner	divider	both	**both**
Reconfigurable operation	None		None	None	Support, Two-way		Support, Four-way	Support, Three-way	**Support, Two-way**
Circuit topology	Active-based, DA[1]		Active-based, IL[2]	Active-based, BDA[3]	Active-based, DA[1]		Passive-based WPD[4]	Passive-based WPD[4]	**Active-based, BDA[3], Switching**
Bandwidth [GHz]	1-10.6	1-10.6	DC-40	2.0-22.0	2.0-18.0	2.0-18.0	2.3-2.6	4.8-5.2	**2.0-23.0**
Gain (div./comb.) [dB]	9.5	6.0	5.0	9.6 / 8.9	2.4-3.2	3.9-4.9	-7.2[+]	-5.51[#] / -5.51[#]	**9.3±1.5 / 9.3±1.5**
Isolation (div./comb.) [dB]	N.A.	N.A.	> 28	> 22 / > 21	-	-	12.1[+]	26.2[#]/26.2[#]	**> 23 / > 23**
NF (div./comb.) [dB]	N.A.	5.0	7.0	11 / 13	< 6.5*	< 7.6*	-	-	**10 / 12**
Amp./phase. imbalance [dB/º]	N.A.	N.A.	0.16 / 14	0.8 / 3.5	-	-	-	0.1[#] / 1.8[#]	**0.2 / 1.8**
OP1dB (div./comb.) [dBm]	7.1	N.A.	5	2 / 3	-	-	-	-	**3.6 / 3.4**
OIP3 (div./comb.) [dBm]	N.A.	N.A.	N.A	11 / 12	21	20.6	-	-	**14.2 / 13.5**
P_{DC} [mW]	20.5	15.3	210	100	-		-	-	**120**
Die area [mm^2]	1.17	1.0	0.86	1.3	4.0	4.0	4225	-	**1.3**

[1]: Distributed amplifier. [2]: Interleaf. [3]: Bi-directional DA. [4]: Wilkinson power divider. *: 7.5-12 GHz. +: 1:4 power dividing mode. #: Three-path mode.

Compared with III-V technology implementations, it can provide seamless integration with digital circuitry on same die. It also exhibits good isolation, impedance matching, amplitude/phase imbalance, fast mode switching, and moderate RF linearity (OP1dB and OIP3) in its bandwidth.

V. SUMMARY

This paper has introduced a wideband reconfigurable two-way SiGe active power divider/combiner circuit for large scale wideband reconfigurable active phased array antennas. The design methodology of using a BDA to enable the technique is presented, with a special focus on the effect of the bandwidth of the proposed circuit. To provide bi-directional operation with wide operational bandwidth and high speed mode selection for reconfigurable functionality, the proposed reconfigurable active power divider/combiner using two-stage BDAs and series-shunt switches is implemented in a 130 nm SiGe BiCMOS platform. Compared to reported reconfigurable power dividers and combiners, the proposed circuit demonstrates active gain without requiring additional amplifiers, wide operational bandwidth, and moderate large-signal performance under a DC power consumption of 120 mW.

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REFERENCES

[1] Y. Chung, J. Jeong, Y. Wang, D. Ahn, and T. Itoh, "Power level-dependent dual-operating mode LDMOS power amplifier for CDMA wireless base-station applications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 739–746, Feb. 2005.

[2] H. Fan, X. Liang, J. Geng, R. Jin, and X. Zhou, "Switched multibeam circular array with a reconfigurable network," *IEEE Trans. Antennas Propag.*, vol. 64, no. 7, pp. 3228–3233, Jul. 2016.

[3] M. Ali, M. Kamarudin, M. N. M. Tan, and T. A. Rahman, "Reconfigurable beam shaping antenna with Wilkinson power divider at 5.8 GHz," in *Proc. IEEE Int. RF Microw. Conf.*, Kuala Lumpur, Malaysia, Dec. 2008, pp. 436–440.

[4] K. M. Fathy, E. M. Mansour, N. Nasr, M. Emad, M. A. Ali, and H. F. Hammad, "Adaptable reconfigurable antenna array system with multi–angle and tri–polarization diversity [education column]," *IEEE Antennas Propag. Mag.*, vol. 56, no. 5, pp. 223–237, Oct. 2014.

[5] A. Ouacha, R. Erickson, R. Gunnarsson, B. Carlegrim, C. Samuelsson, and S. Leijon, "Wideband antenna arrays with reconfigurable beamforming and beamshaping," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2007, pp. 1867–1870.

[6] T. Nilsson, C. Samuelsson, M. Alfredson, and A. Ouacha, "Key circuits for a reconfigurable and bi-directional beamformer for ultra wideband applications," in *Proc. 33rd Eur. Microw. Conf.*, Munich, Germany, Oct. 2003, pp. 735–738.

[7] Y. Chung, R. Song, K. Kim, D. Ahn, and T. Itoh, "Power routing scheme with dual operating modes: Two-way Wilkinson divider and one-way signal path," *Electron. Lett.*, vol. 40, no. 2, pp. 129–130, Jan. 2004.

[8] K. Tae Kim, Y. Chung, J. Hoon Kang, T. Itoh, and D. Ahn, "Reconfigurable power divider and combiner with variable power ratio," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Oct. 2004, pp. 57–60.

[9] T. Lehmann, F. Hettstedt, and R. Knoechel, "Reconfigurable Wilkinson power dividers with minimum number of switches," *Electron. Lett.*, vol. 45, no. 2, pp. 111–112, Jan. 2009.

[10] H.-S. Tae, K.-S. Oh, H.-L. Lee, W.-I. Son, and J.-W. Yu, "Reconfigurable 1×4 power divider with switched impedance matching circuits," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 2, pp. 64–66, Feb. 2012.

[11] H. Fan, J. Geng, X. Liang, R. Jin, and X. Zhou, "A three–way reconfigurable power divider/combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 986–998, Mar. 2015.

[12] A. Safarian, L. Zhou, and P. Heydari, "CMOS distributed active power combiners and splitters for multi–antenna UWB beamforming transceivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1481–1491, Jul. 2007.
[13] S.-H. Weng and H.-Y. Chang, "A broadband inductorless active power divider for 10 Gbps high speed transmissions," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 3, pp. 197–199, Mar. 2014.
[14] C.-Y. Huang and R. Hu, "DC–40 GHz wideband active power splitter design with interleaved transmission-line gain cells," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, Dec. 2015, pp. 1–3.
[15] W. Lo and W. Chan, "Broadband integrated active divider and combiner based on distributed amplification," *Electron. Lett.*, vol. 44, no. 13, pp. 779–780, Jun. 2008.
[16] I. Song, M.-K. Cho, J.-G. Kim, and J. D. Cressler, "A SiGe–BiCMOS wideband (2–22 GHz) active power divider/combiner circuit supporting bidirectional operation," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4676–4684, Dec. 2016.
[17] M.-K. Cho, J.-G. Kim, and D. Baek, "A switchless CMOS bi–directional distributed gain amplifier with multi–octave bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 11, pp. 611–613, Nov. 2013.
[18] M.-K. Cho, I. Song, J.-G. Kim, and J. D. Cressler, "An active bi–directional SiGe DPDT switch with multi–octave bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 4, pp. 279–281, Apr. 2016.
[19] M.-K. Cho, I. Song, Z. E. Fleetwood, and J. D. Cressler, "A SiGe–BiCMOS wideband active bidirectional digital step attenuator with bandwidth tuning and equalization," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 8, pp. 3866–3876, Aug. 2018.
[20] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 31–39, Jan. 2006.
[21] MACOM. *Datasheet of MASW-002103-1363*. Accessed: Nov. 10, 2019. [Online]. Available: https://cdn.macom.com/datasheets/MASW-002103-1363.pdf
[22] J. Chen and A. M. Niknejad, "Design and analysis of a stage–scaled distributed power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1274–1283, May 2011.
[23] B. Sewiolo, G. Fischer, and R. Weigel, "A 12-GHz high–efficiency tapered traveling–wave power amplifier with novel power matched cascode gain cells using SiGe HBT transistors," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 10, pp. 2329–2336, Oct. 2009.
[24] A. Arbabian and A. Niknejad, "Design of a CMOS tapered cascaded multistage distributed amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 4, pp. 938–947, Apr. 2009.
[25] D. M. Pozar, *Microwave Engineering*. New York, NY, USA: Wiley, 1998.
[26] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.

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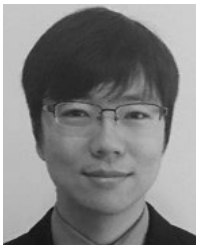

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