# High Resolution a-IGZO TFT Pixel Circuit for Compensating Threshold Voltage Shifts and OLED Degradations

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**ABSTRACT** In this paper, we propose a novel voltage programmed pixel circuit based on amorphous-indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) for active-matrix organic light-emitting displays. Through the extensive simulation work based on a-IGZO TFT and OLED models, we confirm that the proposed pixel circuit can compensate for threshold voltage variations of TFTs and OLED degradation over wide dynamic range ($\sim 10^4$) of OLED current as well as achieve a high pixel aperture ratio with the suppressed OLED current error rate below 9%.

**INDEX TERMS** Active-matrix organic light-emitting display (AMOLED), pixel circuit, amorphous-indium-gallium-zinc-oxide TFT (a-IGZO TFT), compensation, high aperture ratio.

## I. INTRODUCTION

Recently, it has been started to manufacture active-matrix organic light-emitting displays (AMOLEDs) by display industries as commercial products. Among various backplane technologies for AMOLEDs, amorphous indium-gallium-zinc-oxide thin-film transistor (a-IGZO TFT) has been adopted particularly for large-sized display backplanes due to its high field-effect mobility, low leakage current, and good electrical stability and uniformity over large area [1]–[3]. However, current AMOLEDs still suffer from remaining technical problems such as threshold voltage variation of TFTs and OLED degradation which consequently results in additional problem of the small aperture ratio created by the complicated compensation pixel circuits. In order to resolve these problems for accelerating the market penetration of AMOLEDs, many different approaches for achieving efficient compensating pixel circuits have been developed [4]–[10]. Among those, current programming method has been generally known to have superior property on the precisely compensation of threshold voltage and mobility variation of TFTs using current-mirror or current-scaling scheme [4], [5]. However, at the same time, the current programming method has the slow programming time issue especially when the OLED current level is low, which makes it hard to be implanted for commercial products. On the other hand, voltage programming methods provide fast programming time but require relatively large numbers of TFTs and capacitors to compensate threshold voltage variation of TFTs and OLED degradation [6], [7], resulting in reductions of pixel aperture ratio and display resolution which leads to an increase of the power consumption. Therefore, there have been constant demands for developing the high performance pixel circuit for AMOLEDs to resolve the problems mentioned above.

This paper presents a novel pixel circuit compensating for threshold voltage variation of TFTs and OLED degradation with a reduced and the number of signal lines, achieving a high aperture ratio and low power consumption to be applied for large size and high resolution AMOLED displays.
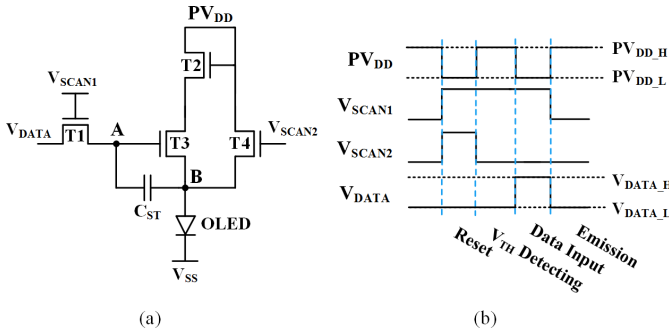
**FIGURE 1.** (a) Schematic circuit diagram and (b) operational waveforms of the proposed pixel circuit.



**FIGURE 2.** Operation phases of the proposed pixel circuit (a) Reset (b) $V_{TH}$ detecting (c) Data input and (d) Emission.

## II. PROPOSED CIRCUIT CONFIGURATION AND ITS OPERATION

Fig. 1(a) shows the proposed pixel circuit consisting of one driving TFT (T3), three switching TFTs (T1, T2, and T4), one storage capacitor ($C_{ST}$), and four signal lines. Fig. 1(b) shows operational input signal waveforms for the proposed pixel circuit; $V_{SCAN1}$ and $V_{SCAN2}$ are control signals for supplying the data input and resetting the source node voltage of driving TFT, respectively. $V_{DATA}$, $PV_{DD}$, and $V_{SS}$ refer to input data voltage, DC power supply, and ground-state signal lines, respectively. The operation phase of the proposed circuit is divided into four periods: reset, $V_{TH}$ detecting, data input, and emission. Fig. 2 (a)-(d) shows the operation phase schemes and principles of the proposed circuit as described as below.

### A. RESET PHASE
During the reset phase, the control signal $V_{SCAN1}$ and $V_{SCAN2}$ are set to high level, so that T1 and T4 are turned on. Through these TFTs, node A and B are set to $V_{DATA\_L}$ and $PV_{DD\_L}$, respectively. Thus, in this phase, the gate and source nodes of driving TFT are reset to default reset voltages regardless of the voltage distribution in the previous phase. At the same time, since T2 and T3 are turned off, the OLED current doesn't flow from the anode to the cathode of the OLED for enhancing the contrast ratio of the display.

### B. $V_{TH}$ DETECTING PHASE
During the $V_{TH}$ detecting phase, signal levels of $PV_{DD}$ and $V_{SCAN2}$ are inverted whereas the $V_{SCAN1}$ level is maintained as high. As a result, node A is maintained as $V_{DATA\_L}$, and node B is source-followed through T2 and T3 so that $C_{ST}$ can be charged up to $-V_{TH\_T3}$ since $V_{DATA\_L}$ is set equal to 0 V. Therefore, $C_{ST}$ stores the detected voltage equal to the threshold voltage of T3.

### C. DATA INPUT PHASE
In this phase, $PV_{DD}$ is changed to a low level while both $V_{SCAN1}$ and $V_{SCAN2}$ keep their voltages same as in the previous phase. Accordingly, node A is charged up to $V_{DATA\_H}$ since there is no voltage supplied by $PV_{DD}$ through T2. At
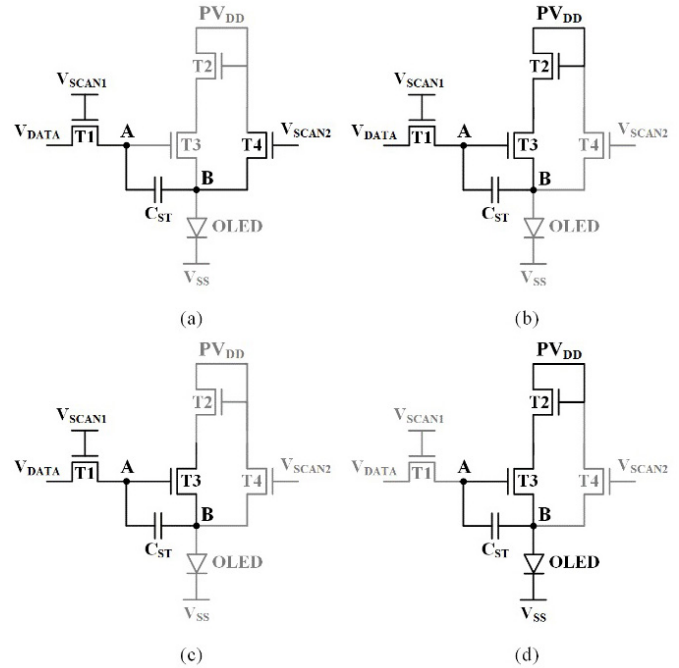
the same time, due to the coupling effect of $C_{ST}$ and $C_{OLED}$, node B is slightly charged up to $-V_{TH\_T3} + [C_{ST}/ (C_{ST} + C_{OLED})]V_{DATA}$.

### D. EMISSION PHASE
In the final phase, all signal lines have low voltage levels except $PV_{DD}$ signal. In this phase, since T4 is turned off by $V_{SCAN}$, node B is determined to be equal to $V_{OLED}$. Subsequently, the storage voltage at $C_{ST}$ is maintained as same as in the data input phase, and node A is set to $V_{TH\_T3} + [C_{OLED}/ (C_{ST} + C_{OLED})]V_{DATA} + V_{OLED}$ by the voltage conservation as in the follow equation.

$$V_{B(Phase\_D)} = V_{OLED}$$
$$V_{A(Phase\_D)} = V_{A(Phase\_C)} - V_{B(Phase\_C)} + V_{OLED}$$
$$= V_{DATA\_H}$$
$$- \left( -V_{TH\_T3} + \frac{C_{ST}}{C_{ST} + C_{OLED}} V_{DATA\_H} \right)$$
$$+ V_{OLED}$$
$$= V_{DATA\_H} \left( 1 - \frac{C_{ST}}{C_{ST} + C_{OLED}} \right)$$
$$+ V_{TH\_T3} + V_{OLED}$$
$$= V_{TH\_T3} + \left( \frac{C_{OLED}}{C_{ST} + C_{OLED}} \right) V_{DATA\_H}$$
$$+ V_{OLED} \tag{1}$$

Since the OLED current is equal to the current flowing at driving TFT (T3), so the OLED current can be defined

**TABLE 1.** Design parameters of proposed pixel circuit.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_{SCAN1}$ | -7 ~ 15 V | W/L of T1,T2, and T4 | 5 $\mu$m/5 $\mu$m |
| $V_{SCAN2}$ | -7 ~ 15 V | W/L of T3 | 10 $\mu$m/5 $\mu$m |
| $PV_{DD}$ | -5 ~ 15 V | $C_S$ | 0.4 pF |
| $V_{DATA}$ | 0.4 ~ 2.7 V | $C_{OLED}$ | 3 nF |
| $V_{SS}$ | 0 V | | |

as in the follow equation,

$$
\begin{aligned}
I_{OLED} &= \frac{k}{2} \left( V_{GS\_T3} - V_{TH\_T3} \right)^2 \\
&= \frac{k}{2} \left( V_A - V_B - V_{TH\_T3} \right)^2 \\
&= \frac{k}{2} \left( V_{TH\_T3} + \frac{C_{OLED}}{C_S + C_{OLED}} V_{DATA} + V_{OLED} \right. \\
&\qquad \left. - V_{OLED} - V_{TH\_T3} \right)^2 \\
&= \frac{k}{2} \left( \frac{C_{OLED}}{C_{ST} + C_{OLED}} V_{DATA} \right)^2 \approx \frac{k}{2} V_{DATA}^2 \qquad (2)
\end{aligned}
$$

where $k = \mu C_{OX} W/L$. As shown from (2), the OLED current during the emission phase is independent of variation of the threshold voltage of T3 and the operating voltage of OLED. In general, the value of $C_{OLED}$ can be varied by the mismatch during the process or by bias conditions. On the contrary, the value of $C_{ST}$ is relatively very stable and is rarely perturbed by the process since it is usually well defined by the photolithography. When we compare the values of $C_{OLED}$ and $C_{ST}$ for the conventional AMOLED display pixel, the value of $C_{OLED}$ ($\sim$ nF) is generally much larger than that of $C_{ST}$ ($\sim$ pF). Therefore, from this relationship, our equation (2) for $I_{OLED}$ can be simplified, and $I_{OLED}$ depends solely on $V_{DATA}$. Therefore, we can expect that the proposed pixel circuit can supply stable OLED current regardless of $V_{TH}$ or $C_{OLED}$ variations caused by the harsh stress conditions.

## III. SIMULATION RESULTS AND LAYOUT

To confirm compensation functionality of proposed pixel circuit, we performed the circuit simulations based on the previously developed a-IGZO TFT model [11]. Table 1 represents design parameters of proposed pixel circuit. The channel width / length of all TFTs were fixed as 5$\mu$m / 5$\mu$m, respectively, except the driving TFT (T3) that had the channel width / length of 10$\mu$m / 5$\mu$m. The threshold voltage and mobility of all TFTs were set equally to 0.4 V and 10.1 cm$^2$/V·s, respectively. The storage capacitor was designed as 0.4pF. The OLED model used in the simulation consists of two junction diodes and two series resistors connected in parallel with a 3nF capacitor [12]–[14]. Note that though the proposed pixel circuit requires negative voltages to be supplied for switching TFTs and $PV_{DD}$, we expect that the conventional gate driver circuit can be adopted for
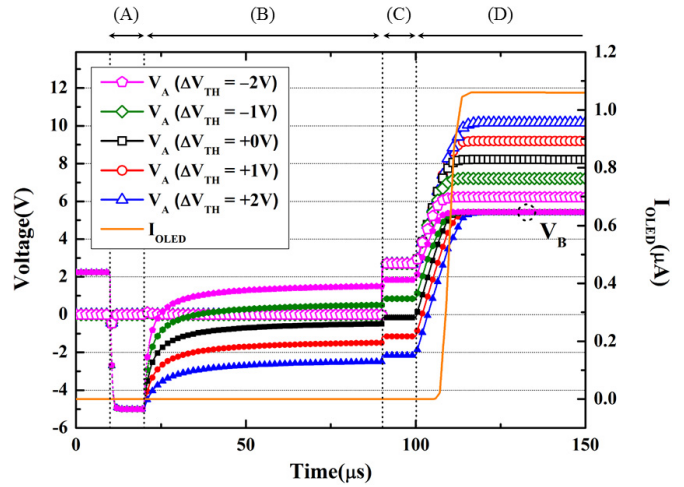
**FIGURE 3.** Simulated transient waveforms of the proposed circuit in four operation phases for different positive and negative $V_{TH}$ variations at $V_{DATA}$=2.7 V.
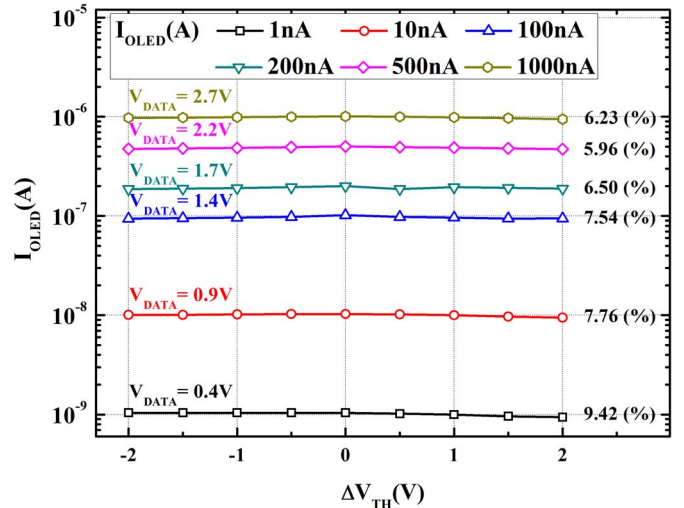
**FIGURE 4.** OLED current variations of the proposed circuit as a function of the threshold voltage shift varying from −2V to 2V.

generating negative voltages without any complication on the display driver.

Fig. 3 shows the time domain simulation results of the OLED current and gate-to-source node voltage of driving TFT (T3) when $V_{DATA\_H}$ was equal to 2.7 V. In the $V_{TH}$ detecting phase (B), node B was equal to the threshold voltage of T3 by the source follow operation. During the phase (C), the voltage at node A was accurately programmed to $V_{DATA\_H}$ while node B was not perturbed from the voltage of the previous phase. Finally, in the emission phase (D), since gate and source node voltages of T3 were increased equally by $V_{OLED}$, $I_{OLED}$ was maintained the same regardless of the threshold voltage variations, which is consistent with the current equation (2).

As shown in Fig. 4, when threshold voltage of T3 was shifted from −2 V up to 2 V the proposed circuit showed
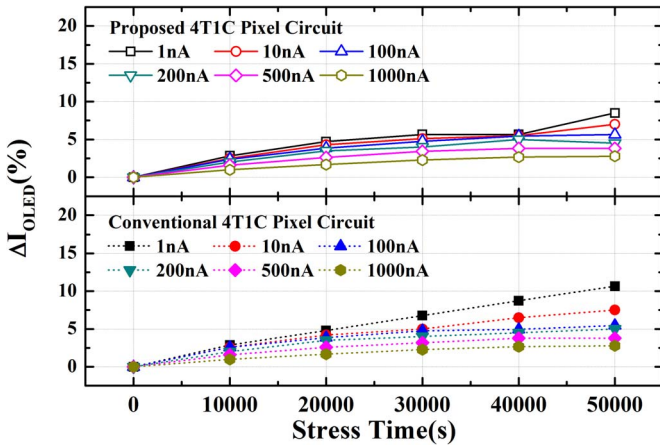
**FIGURE 5.** OLED current error rates of the proposed 4T1C pixel circuit as a function of OLED stress time in comparison to those of conventional 4T1C pixel circuit [18].
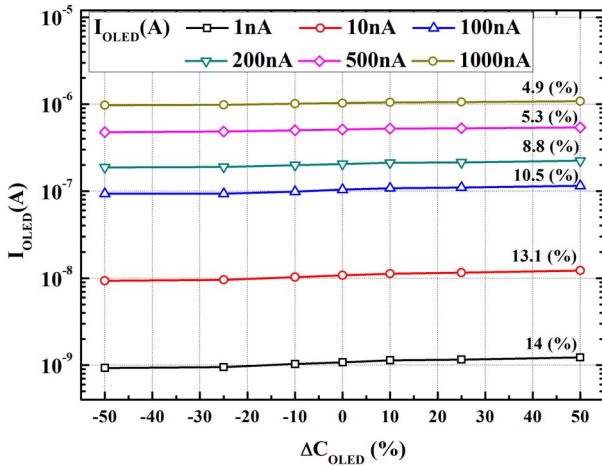


**FIGURE 6.** OLED current variations of the proposed circuit as a function of $C_{OLED}$ varying from −50 % to +50% of the initial value (= 3 nF).



**FIGURE 7.** Schematic layouts of: (a) the proposed pixel circuit and (b) the conventional pixel circuit with 4-TFTs and 1-capacitor [18].

good stability against threshold voltage variations over wide current range. More specifically, when the OLED current was high as $1 \mu A$, the maximum error rate was equal to 6.2%, while the OLED current was as low as 1nA, the maximum error rate was suppressed as 9.4%.

In order to verify the OLED current compensation of the proposed circuit, the turn-on voltage of OLED was intentionally varied for different levels of OLED current based on the OLED degradation model over increasing stress time [15], [16]. Then, we compared the performance of the proposed pixel circuit with the conventional 4T1C pixel circuit [18]. As shown in Fig. 5, when the OLED turn-on voltage was increased by 0.275V at 50,000 sec, the maximum OLED current variation of the proposed pixel circuit could be suppressed below 8.6% while that of the conventional 4T1C pixel circuit surpassed 10% for the low OLED current level. Therefore, we could confirm that the proposed pixel circuit could effectively compensate for the OLED degradation over a wide dynamic range of OLED currents
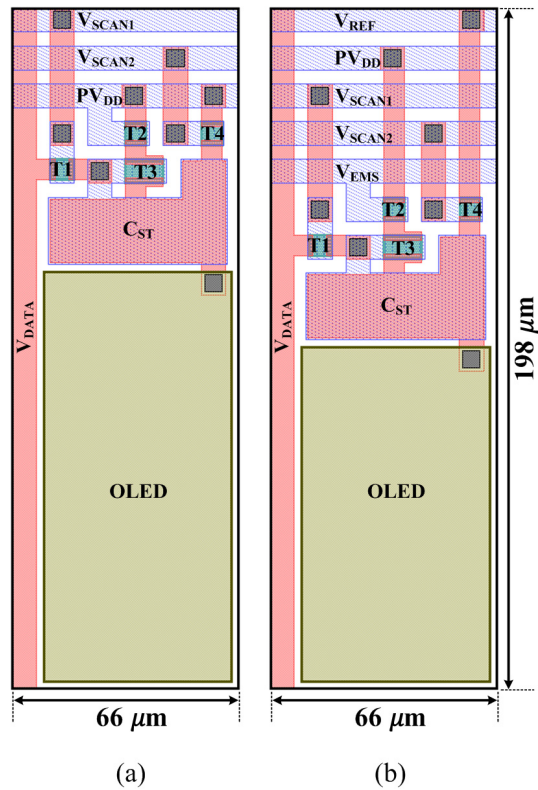
as predicted by Eq. (2). Although the proposed pixel circuit does not show significant improvement in the performance, it could reduce the number of signal lines to increase the aperture ratio by 9.7% in comparison to the 4T1C conventional pixel circuit with 7 voltage signal lines.

Furthermore, we performed the additional analysis on $I_{OLED}$ variation when $C_{OLED}$ was changed from −50% to +50% of the initial capacitance value (=3 nF) for different levels of $I_{OLED}$. As shown in Fig. 6, the maximum error rate of the OLED current could be maintained below 14% for ±50% capacitance variations. Therefore, the simulation results confirm that the OLED current of the proposed pixel circuit can be stably maintained and rarely perturbed by any possible $C_{OLED}$ variation caused by the fabrication process.

Fig. 7 (a) and (b) show the layouts of proposed and conventional 4T1C pixel circuits [18]. We performed the layout works for 13.3 inch in WXGA+ display using 4 $\mu m$ design rule. The sub-pixel size was set to 66×198 $\mu m$, and considered to be fabricated by 5-mask etch stop process [20]. As shown in Fig. 7, in the proposed pixel circuit, we could successfully eliminate two signal lines from the previous 4T1C circuit and accordingly the aperture ratio of the proposed circuit could increase up to 50.3%, compared to 41.0% aperture ratio of the conventional circuit.

Finally, we summarized key factors of the proposed pixel circuit in comparison to other pixel circuits in [17]–[19] as shown in Table 2. The summary confirms that our proposed

**TABLE 2. Key factors of the proposed pixel circuit in comparison to previous researches.**

| Parameter | Conventional 2T1C | Ref. [17] | Ref. [18] | Ref. [19] | This work |
|---|---|---|---|---|---|
| Active layer | All | a-Si a-InGaZnO | poly-Si | a-InGaZnO | a-InGaZnO |
| # of TFT | 2 | 3 | 4 | 5 | 4 |
| # of capacitor | 1 | 1 | 1 | 2 | 1 |
| # of signal line | 3 | 5 | 6 | 7 | 5 |
| $V_{TH}$ compensation | X | O | O | O | O |
| OLED compensation | X | X | O | O | O |

pixel circuit can provide the full compensation for the threshold voltage shift and the OLED degradation with less number of signal lines and TFTs. Through the enhanced aperture ratio, we expect that the resolution and brightness of the display could be improved while the display power consumption would be reduced at the same operating condition.

## IV. CONCLUSION

We proposed a novel voltage-programmed AMOLED pixel circuit using a-IGZO TFTs. We confirmed that the non-uniformity on the display image caused by $V_{TH}$ variation and OLED degradation could be compensated by using the proposed pixel circuit. At the same time, by reducing the number of signal lines from the circuit, we could achieve an improved aperture ratio on the single pixel circuit to be applied for low-power high-resolution AMOLEDs.

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