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Ferroelectric-Metal Field-Effect Transistor With Recessed Channel for 1T-DRAM Application

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ABSTRACT The ferroelectric-metal field-effect transistor with recessed channel (RC-FeMFET) is proposed for one transistor dynamic random-access memory (1T-DRAM). Through technology computer-aided design (TCAD) simulations, the effects of inter-metal insertion on the FeFET with recessed channel (RC-FeFET) is identified. By evaluating electric field (e-field) across interlayer (IL) and memory window (MW), the improvements of program/erase cycling endurance and read current sensing margin (RSM) are verified in the RC-FeMFET. Moreover, considering program voltage (V_W) and polarization switching time (τ_p), the guide line of the RC-FeMFET design is provided in terms of e-field across IL and MW for 1T-DRAM applications.

INDEX TERMS Ferroelectric-gate field-effect transistor (FeFET), Ferroelectric devices, one transistor dynamic random-access memory (1T-DRAM), endurance characteristics of FeFET, recess channel.

I. INTRODUCTION

One transistor dynamic random-access memory (1T-DRAM) has been extensively researched to overcome the scaling limitation of conventional one transistor-one capacitor (1T1C) DRAMs [1]–[5]. Especially, ferroelectric-gate field-effect transistors (FeFETs) have been considered as one of the strongest candidates because they are not only completely compatible with the fabrication process of existing DRAM cell transistors, but also fast program/erase speeds, a high on/off current ratio for stable read current sensing margin (RSM), and robust data retention are achievable [6], [7]. Typically, FeFETs have SiO_2 interlayer (IL)/hafnium zirconium oxide (HZO) ferroelectric layer (FE)/metal gate stacks where $\sim$ 1 nm IL is inevitable to suppress depolarization field and to maximize voltage drop across FE. Although the voltage drop is enhanced and program voltage (V_W) is reduced by thinning the SiO_2, the electric field (e-field) across the SiO_2 is still relatively high and comparable to the breakdown field of the SiO_2 layer, which limits the program/erase (P/E) cycling endurance to $< 10^6$ [7]–[11]. In this regard, for the commercialization of FeFETs as 1T-DRAM, the e-field across the SiO_2 IL (E_{IL}) should be minimized to obtain robust endurance characteristics without sacrificing the voltage drop over the FE [12], [13].

In order to obtain reduced E_{IL} and enhanced electric field across FE (E_{FE}), the researches on planar ferroelectric-metal field-effect transistors (FeMFET) with the area ratio between metal-ferroelectric-metal (MFM) capacitor and underlying MOSFET have also been conducted [14], [15]. Obviously, the planar FeMFETs decrease E_{IL} and increase E_{FE} simultaneously, which ensures robust endurance and wide memory window (MW). However, they have the disadvantage in terms of area scaling because the foot print of the planar FeMFETs is determined by the large area of the MOSFET. Thus, the novel device structure of FeMFETs is required to secure the

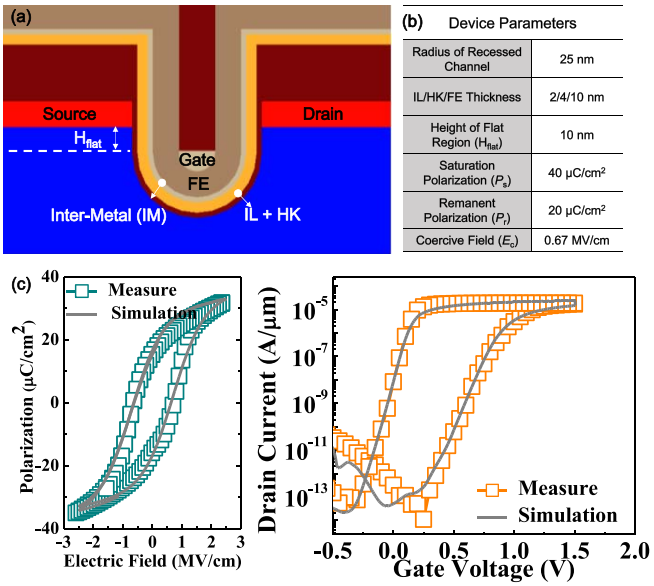

FIGURE 1. (a) The device structure of the ferroelectric-metal field-effect transistor with recessed channel (RC-FeMFET). (b) The device parameters used in technology computer-aided design (TCAD) simulations. (c) The calibration results for P-E curve of metal-ferroelectric-metal (MFM) capacitor and hysteretic drain current (I_D)-gate voltage (V_G) curve of planar FeFET.

high endurance and wide MW without sacrificing the foot print of the conventional DRAM cell transistors.

In this paper, the ferroelectric-metal field-effect transistor with recessed channel (RC-FeMFET) is proposed for 1T-DRAM applications. The RC-FeMFET is designed to secure three important advantages as a 1T-DRAM: 1) High performance, 2) Robust reliability, 3) Easy scalability, and 4) Complete process compatibility with those of conventional DRAM cell transistors. To verify the feasibility of the RC-FeMFET, technology computer-aided design (TCAD) simulations are performed with the calibrated device parameters by experimentally extracted electrical characteristics from the fabricated planar FeFET [16]. In particular, the effects of the metal insertion between IL/high-k dielectric layer (HK) and FE on MW, E_{IL}, V_W, and operation speeds are rigorously investigated.

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The device structure and fabrication method of RC-FeFET were demonstrated in our previous work [16]. Figs. 1(a)-(b) show the device structure of the proposed RC-FeMFET and the device parameters for SENTAURUS TCAD simulations. In the simulations, PhuMob and HighFieldSaturation are used as a mobility model, and Hurkx Band2Band and SRH are applied as a recombination model. The Preisach model parameters and physical thickness of IL/FE are referred from the previous research to reflect ferroelectric switching dynamics [16]. The Preisach model is expressed as follow.

$$P_{aux} = c \cdot P_s \cdot \tanh(w \cdot (E \pm E_c)) + P_{off} \quad (1)$$

where E is electric field, P_{aux} is auxiliary polarization and

$$w = \frac{1}{2F_c} \ln \frac{P_s + P_r}{P_s - P_r} \quad (2)$$

where P_s is saturation polarization, P_r is remanent polarization, E_c is coercive field. Fig. 1(c) shows the calibration result of polarization vs electric field (P-E) curve from metal-ferroelectric-metal (MFM) capacitor and hysteretic drain current (I_D)-gate voltage (V_G) curve from planar FeFET, which are used to determine the ferroelectric parameters of the Preisach model [16]. There might be discrepancy of the ferroelectric parameters between planar and non-planar structures. Even, it has been reported that the polarization of FE materials in curved structures [17] is enhanced compared to that in planar structures. That is, it means that the performance of FeFETs with curved structures is underestimated when the same device parameters are used. Therefore, to investigate the changes of device performances induced by a structural change, it is acceptable to use the same device parameters as those of the planar device for simulations of curved structures.

The key process flow of the proposed RC-FeMFET is depicted in Fig. 2. The RC-FeMFET can be fabricated by inserting an additional atomic layer deposition (ALD) intermetal layer (IM) between IL and FE (Fig. 2d). Here, to prevent the electron charging in the IM by tunneling current through IL, 4 nm of high-κ (HK) HfO_2 was inserted between IL and IM. Also, the buried gate can be constructed by an etch-back process after the chemical mechanical polishing (CMP) of the gate metal as shown in Fig. 2(e) [18], [19]. The buried gate structure is essential to alleviate the capacitive coupling between the source/drain and the IM in RC-FeMFET.

III. RESULTS AND DISCUSSION

In the previous study [16], the RC-FeFET was proposed to improve the endurance characteristic which is one of the critical problems for the commercialization of FeFETs. Although the wide MW by the enhancement of E_{FE} and reduced E_{IL} was achieved in the RC-FeFET, there are two limitations in terms of the device structure. 1) once the radius of recessed channel and the thicknesses of IL/FE are determined, the radius ratio [radius of IL (R_{IL})/radius of FE (R_{FE})] of FE and IL is not adjustable and the increase of the ratio is limited. 2) there is no benefit for the reduction of E_{IL} at the not-rounded region of the channel and thereby the flat region (the weakest region) can be the bottleneck to the endurance improvement. Although the height of the flat region (H_{flat}, shown in Fig. 1a) could be controlled by delicate dry-etching into the silicon substrate, the flat region cannot be perfectly removed by the variations of the dry-etching and source/drain dopants diffusion.

Here, the RC-FeMFET can solve both of these problems simultaneously by inserting IM between IL/HK and FE. Because the IM occupies the physical space in the recessed area without voltage drop, R_{FE} is diminished with

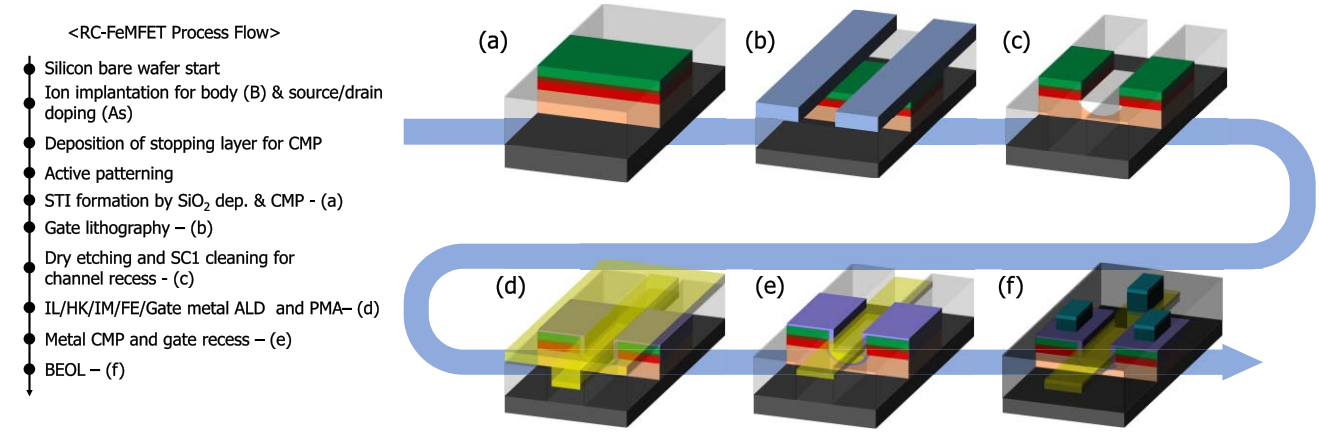

FIGURE 2. The schematic diagram of process flow of RC-FeMFET. The key processes are depicted on (a)–(f).

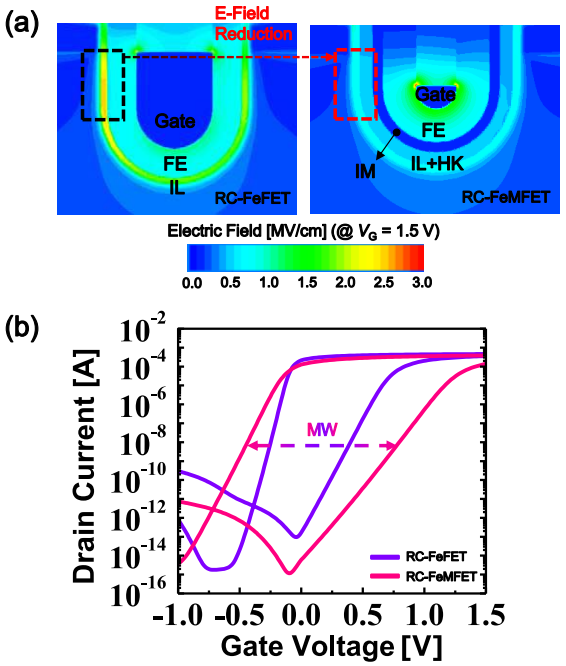

FIGURE 3. (a) The electric field (e-field) contours of conventional FeFET with recessed channel (RC-FeFET) and RC-FeMFET at gate voltage (V_G) = 1.5 V. The reduction of averaged e-field over IL (E_{IL}) is confirmed in RC-FeMFET. (b) The I_D-V_Gs curves of RC-FeFET and RC-FeMFET at 50 mV of drain voltage. The memory window (MW) of RC-FeMFET is wider than that of RC-FeFET.

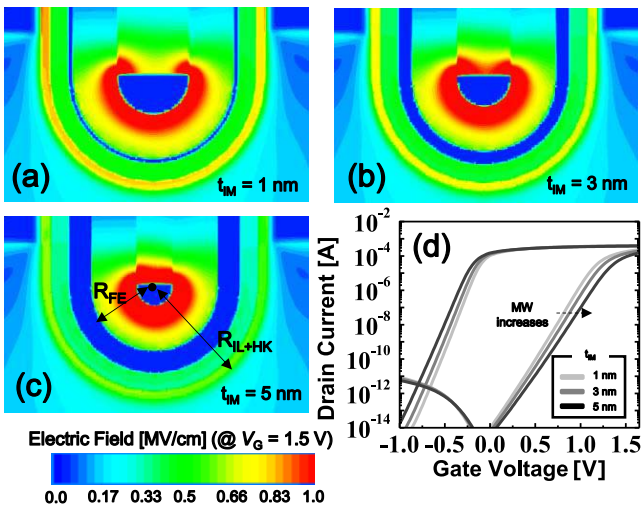

FIGURE 4. The e-field contours of RC-FeMFET with (a) 1 nm, (b) 3 nm, and (c) 5 nm of inter-metal layer thickness (t_{IM}). The thicker t_{IM} causes reduced E_{IL}. (d) The hysteretic I_D-V_Gs with respect to t_{IM}. The MW of RC-FeMFET is increased with the thicker t_{IM}.

unchanged R_{IL+HK} (namely, increasing radius ratio) and hence both E_{FE} enhancement and E_{IL} reduction are achievable (Fig. 3a) as compared to the RC-FeFET. The RC-FeFET with IL/HK/FE stacks is not analyzed since it can be easily expected that the MW is diminished by the reduced E_{FE} (namely, by voltage dividing between IL and HK) without the IM. Accordingly, the hysteretic I_D-V_Gs curves of Fig. 3(b) confirm that the RC-FeMFET has the wider MW than the RC-FeFET thanks to the enhanced E_{FE}. Also, it should be noted that the reduced E_{IL} is uniformly distributed over all the channel regions of the RC-FeMFET since the inserted IM should have equipotential. That is, in spite of the non-rounded part of the channel, the E_{IL} is averaged along the entire recessed channel and the weakest point for endurance disappears by the uniform distribution of the averaged E_{IL}.

As above-mentioned, the thickness of IM is the critical parameter which can significantly affect the electrical characteristics of the RC-FeMFET. It can be easily expected that R_{FE} is determined by eq. (1) once the radius of recessed channel and the thicknesses of IL/HK (t_{IL+HK})/IM (t_{IM}) are selected by considering the spatial restriction. It means that averaged E_{IL} and E_{IM} can be modulated by t_{IM}.

$$R_{FE} = R_{IL+HK} - t_{IL+HK} - t_{IM} \tag{3}$$

Figs. 4(a)–(c) depict the e-field contours with respect to t_{IM}. Expectedly, the E_{IL} is reduced and the E_{FE} is enhanced with the thicker t_{IM} based on the gauss law. The general gauss's

law in a spherical surface is defined as

$$\Phi_E = \oint \vec{E} \cdot dA = \frac{q}{\epsilon_0} \tag{4}$$

where $\vec{E}$ is electric field, A is area, q is elementary charge, and ε_0 is the vacuum permittivity, but in a cylindrical conductor, it can be summarized as follows.

$$E = \frac{\lambda}{4\pi\epsilon_0 R} \tag{5}$$

where λ is the line charge density, ε_0 is the vacuum permittivity and R is the distance from the conductor. In the case of the recessed channel FeFET, it has a cylinder-shaped gate cut in half and the radius of the FE (namely, distance from the conductor) is smaller than that of the IL+HK because the FE is deposited on top of the IL+HK. Accordingly, the electric field across the FE becomes larger than that over the IL since R_{FE} is smaller than R_{IL+HK}. Moreover, according to the Gaussian law described above, it is evident that the electric field near the top surface is larger. That is, the amount of polarization is changed with respect to the location of the FE layer, and the polarization near the top surface becomes larger. In the Preisach model, this effect is reflected because the polarization is determined by the electric field inside the FE. The planar channel FeFET do not have the distribution of polarization in the thickness direction of FE, whereas, for the recessed channel FeFET, it is observed that the polarization becomes larger as the FE is closer to the gate. The effect of the enhanced E_{FE} can be confirmed by the extended MW in Fig. 4(d). However, considering that the small R_{FE} change by $t_{IM} = 1$ nm makes the similar MW to that by $t_{IM} = 5$ nm, the improved MW of the RC-FeMFET (Fig. 3b) cannot be explained only by the E_{FE} enhancement. This can be understood by noticing that the potential of the IM in RC-FeMFET is uniformly distributed by the averaged E_{IL}/E_{FE} and thereby it has the uniform energy band along the channel. In contrast, the RC-FeFET has the non-uniform polarization and energy band distribution along the channel (Fig. 3a) and its threshold voltage is determined by the highest energy barrier [20]–[22], meaning that the larger V_G is required than the RC-FeMFET for the same MW. Therefore, it is proved that the improved MW of the RC-FeMFET results from the combination of the enhanced E_{FE} and the uniform E_{IL}/E_{FE} distribution by the IM introduction.

Fig. 5 shows the energy band diagrams of source-side gate dielectric stacks at $V_G = 3$ V. It is confirmed that the RC-FeMFET has the enhanced E_{FE} and reduced E_{IL} even at the source-side not-rounded region by the insertion of equipotential IM which causes uniform E_{IL}/E_{FE}. Here, it should be noted that charge trapping between FE and IL (RC-FeFET) and IM charging (RC-FeMFET) can also reduce MW and degrade endurance characteristics [8], [23]. In addition, power consumption can be increased by the gate leakage current based on direct tunneling via the thin IL, which must be considered in FeMFETs with IM. However, the insertion of HK not only inhibits IM charging caused by tunneling current, but also contributes to the E_{IL} reduction and E_{FE} enhancement [14], [15].

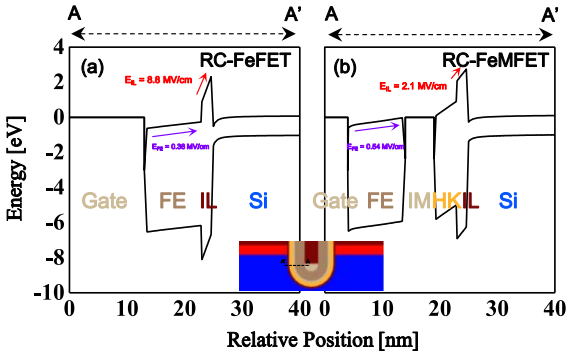

FIGURE 5. The energy band diagrams of (a) RC-FeFET and (b) RC-FeMFET across source-side gate stacks at $V_G = 3$ V. The E_{IL}s are 8.8 and 2.1 MV/cm for RC-FeFET and RC-FeMFET, respectively.

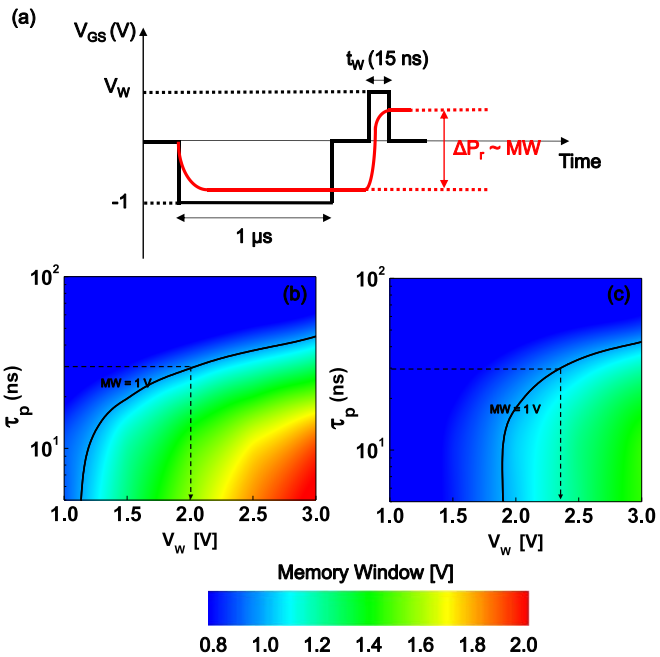

FIGURE 6. (a) The timing diagram of pulse program operation. The MWs of (b) RC-FeMFET and (c) RC-FeFET as functions of polarization switching time (τ_P) and V_W. The solid line indicates contour line which shows the correlation between τ_P and program voltage (V_W) required for 1 V of MW. The dotted line and arrow denote V_W required for 1 V of MW with 30 ns of τ_P.

To validate the feasibility of the RC-FeMFET to 1T-DRAM, pulse program operations are investigated considering write recovery time (t_{WR}) of DRAMs. Since the t_{WR} of state-of-art DRAM cell transistors is about 15 ns, the program pulse width (t_W) is set to 15 ns in this work [2], [24], [25]. Fig. 6(a) shows the timing diagram of the pulse program operation, where the difference of remanent polarization between programed and erased states (namely, $P_{up} - P_{down}$) is defined as ΔP_r. MWs are calculated from the ΔP of the pulse program by using the correlation between MW and ΔP extracted from the hysteretic $I_D - V_G$ characteristics. Figs. 6(b) and (c) indicate the

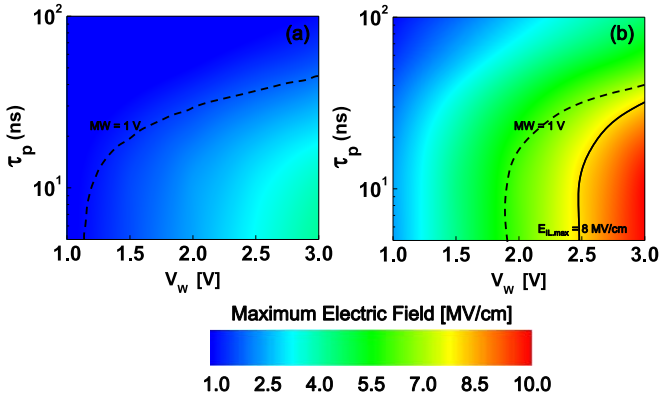

FIGURE 7. The maximum e-field across IL ($E_{IL.max}$) of (a) RC-FeMFET and (b) RC-FeFET as functions of τ_P and V_W. The solid and dotted lines indicate contour lines required for $E_{IL.max}$ = 8 MV/cm and MW = 1 V, respectively.

MWs of RC-FeMFET and RC-FeFET with respect to the polarization switching time (τ_P) and V_W, respectively. The MWs are extracted at $I_D = 10^{-9}$ A. The $V_W < 3$ V is used by considering the V_G of standard DRAM cells and the τ_P with the range from 5 to 100 ns is applied since HfO_2-based ferroelectric materials with $\tau_P < 10$ ns have been reported in previous studies [26]–[28]. It is observed that the range of τ_P and V_W required for MW > 1 V is much wider in RC-FeMFET than RC-FeFET (MW > 1 V is sufficient to achieve the RSM for stable 1T-DRAM operations). This implies that the RC-FeMFET needs the smaller V_W for the same MW. For instance, for MW of 1 V with $\tau_P = 30$ ns, the MW contours of Figs. 6(b)-(c) show that 2.0 V (RC-FeMFET) and 2.4 V (RC-FeFET) of V_W are required, respectively. This result proves that the RC-FeMFET is advantageous in terms of power efficiency as well.

To evaluate the design margin of the proposed RC-FeMFET, the maximum e-field across IL ($E_{IL.max}$) is also investigated since the $E_{IL.max}$ is the critical parameter directly related to the endurance characteristics of FeFETs. Figs. 7(a)–(b) show the $E_{IL.max}$ contours of RC-FeMFET and RC-FeFET as functions of V_W and τ_P, respectively. According to previous studies, the breakdown strength is between 8 and 10 MV/cm for the SiO_2 deposited by chemical vapor deposition (CVD) [29]. Thus, assuming that the 8 MV/cm is the $E_{IL.max}$ for stable P/E cycling endurance, the RC-FeMFET has the much wider design margin of V_W and τ_P (space between dotted and solid lines shown in Figs. 7a–b). Consequently, based on the contours of MW and $E_{IL.max}$, it is confirmed that high performance and reliability 1T-DRAM operations can be stably realized using the RC-FeMFET only by introducing IM to recessed channel device structure which is completely compatible with industry-standard DRAM cell transistors.

IV. CONCLUSION

In this letter, we propose the RC-FeMFET as the 1T-DRAM with high performance and robust reliability. The results of TCAD simulations provided that the wide MW of the RC-FeMFET comes from the combination of the enhanced E_{FE} and the uniform E_{IL}/E_{FE} distribution by the IM insertion. To verify the feasibility of the RC-FeMFET, the MW and E_{IL} are analyzed with $t_W = 15$ ns in terms of V_W and τ_P. As a result, it is found that high performance and endurance robust 1T-DRAM operations can be stably realized with the RC-FeMFET. Furthermore, the guide line of the RC-FeMFET device design is provided in terms of E_{IL} and MW with respect to V_W, t_W, and τ_P for 1T-DRAM applications

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