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Novel Boosting Scheme Using Asymmetric Pass Voltage for Reducing Program Disturbance in 3-Dimensional NAND Flash Memory

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ABSTRACT In this paper, novel boosting scheme using asymmetric pass voltage (V_{pass}) is proposed to obtain high channel boosting potential and to reduce program disturbance in 3-D NAND flash memory. The proposed scheme has the same program bias and timing conditions as conventional self-boosting except for V_{pass} voltages applied to both adjacent word-lines of selected word-line (WL_{sel}). Reduced V_{pass} ($V_{pass1} = V_{pass} - \Delta V$) is applied to previous word-line (WL_{n-1}) of WL_{sel} and increased V_{pass} ($V_{pass2} = V_{pass} + \Delta V$) is applied to next word-line (WL_{n+1}). In this scheme, the V_{pass1} cuts the channel off and causes local boosting when the channel potentials of inhibit strings are boosted up. Meanwhile, the V_{pass2} compensates the program speed reduction of selected cell ($cell_{sel}$) induced by the decreased voltage of the V_{pass1}. Through the measurements of program disturbance in fabricated devices, it is revealed that the program disturbance is significantly improved without the reduction of program speed by the proposed scheme. Furthermore, the V_{pass1} and V_{pass2} are optimized to maximize the improvement.

INDEX TERMS 3-D NAND flash memory, asymmetric pass voltage, local-boosting scheme, program disturbance.

I. INTRODUCTION

Program disturbance which eventually causes program failure in erase state is one of the key challenges to realize multi-bit NAND flash devices with reliable operation characteristics. Typically, the program disturbance consists of the disturbances by program voltage (V_{pgm}) and V_{pass}. The V_{pgm} disturbance occurs at the WL_{sel} of inhibit string, while the V_{pass} disturbance is generated by soft-program at the unselected WLs (WL_{unsel}) of program string. There is trade-off between V_{pgm} and V_{pass} disturbances because the higher V_{pass} enhances the channel boosting potential of inhibit string, whereas it accelerates the undesirable soft-program at the WL_{unsel}s of program string. Therefore, V_{pass} window margin in NAND flash can be defined as the error-free region for both V_{pgm} and V_{pass} disturbances as a function of V_{pass}. Many approaches have been discussed to improve the program disturbance [1]–[3]. Above all things, It has been considered that local-boosting scheme is one of the most effective methods to improve channel boosting potential and to reduce back-pattern dependency in inhibit string where unselected memory cells ($cell_{unsel}$) have various threshold voltages (V_{th}) [4]–[6].

However, in the local-boosting scheme, a relatively low voltage (V_{local}) compared to V_{pass} is required to cut-off the channel of inhibit string and a graded bias condition should be adopted to suppress the Gate Induced Drain Leakage (GIDL)-induced disturbance caused by the large potential difference between V_{local} and V_{pass} [7]–[10]. Moreover, to prevent the disturbance generated by Drain-Induced Barrier Lower (DIBL), Erase-Area Self-Boosting (ESAB) scheme has been used since it can reduce the potential difference between source-side

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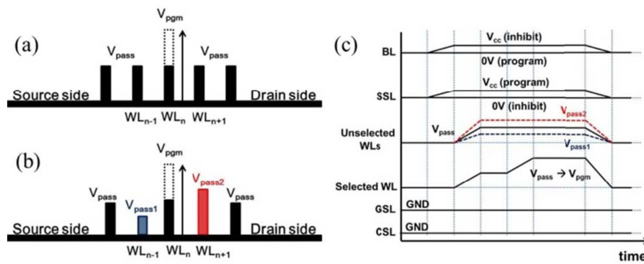

FIGURE 1. (a) Conventional self-booting scheme [3]. (b) Proposed asymmetric V_{pass} boosting scheme. (c) Timing condition that is used at proposed asymmetric V_{pass} boosting scheme.

and drain-side channels based on V_{local} during channel boosting [11]. Thus, the introduction of an additional low voltage generator circuit is inevitable and the increase of the channel potential by the local-boosting is reduced by the graded bias than expected.

In this letter, we propose the novel boosting scheme with the same bias and timing conditions as conventional self-boosting scheme except for V_{pass} voltages applied to both adjacent WLs of WL_{sel}. In the proposed scheme, WL_{n-1} cell ($cell_{n-1}$) can turn off and thus local boosting occurs by applying V_{pass1} with small voltage reduction (ΔV) from V_{pass} to WL_{n-1} without the introduction of an additional low voltage generator circuit and complex timing condition. Furthermore, the reduced program speed of $cell_{sel}$ by V_{pass1} can be completely compensated by applying V_{pass2} with increased ΔV to WL_{n+1}. From the TCAD simulations and the measurements of fabricated devices, the validity of the proposed boosting scheme is rigorously investigated.

II. EXPERIMENT

In order to clarify the program disturbance mechanisms, the measurements of fabricated devices are performed. The measured gate-stack type 3-D flash memory has thin tube-type polycrystalline silicon (poly-Si) body, gate dielectric stacks including SiN layer, and virtual source/drain. The cell string is similar to that of the p-BiCS structure [12], [13]. The gate length (L_g), space between vertical WLs, and tube diameter are all less than 100 nm. In 3-D NAND arrays, there are additional $cell_{unsel}$s that should be inhibited in different ways from conventional 2-D NAND arrays. Fig. 2(a) shows the inhibition cases of the $cell_{unsel}$s according to bit-line (BL) and string select line (SSL) gate biases. Among them, it has been reported that BL: 0V, SSL: 0V case ($cell_{INH2}$) has the worst program disturbance due to the leakage current flowing from boosted channel to BL [14]. The V_{th} of the $cell_{INH2}$ in erase state is extracted each time applying Incremental Step Program Pulse (ISPP) at 90 °C to analyze the program disturbance under the worst condition. $\triangle V_{pgm}$ of 0.5 V is used in the ISPP and all the V_{th}s are extracted by a constant current method at 5 x 10^{-9} A. Before the ISPP, erase (E), program1 (P1), program2 (P2), and program3 (P3) states are set to the V_{th}s of -2 V, -0.4 V, 1.3 V, and 3 V, respectively. To compare the proposed boosting scheme with the self-boosting scheme, the bias and timing conditions of Figs. 1(a) and (b) are used.

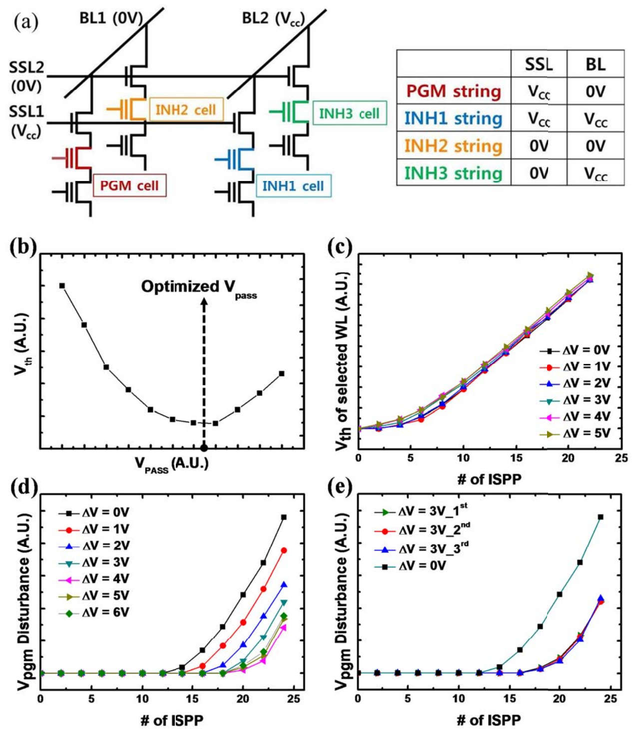

FIGURE 2. (a) Program and inhibition cases of 3-D NAND flash memory. (b) V_{pass} window optimization. V_{pass} window is extracted from one of center word lines by using conventional self-boosting method. (c) Measured program speed of $cell_{sel}$ in PGM string according to ΔV. (d) Measured V_{pgm} disturbance of $cell_{sel}$ in INH2 string according to ΔV. (e) Repeatability of V_{pgm} disturbance improvement in proposed boosting scheme with ΔV of 3 V.

III. RESULTS AND DISCUSSION

Firstly, V_{pass} is optimized through V_{pass} window measurements as can be seen Fig. 2(b). The V_{pass} window is extracted by using self-boosting scheme after block erase. Then, the effects of V_{pass1} and V_{pass2} with various ΔVs on the V_{pgm} disturbance of the $cell_{INH2}$ are measured after block erase. Note that the proposed scheme is the same as self-boosting scheme in the case of $\Delta V = 0$ V. Fig. 2(d) shows that the disturbance gets improved with the increased ΔV and the disturbance is no longer improved from $\Delta V = 5$ V. Over $\Delta V = 5$ V, the disturbance starts to be degraded slightly. To clarify the disturbance improvement, the V_{pgm} disturbance is measured repeatedly with ΔV of 3 V. Fig. 2(e) shows that the reduction of the V_{pgm} disturbance appears repeatedly. Furthermore, Fig. 2(c) indicates that the program speed of the $cell_{sel}$ in the program string is nearly unchanged regardless of ΔV because the reduced ΔV of the V_{pass1} is completely compensated by the increased ΔV of the V_{pass2}. Thus, the improved disturbance characteristics should result from the enhancement of the boosted channel potential by the proposed scheme.

To investigate the change of the disturbance as a function of the ΔV, TCAD simulations are carried out by using Synopsys Sentaurus. Figs. 3(a) and (b) show the simulated cross-sectional structures of 3-D NAND flash memory which

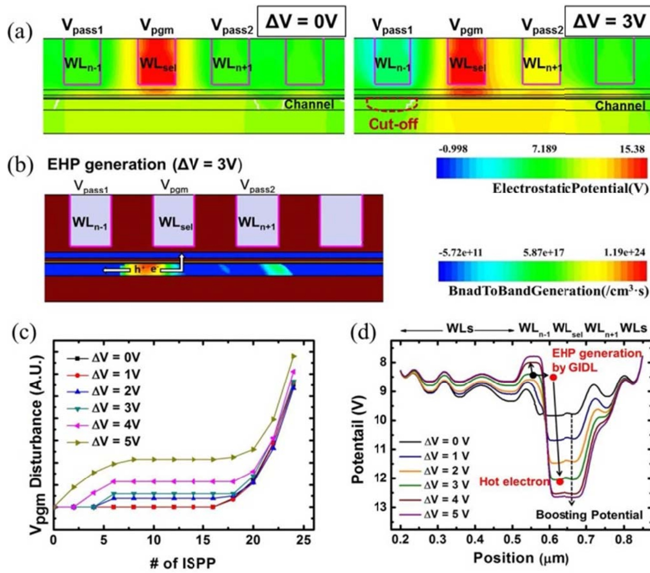

FIGURE 3. Figures are cross-sectional and half images of tube-type 3-D NAND flash memory with gate-all-around (GAA) structure. (a) Simulation results show that higher channel potential can be obtained when the proposed boosting scheme is applied with proper ΔV. (b) Electron-hole pair generated between WL_{sel} and WL_{n-1}. (c) Measured V_{pgm} disturbance of WL_{sel} in INH2 string according to ΔV with WL_{n-1} of P3 state. (d) Potential profile according to channel direction and illustration of hot-carrier disturbance at WL_{sel}.

are composed of nine WLs, one SSL, and one ground select line (GSL) for simplicity. Program operations are simulated under the bias and timing conditions of Figs. 1(a) and (b) after block erase. Figs. 3(a) show that the channel potential beneath the $cell_{sel}$ is more boosted as the V_{pass1} becomes deceased. This phenomenon can be explained by the fact that the turn-off condition of the $cell_{n-1}$ (V_{pass1} − channel potential of $cell_{n-1}$ < V_{th} of $cell_{n-1}$) is achievable when V_{PGM} pulse is rising and the channel potential of the $cell_{n-1}$ is boosted up by the V_{PGM} as can be seen in Figs. 3(a). Consequently, the stronger turn-off of the $cell_{n-1}$ occurs and thus the channel potential of the $cell_{sel}$ becomes increased with the reduced V_{pass1}.

To investigate the influence of the $cell_{n-1}$ V_{th} on the V_{pgm} disturbance under the proposed boosting scheme, the $cell_{n-1}$ in the inhibit string is set to P3 state and then the disturbance of the $cell_{sel}$ is monitored throughout the ISPP (ΔV = 0 V is used during the V_{th} setting of the $cell_{n-1}$ to exclude the effects of the V_{pass} disturbance by V_{pass2} on the V_{pgm} disturbance of the $cell_{sel}$). Fig. 3(c) indicates that the disturbance is nearly unchanged according to the V_{pass1} reduction and then the disturbance starts to be degraded from ΔV = 3 V as the $cell_{n-1}$ has P3 state. The degradation of the disturbance over ΔV = 3 V can be understood by the GIDL-induced electron-hole pair (EHP) generation between WL_{n-1} and WL_{sel} as depicted in Fig. 3(b). The energy band diagram of Fig. 3(d) presents that the EHP is easily generated by the $cell_{n-1}$ with the high V_{th} (P3 state) as compared to when the $cell_{n-1}$ has the low V_{th} (E state). The electrons

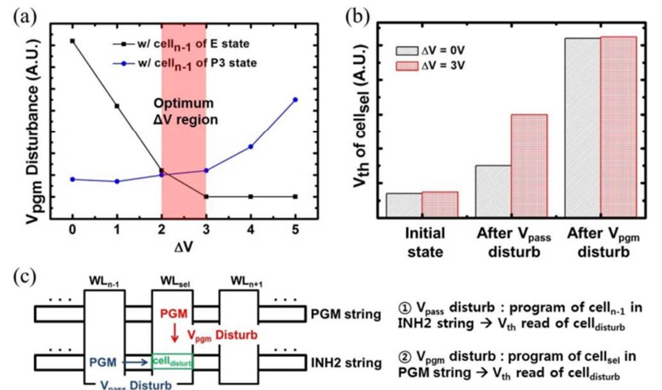

FIGURE 4. (a) Measured ΔV window as a function of ΔV. (b) V_{th} change of $cell_{sel}$ by series of disturbance consisting of V_{pass} and V_{pgm} disturbances. (c) Diagram that explains how $cell_{sel}$ V_{th}s of Fig. 4(b) are extracted.

of the generated EHP are accelerated by the large potential difference between the $cell_{n-1}$ (P3 state) and the $cell_{sel}$ and can obtain enough energy to be injected into the storage node of the $cell_{sel}$ [7]. Thus, it can be expected that the degradation of the disturbance over ΔV = 3 V results from the GIDL-induced HCI caused by the combination of the strongly turn-off $cell_{n-1}$ and the highly boosted channel potential.

When considering the correlation between the V_{th} and the turn-off condition of the $cell_{n-1}$, it can be simply noticed that both the sensitive disturbance degradation and the insensitive disturbance improvement to the V_{pass1} reduction are because the $cell_{n-1}$ turns off enough and the GIDL-induced HCI occurs at a relatively high V_{pass1}. Hence, the ΔV of V_{pass1} and V_{pass2} is optimized by considering the V_{th} of the $cell_{n-1}$. Fig. 4(a) demonstrates that the optimized ΔV is determined at the ΔV (ΔV = ∼3 V) where the disturbance at the $cell_{n-1}$ of E state (Channel boosting limitation) and that at the $cell_{n-1}$ of P3 state (GIDL-induced HCI limitation) are simultaneously minimized.

Finally, the effects of the V_{pass} disturbance by the V_{pass2} on the V_{pgm} disturbance of the $cell_{disturb}$ are checked by programing the $cell_{sel}$ in the program string after setting the V_{th} of the $cell_{n-1}$ in the inhibit string to P3 state with ΔV = 3 V and ΔV = 0 V, respectively. Fig. 4(b) shows that the V_{th} change of the $cell_{disturb}$ by the V_{pass2} cannot affect the V_{th} after finishing the programing although the $cell_{disturb}$ experiencing the V_{pass2} with ΔV = 3 V has the higher V_{th} due to the V_{pass} disturbance before the programing (the $cell_{sel}$ in the program string is programed to P3 state by using the proposed boosting scheme with the optimized ΔV = 3 V). This means that the program disturbance is determined only by the boosting potential otherwise the V_{th} of the $cell_{disturb}$ is too much increased by the V_{pass} disturbance before the programing (namely, in Fig. 4(b), V_{th} of $cell_{disturb}$ at After V_{pass} disturb < V_{th} of $cell_{disturb}$ at After V_{pgm} disturb). Thus, the optimized ΔV = 3 V is valid despite of the high V_{pass2}.

Additionally, it should be noted that the same ΔV for V_{pass1} and V_{pass2} is used to compare the program disturbance of the proposed boosting scheme to that of the conventional self-boosting at the same program speed because asymmetric ΔV makes the program speed slow or fast by the coupling between V_{PGM} and V_{pass1}/V_{pass2}. However, the different ΔVs for V_{pass1} and V_{pass2} can be used to improve the program disturbance. For example, in the case of $\Delta V = 3V$, the ΔV of V_{pass2} can be increased with the fixed V_{pass1} ΔV of 3 V in the range that the V_{pass} disturbance by V_{pass2} is smaller than the V_{pgm} disturbance after programing and the GIDL-induced disturbance is smaller than the disturbance determined by channel boosting. Furthermore, the proposed scheme can be also applied to 2-D NAND. However, compared to 3-D NAND with thin poly channel, the boosting potential of 2-D NAND is lower because 2-D NAND has bulk silicon channel. Thus, the proposed boosting scheme is more effective in 3-D NAND as the high channel boosting potential easily turns off the $cell_{n-1}$.

IV. CONCLUSION

In this study, we propose a novel boosting scheme with the same bias and timing conditions as conventional self-boosting scheme except for the V_{pass} voltages applied to both adjacent WLs of WL_{sel}. From TCAD simulations and the measurements of fabricated devices, it is verified that the $cell_{n-1}$ can turn off and thus local boosting occurs by applying the V_{pass1} with small ΔV reduction to WL_{n-1}. Furthermore, the reduced program speed of the $cell_{sel}$ by the V_{pass1} can be completely compensated by applying the V_{pass2} with increased ΔV to WL_{n+1}.

The ΔV of V_{pass1} and V_{pass2} is optimized by considering the V_{th} of the $cell_{n-1}$ and the V_{pass} disturbance to maximize the improvement. As a result, $\Delta V = 3$ V is determined as the optimized ΔV that can minimize both the disturbance limited by the boosting potential and that by the GIDL-induced HCI.

REFERENCES

[1] K. Takeuchi, S. Satoh, K. Imamiya, and K. Sakui, "A source-line programming scheme for low-voltage operation NAND flash memories," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 672–681, May 2000.
[2] T. Cho *et al.*, "A dual-mode NAND flash memory: 1-Gb multilevel and high-performance 512-Mb single-level modes," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1700–1706, Nov. 2001.
[3] J. Lee *et al.*, "A 90-nm CMOS 1.8-V 2-Gb NAND flash memory for mass storage applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1934–1942, Nov. 2003.
[4] T.-S. Jung *et al.*, "A 3.3 V 128 Mb multi-level NAND flash memory for mass storage applications," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, 1996, pp. 32–33.
[5] J.-K. Kim, H.-B. Pyeon, H. Oh, R. Schuetz, and P. Gillingham, "Low stress program and single wordline erase schemes for NAND flash memory," in *Proc. IEEE Non Volatile Semicond. Memory Workshop (NVSMW)*, Monterey, CA, USA, 2007, pp. 19–20.
[6] K.-T. Park *et al.*, "Dynamic vpass controlled program scheme and optimized erase Vth control for high program inhibition in MLC NAND flash memories," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2165–2172, Oct. 2010.
[7] J.-D. Lee *et al.*, "A new programming disturbance phenomenon in NAND flash memory by source/drain hot-electrons generated by GIDL current," in *Proc. IEEE Non Volatile Semicond. Memory Workshop*, Monterey, CA, USA, Feb. 2006, pp. 31–33.
[8] S. J. Joo *et al.*, "Abnormal disturbance mechanism of sub-100 nm NAND flash memory," *Jpn. J. Appl. Phys.*, vol. 45, no. 8A, pp. 6210–6215, Aug. 2006.
[9] K.-T. Park, S. Lee, J.-S. Sel, J. Choi, and K. Kim, "Scalable word-line shielding scheme using dummy cell beyond 40 nm NAND flash memory for eliminating abnormal disturb of edge memory cell," *Jpn. J. Appl. Phys.*, vol. 46, no. 4B, pp. 2188–2192, Apr. 2007.
[10] T. Melde *et al.*, "Select device disturb phenomenon in TANOS NAND flash memories," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 568–570, May 2009.
[11] D. Oh *et al.*, "Program disturb phenomenon by DIBL in MLC NAND flash device," in *Proc. IEEE Non Volatile Semicond. Memory Workshop*, Opio, France, 2008, pp. 5–7.
[12] R. Katsumata *et al.*, "Pipe-shaped BiCS flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices," in *VLSI Symp. Tech. Dig.*, Honolulu, HI, USA, 2009, pp. 136–137.
[13] E.-S. Choi and S.-K. Park, "Device considerations for high density and highly reliable 3D NAND flash cell in near future," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2012, pp. 9.4.1–9.4.4.
[14] H. Yoo *et al.*, "Modeling and optimization of the chip level program disturbance of 3D NAND flash memory," in *Proc. IEEE Int. Memory Workshop*, Monterey, CA, USA, 2013, pp. 147–150.

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