Process enabling highly accurate die position for fan-out package applications

H.-P. Park and Y.-H. Kim✉

A new process that can improve die shift issue in process utilising back-sided under bump metallurgy (UBM) via a self-alignment effect for fan-out package applications is proposed. The die and the pad of the substrate are spontaneously aligned and the degree of accuracy is very high after reflow. For the experiment, two kinds of UBM pads were prepared on glass dies and the SAC305 solder was formed on the copper pads of an frame retardent (FR)-based substrate. The die shift value was from 20 to 50 μm after pick-and-placement. After reflow, the maximum die shift value was <1 μm. An initially misaligned die with a large shift was aligned with a high degree of accuracy during reflow due to the surface tension of the molten solder. The proposed process improves the die shift issue in the fabrication of fan-out wafer-level packaging and the active die embedded substrate.

Introduction: The next generation of products – with their improved performance, diverse functionality, thinner body outline, and longer battery life – will bring great advantages to the mobile and automotive industries. To maximise their utility in various applications, these advanced products require appropriate packaging technologies that ensure greater performance, lower costs, a smaller form factor, and a higher level of integration. To satisfy this trend, wafer-level packaging (WLP) technologies such as micro-bumping, fine pitch bonding technologies, and redistribution layers (RDLs) have received more attention due to WLP's competitive finer resolution for signal distribution and its shorter interconnection length for high input/output pin counts. These characteristics make it possible to satisfy the requirements of various advanced products [1]. Typically, WLP is called fan-in WLP, in which the die area is the same as the package area; therefore, the pin count is limited by the die size. Owing to these limitations, fan-in WLP has been applied to low-end products having a small pin count. Fan-out WLP (FOWLP) has emerged in order to overcome the pin count limitation of fan-in WLP. In FOWLP, an artificial wafer is fabricated first, in which known good dies (KGDs) are placed with large margins between them, so that the extended area between the KGDs is utilised to redistribute the pin count. Furthermore, FOWLP can enable a smaller and thinner form factor, and an improved electrical and enhanced thermal performance [2].

However, manufacturing issues such as wafer warpage or a die shift during the process have limited the widespread adoption of FOWLP technology. The wafer warpage issue can be improved by adopting low shrinkage compounds or by matching the coefficient thermal expansion properties of the compounds considering the population or thickness of the die on a temporary carrier [3]. However, die shift issue during the process is not straightforward. The die shift issue can occur when the die-attach machine pick-and-places the die with a certain degree of tolerance and the attached die is then shifted by compressive stress during wafer moulding [4]. Several papers describe improvements in die shift issue during the process [5, 6]. Even though previous studies show an improvement in the die shift issue during the process, the total shift value was still in the range of 30–45 μm and a subsequent RDL process was required for a more accurate position of the die to interconnect the die pad with an RDL via. Moreover, the scalability of the RDL is getting finer and the RDLs are approaching a 2/2 μm line width and line spacing [7]. Therefore, minimising the die shift value is very important for the advanced device packaging by FOWLP technology.

To improve the die shift issue in FOWLP, we propose a new process utilising the self-alignment of molten solder by employing under bump metallurgy (UBM) on the rear side of the chip. The metal pad on the carrier and the solder that formed on either a back-sided UBM or a metal pad is matched. This self-alignment has been widely applied to flip-chip bonding [8]. Our approach is to improve the alignment accuracy by utilising the flip-chip self-alignment effect. Our newly proposed process consists of the wafer and assembly processes. In the wafer process, a copper (Cu)-pillar bump is first fabricated on the active side, and then the wafer is back-grinded to reduce wafer thickness. The UBM pad is formed on the back side of the die by the thin film deposition and lithography method. The fabricated UBM pad is used as a solder wetting layer during reflow. After the wafer preparation, the assembly process occurs. Individual KGDs are sliced and pick-and-placed on the substrate utilising a back-sided UBM pad with the dies in the face-up direction during reflow. In addition, the encapsulation process is performed by a film-assisted moulding method to protect the Cu-pillar bump from the moulding compounds and to interconnect the RDL via. After this, the RDL and the solder bump formation processes are performed. Finally, the singulation process is carried out for individual packages. Schematic images of our proposed process and structure are depicted in Fig. 1.

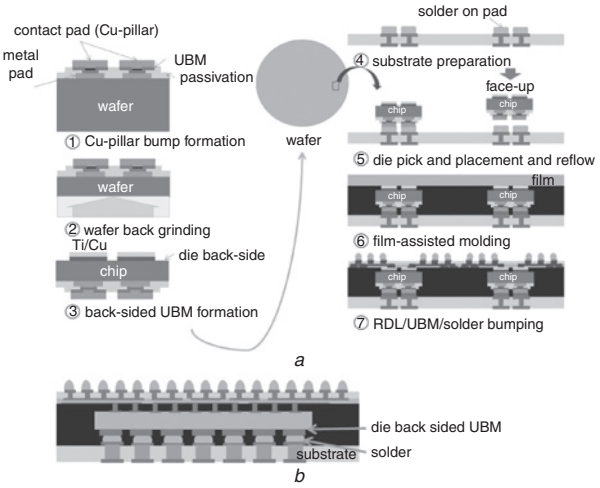

Fig. 1 *Schematic images of proposed process and vertical structure*

a Proposed process utilising back-sided UBM of flip-chip
b Schematic images of vertical structure utilising back-sided UBM for FOWLP

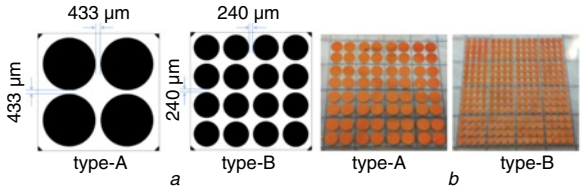

Fig. 2 *Mask design for UBM patterns and their optical images after fabrication*

a Respective UBM patterns for sample types (I) and (II) were designed in circle shape and their *x/y* directions of pattern pitch have same degrees (i.e. type-A is 433 μm and type-B is 240 μm)
b Optical images of UBM patterns on glass die after fabrication

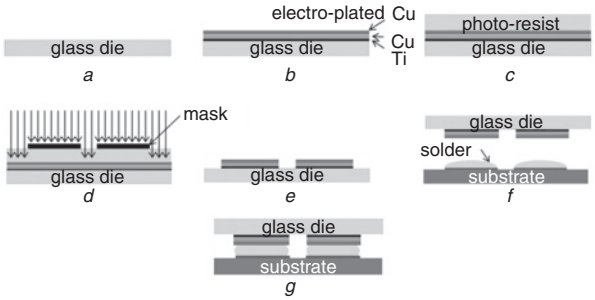

Fig. 3 *Sample fabrication process for experiment*

a Preparation of glass chip
b Ti and Cu thin films deposited on glass chip and Cu layers formed by electroplating
c Photoresist was spin-coated
d Photoresist was exposed and developed using photomask
e Wet etching process was performed by using chemical etchant and Cu and Ti layer was removed
f Glass chip pick-and-placement on substrate
g Reflow process for good wettability and self-alignment of chip position in substrate

Experiments and fabrication: Design of the masks for UBM patterns of types A and B are shown in Fig. 2. The triangle-shaped alignment marks are also located on the die edge to measure the distance between the UBM pad and the fiducial mark on PCB after reflow. The designed patterns and alignment marks were fabricated on a transparent glass

die for optical inspection and measurement. The glass die was prepared by using photolithography, sputtering, and Cu electroplating. Titanium (Ti) (0.05 μm) and Cu (1 μm) thin films were deposited on a glass die as a seed layer for UBM using a DC magnetron sputtering system without breaking the vacuum of the chamber. After the seed layer was deposited on the glass die, 3-μm-thick Cu layers were formed by electroplating and the photoresist was spin-coated, exposed, and developed. The wet etching process was then performed by using a chemical etchant to sequentially remove the Cu and Ti layer. After this, the UBM pads and alignment marks were formed on the glass die. The substrate for assembly is composed of FR-4-based PCB and it was plated in Cu for the metal pad. The SAC305 solder was printed on the Cu pads. The printed solder was reflowed to form 30 μm heights with hemispherical bumps. A fabricated glass die was aligned with the metal pads on the substrate using a flip-chip bonder and all solder joints were made simultaneously during the reflow process at 260°C. The fabrication process for the experiment is shown in Fig. 3.

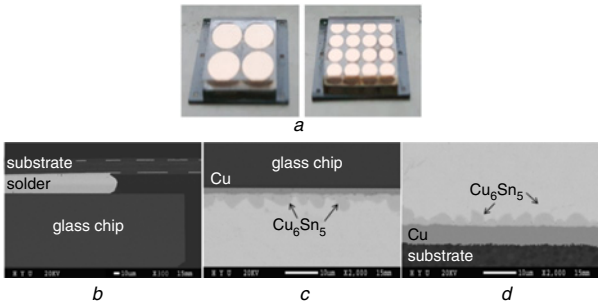

Fig. 4 *Optical and cross-sectional BSE-SEM images after flip-chip bonding*

a Optical microscope images after flip-chip bonding
b Cross-sectional SEM image of flip-chip bonding area
c and *d* Magnified SEM image of Fig. 4*b* showing Cu_6Sn_5 IMC in SAC305/solder interfaces for glass die and substrate side

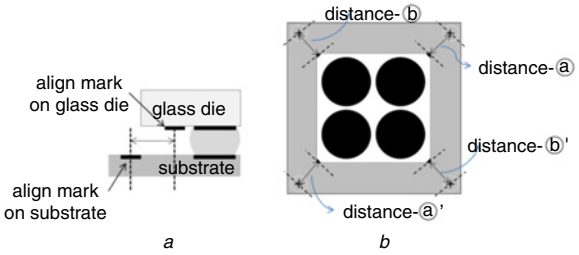

Fig. 5 *Side- and top-view images showing measurement position of die in substrate for die degree of misalignment on one glass chip in substrate*

a Side-view image showing measurement position
b Plan-view image showing four-corner distance of pattern to pattern between glass die and substrate. For perfect centering in substrate unit position, four-corner distances must have same degree (i.e. distance – ⓐ = ⓐ′ = ⓑ = ⓑ′)

Results and discussion: Fig. 4*a* shows optical microscope images after the flip-chip bonding process and the UBM pad and alignment marks are clearly visible through the transparent dies. The cross-sectional back-scattered electron-scanning electron microscopy (BSE-SEM) image in Fig. 4*b* shows the overall flip-chip bonded area between the glass die and the solder on the pad in the substrate. The fabricated glass die was successfully bonded with solder on the pad in the substrate after reflow. From the magnified images in Figs. 4*c* and *d*, the Cu_6Sn_5 intermetallic compound (IMC) was observed at both interface areas: the Cu pad on the glass die side and the solder on the Cu pad on the substrate side. The presence of intermetallic phases in a joint area is an indication of good wetting at the substrate/solder interface during reflow. This result suggests that the soldering process has formed a good bond between the die and the substrate. As shown in Fig. 5, the distance between the four-cornered alignment mark on the glass die and the corresponding cross-shaped alignment mark on the substrate can be determined accordingly. Table 1 summarises the results of the die shift value from the four-corner position distance according to the before and after reflow processes. Before reflow, both types A and B show a wide range of die shift values and their degree ranged from 30 to 50 μm. After reflow, both types A and B show that the degree of die shift was within ±1 μm. In a comparison of types A and B, type-A shows a lower value and the average value of both types was 0.46 μm. That is, the liquid-phase molten solder reacts with the UBM pad and the molten solder reduces the surface tension during reflow. Their corresponding reaction pads can then be aligned with a highly accurate alignment.

Table 1: Results of die shift value from four-corner position distance according to before and after reflow processes

Sample	Die shift value (μm)		
	Before reflow	After reflow	
	Average	Average	Max
Type-A	42.6 ± 7.8	0.46 ± 0.1	0.60
Type-B	33.1 ± 4.3	0.86 ± 0.1	0.90

Summary: We propose a new process using back-sided UBM to improve the die shift issue for FOWLP, and experimentally demonstrate the alignment enhancement. The experimental results correlated with the self-alignment phenomenon in flip-chip soldering. It was found that the maximum die shift value was <±1 μm. This process enabled the dies to align spontaneously on a pad of substrate without any highly accruable die-attach equipment. Furthermore, our process also can be extended to fabricate the panel-level fan-out (FO)-packages to prevent the loss of expensive dies by only placing them on a good site and fabricating the active die embedded substrates.

Acknowledgment: This research was supported by a Semiconductor Industry Collaborative Project between Hanyang University and Samsung Electronics Co. Ltd.

Submitted: *2 February 2017* E-first: *11 May 2017*
doi: 10.1049/el.2017.0357
One or more of the Figures in this Letter are available in colour online.

H.-P. Park and Y.-H. Kim (*Division of Materials Science & Engineering, Hanyang University, Seoul 133-791, Republic of Korea*)

✉ E-mail: kimyh@hanyang.ac.kr

References

1 Liu, P., Wang, J., Tong, L., *et al.*: 'Advances in the fabrication process and applications of wafer level packaging', *J. Electron. Packag.*, 2014, **136**, pp. 1–7
2 Tseng, C.-F., Liu, C.-S., Wu, C.-H., *et al.*: 'In FO (wafer level integrated fan-out) technology'. Proc. IEEE 66th Electronic Components and Technology Conf., Las Vegas, NV, USA, May–June 2016, pp. 1–6
3 Che, F.X., Ho, D., Ding, J.P., *et al.*: 'Modeling and design solutions to overcome warpage challenge for fan-out wafer level packaging technology'. Proc. IEEE 17th Electronics Packaging Technology Conf., Singapore, December 2015, pp. 1–8
4 Eric Kuah, T.H., Hao, J.P., Yin, M., *et al.*: 'Encapsulation challenges for wafer level packaging'. Proc. IEEE Microelectronics and Packaging Conf., Singapore, December 2009
5 Mazuir, J., Olmeta, V., Yin, M., *et al.*: 'Evaluation and optimization of die-shift in embedded wafer-level packaging by enhancing the adhesion strength of silicon chips to carrier wafer'. Proc. IEEE 13th Electronics Packaging Technology Conf., Singapore, December 2011, pp. 747–751
6 Khong, C.H., Kumar, A., Zhang, X., *et al.*: 'A novel method to predict die shift during compression molding in embedded wafer level package'. Proc. IEEE Electronic Components Technology Conf., San Diego, CA, USA, May 2009, pp. 535–541
7 Liu, F., Kubo, A., Nair, C., *et al.*: 'Next generation panel-scale RDL with ultra small photo vias and ultra-fine embedded trenches for low cost 2.5D interposers and high density fan-out WLP''. Proc. IEEE Electronic Components Technology Conf., Las Vegas, NV, USA, May–June 2016, pp. 1157–1522
8 Humpston, G., and Jacobson, D.M.: 'Principles of soldering' (ASM International, The Materials Information Society, Materials Park, OH, USA, 2004)