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Design of Half-Bridge Switching Power Module Based on Parallel-Connected SiC MOSFETs for LLC Resonant Converter with Symmetrical Structure and Low Parasitic Inductance

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Abstract: SiC MOSFETs are used in many power conversion applications because of their superior characteristics, such as fast switching speed, low on-resistance, and high operating temperature. In certain high-power systems, SiC MOSFETs are connected in parallel to enhance their current capacity and power efficiency. However, compared with Si-based devices, the current imbalance caused by the parasitic inductance difference becomes more severe when driving SiC MOSFETs in parallel, owing to the fast switching speed. Furthermore, the power loop inductance imbalance that occurs when constructing a half-bridge with parallel SiC MOSFETs has rarely been addressed in previous studies. In this study, a half-bridge switching power module based on parallel-connected SiC MOSFETs is proposed to solve the current imbalance through a symmetric structure of the gate and power loops. The effects of the magnitude and imbalance of the gate and power loop inductances in the half-bridge structure based on parallel-connected devices are also explained. A detailed printed circuit board layout of the proposed switching power module is provided, and the inductance symmetry is verified through simulations. A double-pulse test is conducted to verify the current-balancing capability of the proposed switching power module. In addition, an LLC resonant converter is designed using the proposed switching power module, and the power loss between parallel SiC MOSFETs is compared. The experimental results indicate the total power loss error between the parallel-connected SiC MOSFETs of the proposed power module is only 1.94%.

Keywords: current-balancing; parasitic inductance; parallel operation; PCB layout; SiC MOSFET

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1. Introduction

Silicon carbide (SiC) power semiconductors have excellent characteristics such as a high breakdown field, high thermal conductivity, low on-resistance, and fast switching speed compared to those of silicon (Si) power semiconductors [1–7]. Owing to these advantages, SiC power semiconductors are employed in various applications, such as in electric vehicle chargers [8–10], multilevel inverters [11], induction heaters [12], fuel cell systems [13], and wireless power transmission [14].

The recent developments in power electronics technology have significantly increased the demand for higher-power-level switching devices. Despite the gradual increase in the capacity of switching devices, it remains insufficient to meet the burgeoning market demand. Against this backdrop, there has been a marked surge in interest towards the technology of parallel connection for switching devices. When operated in parallel, mismatches in typical characteristics such as threshold voltage and on-resistance, coupled

with an asymmetric structure, lead to significant current imbalances, presenting a critical issue [15–17].

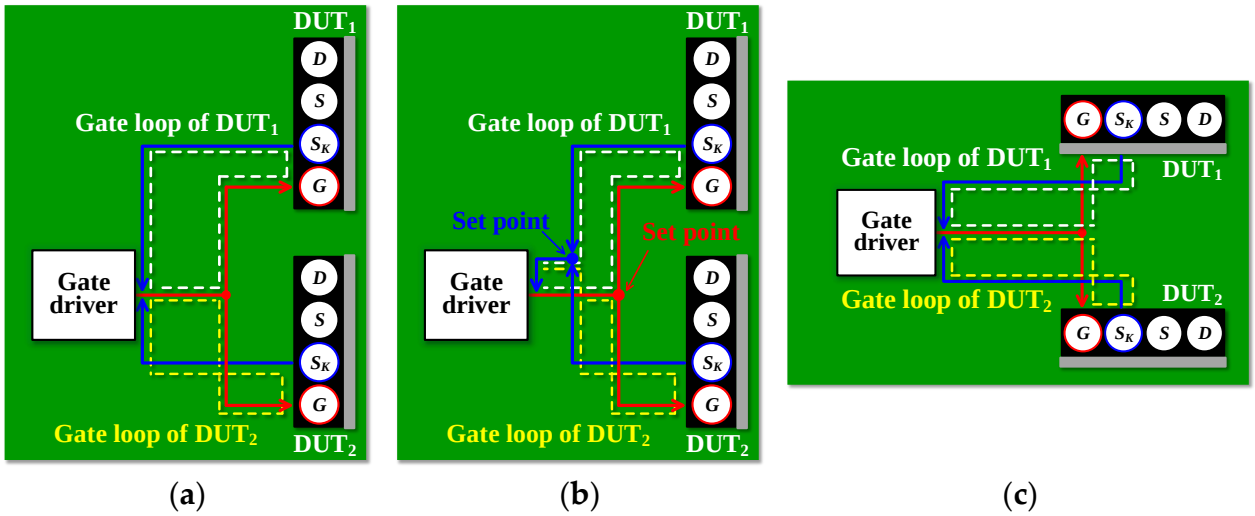
In particular, SiC power semiconductors exhibit a heightened vulnerability to current imbalances when connected in parallel. The switching characteristics of SiC power semiconductors, characterized by their small input and output capacitances, are substantially influenced by the parasitic inductance present in the circuit. The existence of a discrepancy in the magnitude of parasitic inductance, due to an asymmetric structure among parallel-connected SiC devices, results in a pronounced current imbalance between the devices. This phenomenon not only escalates switching losses but also diminishes the efficiency of the power converter. Consequently, a plethora of studies has been undertaken to minimize the current imbalance between parallel-connected switching devices [18–27].

The severity of these issues underscores the urgent need for research aimed at resolving the problems of current imbalance among parallel-connected switching devices. Efforts to enhance the efficiency and reliability of parallel connection technologies have become an indispensable part of designing high-performance power systems.

Lu [18] improved the current-balancing of parallel-switching devices by connecting a toroidal core to the output of a half-bridge module and adjusting the mutual inductance between the devices. However, this method requires an additional current-balancing circuit, which significantly increases volume. A current-balancing method using a common-mode choke between parallel devices was proposed in [19,20]. However, this method increased the parasitic inductance of the gate loop, which induced oscillations in each device. An active gate driver (AGD) that adjusts the driving voltage to improve the transient characteristics of the switching device was proposed in [21,22]. The AGD minimizes the current imbalance between parallel devices by adjusting the slope of the drain current at the transients. However, AGD sacrifices the switching speed for current-balancing, which diminishes the advantages of SiC power semiconductors. As reported in [18–23], active current-balancing methods that add a magnetic material or adjust the slope of the drain current increase the cost, volume, and complexity.

In contrast, structural current-balancing methods do not have the aforementioned disadvantages because the current imbalance is minimized through a symmetrical arrangement between switching devices connected in parallel [24–27]. Figure 1 shows the gate loop formed by the two devices under test (DUTs) and gate drivers using the previously studied methods; the package-type of the switching device is a TO-247-4 with a Kelvin source. In Figure 1, D, S, S_K, and G represent the drain, power source, Kelvin source, and gate of the device, respectively. In [24,25], the current from the gate driver to the gate of each device was matched by arranging the two devices perpendicular to the gate driver output, as shown in Figure 1a. However, there was a large difference in the length of the gate loop because the return path to the gate driver was asymmetric. Prakash et al. [26] set a point that must be passed through to form a symmetrical gate loop, as shown in Figure 1b. The gate loop lengths of the two devices become symmetrical when the gate loop is formed by passing through the set point. However, this method lengthens the gate loop because it must pass through the set point to satisfy symmetry. Both the symmetry and loop length must be considered because the switching characteristics of SiC power semiconductors are sensitive to parasitic inductance. Zhao et al. [27] achieved a symmetrical gate loop by rotating the devices in Figure 1a by 90° to the right, as shown in Figure 1c. However, it is difficult to attach a heatsink because the lead frames of the two devices vertically face the same direction. Even if the devices are bent toward the printed circuit board (PCB) to facilitate a heatsink attachment, there must be sufficient space between DUT_1 and DUT_2, which can result in a long gate loop.

In previous studies, several methods achieved the symmetry of the gate loop. However, the symmetry of the power loop affects the current imbalance. The symmetry of the power loop inductance should be considered in detail when constructing a half-bridge with parallel-connected devices. However, most published papers reported only achieving gate loop symmetry without considering the power loop.



(**a**) (**b**) (**c**)

Figure 1. Conventional structural current-balancing methods (**a**) in [24], (**b**) in [26], (**c**) in [27].

In this study, a half-bridge switching power module (HBSPM) based on parallel-connected SiC MOSFETs with a symmetric structure and low inductance was proposed. The effect of parasitic inductance and symmetry on parallel-connected SiC MOSFETs is analyzed, and a structure with a gate loop and power loop symmetry with low inductance is presented. The proposed HBSPM improves current imbalance through current loop symmetry and allows for easy attachment of a heatsink for practical applications. A detailed PCB layout design was also provided. The symmetry of the proposed HBSPM was analyzed in detail using ANSYS Q3D. Finally, experimental results are presented to verify the current-balancing performance of the proposed paralleled SiC MOSFETs based HBSPM.

The rest of the article is summarized as follows: Section 2 introduces the proposed structural current-balancing method; in Section 3, a detail design of the HBSPM based on the proposed structural method is presented; the experimental verifications are provided in Section 4; and Section 5 concludes this article.

2. Proposed Half-Bridge Switching Power Module Based on Parallel-Connected SiC MOSFETs

This chapter discusses the design and implementation of a half-bridge switching power module utilizing parallel-connected SiC MOSFETs. The verification process conducted with the LTspice simulation tool is described. Section 2.1 introduces the basic structure and operating principles of the switching power module. Following, Section 2.2 explains the impact of gate loop inductance on switching performance and the proposed parallel connection structure to minimize it. Section 2.3 covers the design method of the proposed half-bridge structure to overcome the effects of power loop inductance. Lastly, Section 2.4 discusses the practical structure including a heatsink for actual applications.

2.1. Switching Power Module

Figure 2 shows the overall structure of the proposed half-bridge switching power module based on parallel-connected SiC MOFSETs. The power stage of the proposed HBSPM includes decoupling capacitors high-side and low-side parallel-connected SiC MOSFETs Q_1–Q_4. To provide a short loop for high-frequency current during switching transients, the decoupling capacitors are placed close to the half-bridge leg. As a result, the proposed HBSPM can achieve a small power loop inductance, regardless of the structure of the main board connected to the module. The output of the HBSPM V_{out} represents the pole voltage of the half-bridge leg. The signal stage comprises an isolated gate driver power supply, Iso. $GDPS_1$, and an isolated gate driver, Iso. GD_1, to drive high-side devices by receiving input from Connecter1, and Iso. $GDPS_2$ and Iso. GD_2 to drive low-side devices. A multiphase leg, such as a full-bridge or three-phase leg, can be easily

implemented through parallel connections because the proposed HBSPM includes a gate driving circuit. In addition, parallel-connected SiC MOSFETs provide high efficiency in low-power applications and high-current performance in high-power applications.

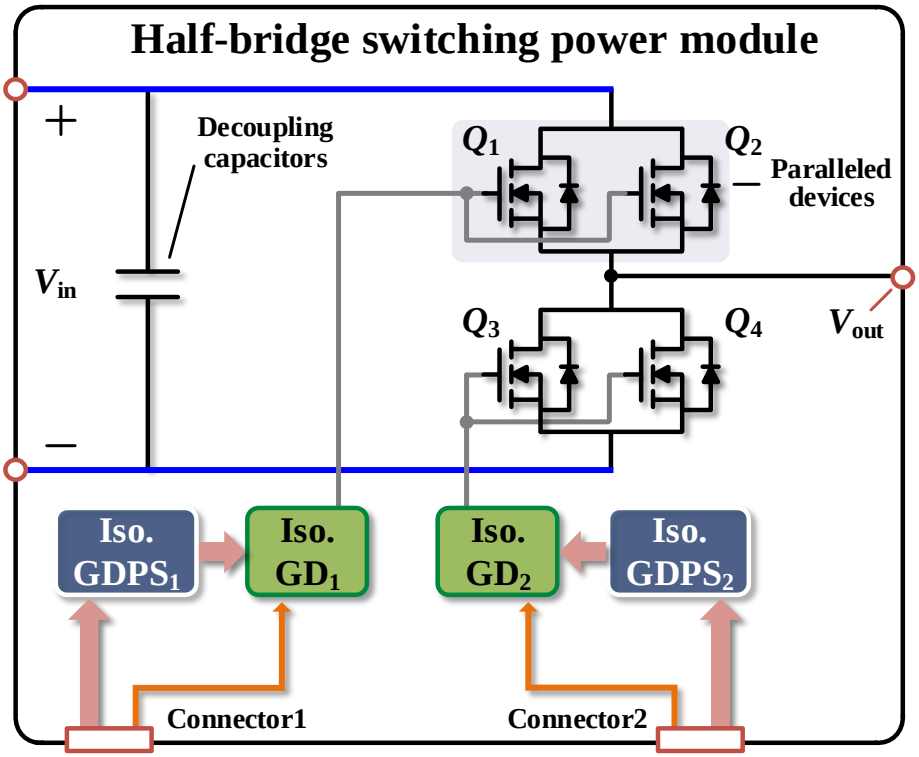


Figure 2. Proposed half-bridge switching power module based on parallel-connected SiC MOSFETs.

2.2. Impact of Gate Loop Inductance and Proposed Parallel Connection Structure

Figure 3a shows the gate loop of a single switching device with the parasitic inductance of the gate loop L_g. In the gate loop, L_g forms an *R-L-C* circuit with the gate resistance R_g and gate-source capacitance C_{gs} of the DUT. As a result, the transfer function of the gate-source voltage V_{gs} to the driving voltage V_g exhibits the characteristics of a second-order system [20]. If L_g increases, the damping ratio of the transfer function decreases, which in turn increases the overshoot of V_{gs}. Additionally, the transfer function has a natural frequency that is determined by L_g and C_{gs}. As L_g increases, the natural frequency decreases, leading to an increase in the fall and rise time of V_{gs} during switching transients [28]. Figure 3b,c show the impact of L_g on the switching characteristics of the DUT in Figure 3a. The selection of L_g values at 10 nH, 20 nH, and 30 nH was aimed at observing the trend within the realistic range of gate loop inductances encountered in typical switching circuits. This approach helps to provide a clear understanding of how different levels of inductance affect the operation of DUT during both turn-on and turn-off transients. Figure 3b shows the V_{gs}, drain-source voltage V_{ds}, and drain current I_d at the turn-off transient when L_g is 10 nH, 20 nH, and 30 nH, respectively. When L_g increases, the damping ratio of the transfer function decreases, causing an increase in the undershoot of V_{gs} and resulting in instability during the turn-off transient. Moreover, due to the increased fall time of V_{gs}, V_{ds} and I_d start changing later. As shown in Figure 3c, an increase in L_g results in an increase in the overshoot and rise time of V_{gs} during the turn-on transient. This implies that the turn-on and off delay increase, and the waveform of V_{gs} becomes unstable when the gate loop inductance increases.

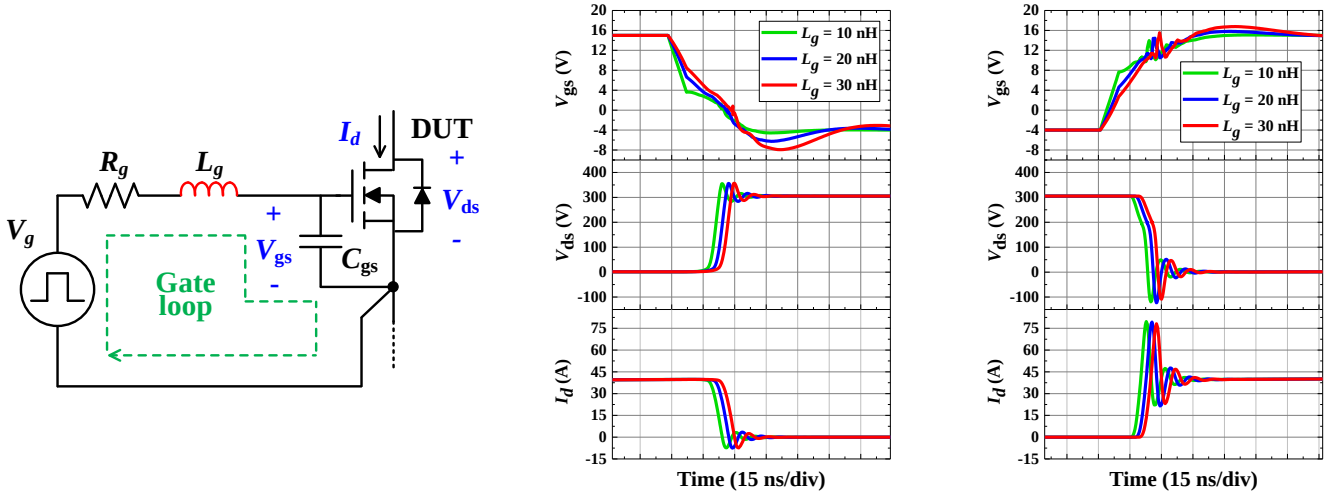


Figure 3. Simulated waveforms of switching transient under different Lg. (**a**) Gate loop of a single switching device. (**b**) Turn-off transient. (**c**) Turn-on transient. (V_g = 15/−4 V, R_g = 10 Ω, DUT = C3M0032120K).

Figure 4a shows the gate loops of parallel-connected devices with gate loop inductance, and Figure 4b,c show the impact of the gate loop inductance imbalance on the parallel-connected devices. The asymmetry of L_g between parallel-connected devices leads to a difference in the fall and rise time, resulting in a current imbalance during switching transients. Figure 4b shows the V_{gs}, V_{ds}, and I_d of each device at the turn-off transient when the gate loop inductance of DUT_1 Lg_1 is 10 nH and the gate loop inductance of DUT_2 L_{g2} is 20 nH. The V_{gs} of DUT_1 decreases faster than that of DUT_2, and the I_d of DUT_1 starts to decrease faster as well because L_{g1} is smaller than L_{g2}. Therefore, the I_d of DUT_2 rises instantaneously. Even in the turn-on transient, DUT_1 begins to conduct first, which results in a large current overshoot at DUT_1, as shown in Figure 4c. Consequently, both the magnitude of the gate loop inductance of each device and the symmetry between the devices must be considered when the devices are driven in parallel.

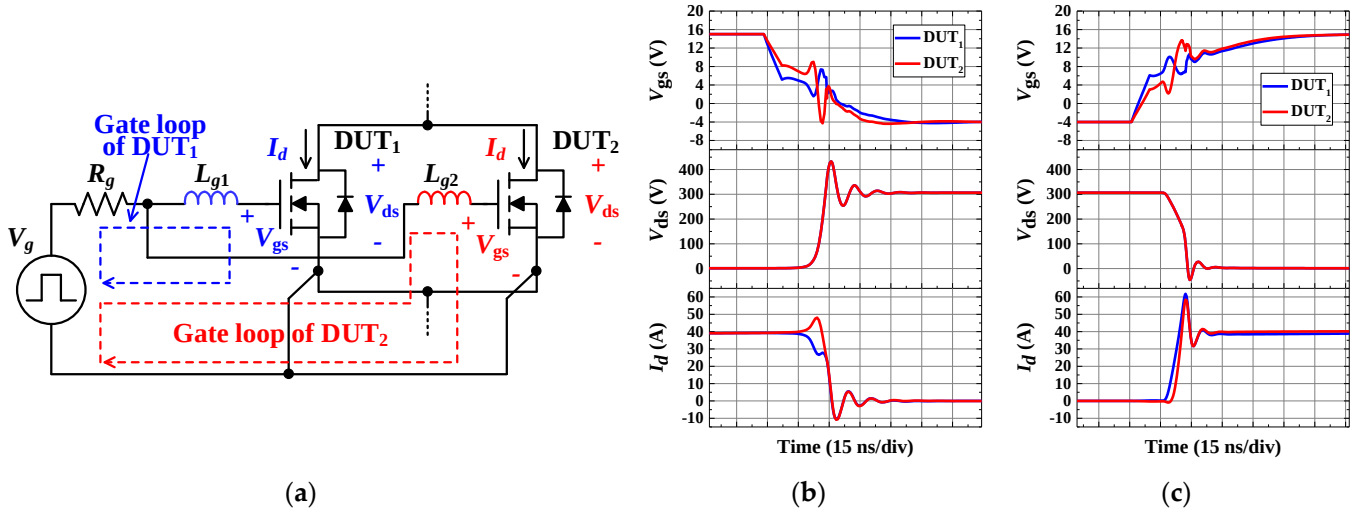


Figure 4. Simulated waveforms of parallel-connected SiC MOSFETs with gate loop inductance imbalance. (**a**) Gate loops of parallel-connected switching devices. (**b**) Turn-off transient. (**c**) Turn-on transient. (L_{g1} = 10 nH, L_{g2} = 20 nH, V_g = 15/−4 V, R_g = 10 Ω, DUT = C3M0032120K).

Figure 5 shows the proposed parallel connection structure and the gate loop of each device. As shown in Figure 1a,b, DUT_1 and DUT_2 are positioned on the vertical line; however, DUT_2 is rotated by 180°. The gate driver is positioned horizontally from the center of the two devices.

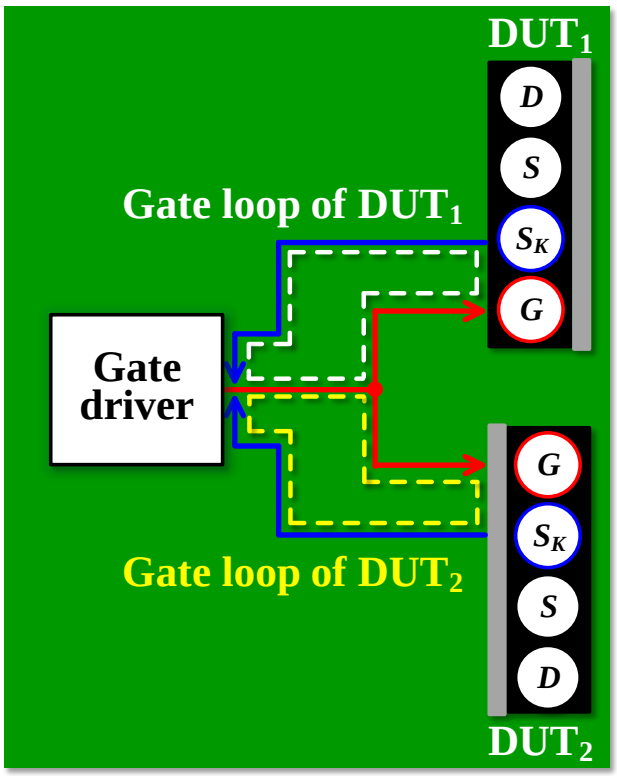
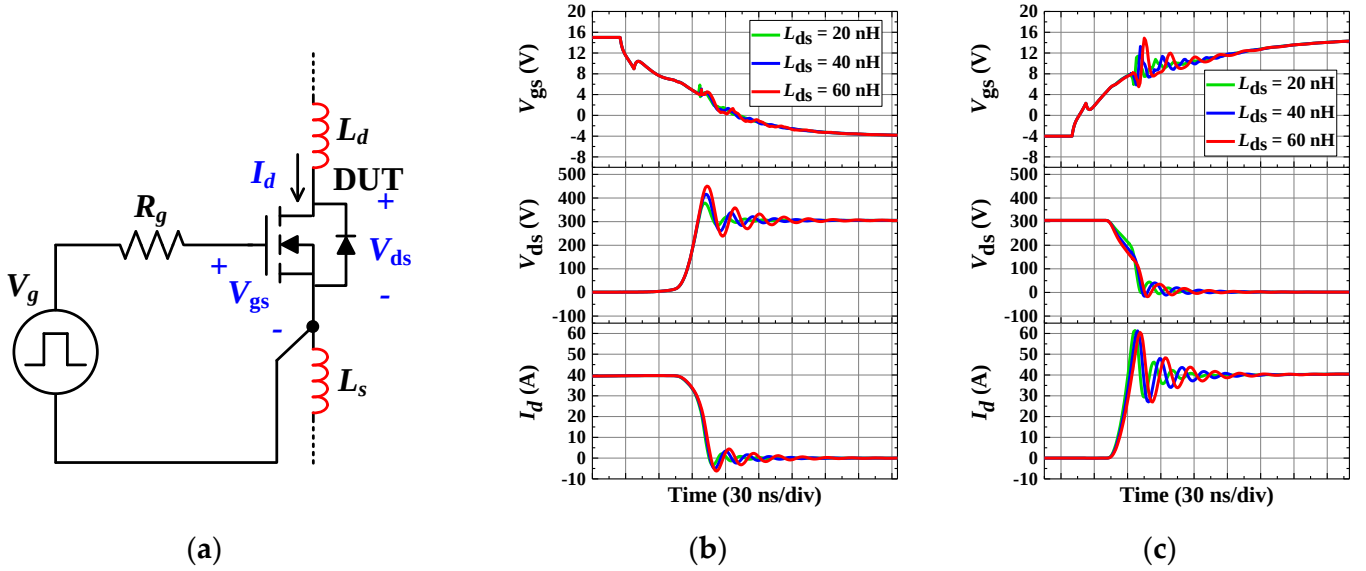


Figure 5. Proposed parallel connection structure.

In the proposed structure, the gate and Kelvin sources of the two devices are located at the same distance from the gate driver, and a symmetrical gate loop can be formed. In addition, when attaching the heatsink, DUT_1 is bent to the left and DUT_2 to the right so that there is no restriction on the distance between the two devices, unlike in Figure 1c. Therefore, the proposed structure can achieve both symmetry and a short gate loop length while facilitating a heat dissipation design.

2.3. Effect of Power Loop Inductance and Proposed Half-Bridge Structure Based on Parallel-Connected SiC MOSFETs

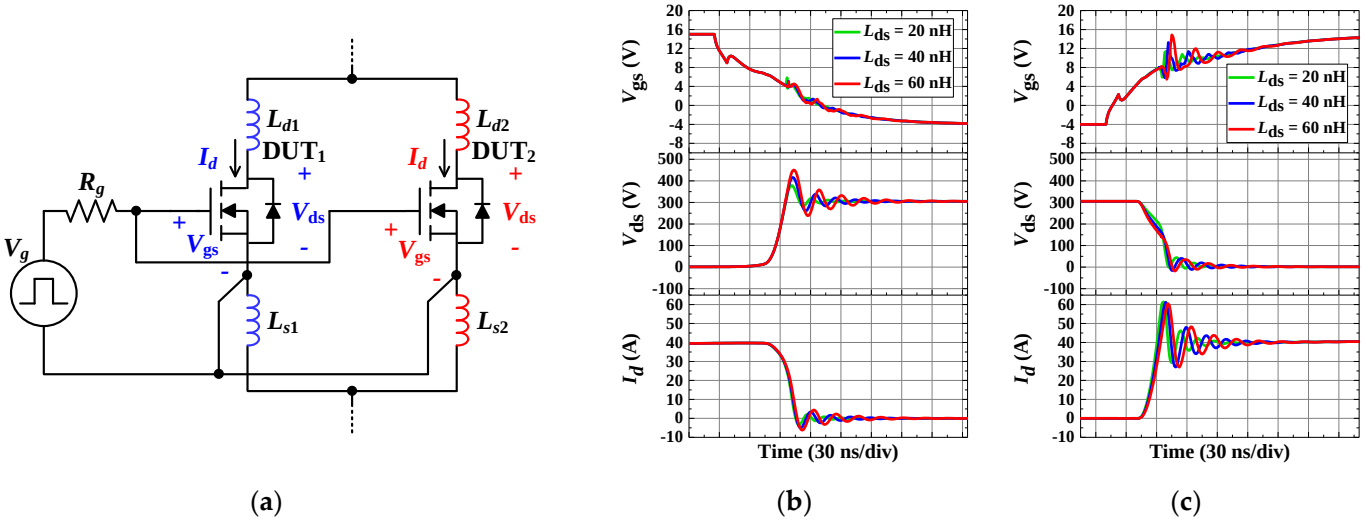
Figure 6a shows the parasitic inductance of the power loop, comprising the drain inductance L_d and source inductance L_s of a single switching device. During switching transients, the induced voltage by di/dt across the power loop inductance increases the overshoot and ringing of V_{ds}. Additionally, when the power loop inductance increases, the slope of I_d decreases, which slows down the switching speed. Figure 6b,c show the effect of the drain-source inductance L_{ds}, which is the sum of L_d and L_s, on the switching characteristics of the DUT in Figure 6a. As shown in Figure 6b, the oscillations of V_{ds} and I_d increase as L_{ds} increases at the turn-off transient. Figure 6c shows the waveforms during the turn-on transient. The oscillations of the voltage and current increase with an increase in L_{ds}, which is similar to the turn-off transient. Moreover, an increase in L_{ds} leads to a decrease in the slope of I_d. If the power loop inductance of the parallel-connected devices is asymmetrical, it not only causes an increase in oscillation but also results in a current imbalance due to the difference in the slope of I_d.



(**a**) (**b**) (**c**)

Figure 6. Simulated waveforms of switching transient under different Lds. (**a**) Drain and source inductances of a single switching device. (**b**) Turn-off transient. (**c**) Turn-on transient. (V_g = 15/−4 V, R_g = 10 Ω, DUT = C3M0032120K).

Figure 7a shows the drain–source inductance of each device connected in parallel, while Figure 7b,c show the impact of the drain–source inductance imbalance on the parallel-connected devices. The drain inductance L_{d1} and source inductance L_{s1} of DUT_1 are 10 nH and the inductances of DUT_2 (L_{d2} and L_{s2}) are 20 nH. As shown in Figure 7b,c, the gate-source and drain-source voltages of the two devices are almost the same; however, an imbalance in the drain current occurs because the *di/dt* of DUT_1 with smaller L_{ds} is larger than that of DUT_2. More current flows to DUT_1 with a small parasitic inductance, and this increases switching loss.



(**a**) (**b**) (**c**)

Figure 7. Simulated waveforms of parallel-connected SiC MOSFETs with drain-source inductance imbalance. (**a**) Drain and source inductances of parallel-connected switching devices. (**b**) Turn-off transient. (**c**) Turn-on transient. (L_{d1} = 10 nH, L_{s1} = 10 nH, L_{d2} = 20 nH, L_{s2} = 20 nH, V_g = 15/−4 V, R_g = 10 Ω, DUT = C3M0032120K).

The power loop inductance must be considered in more detail if a half-bridge leg is constructed using parallel-connected devices. Figure 8 shows the parasitic inductance of a half-bridge leg based on parallel-connected devices.

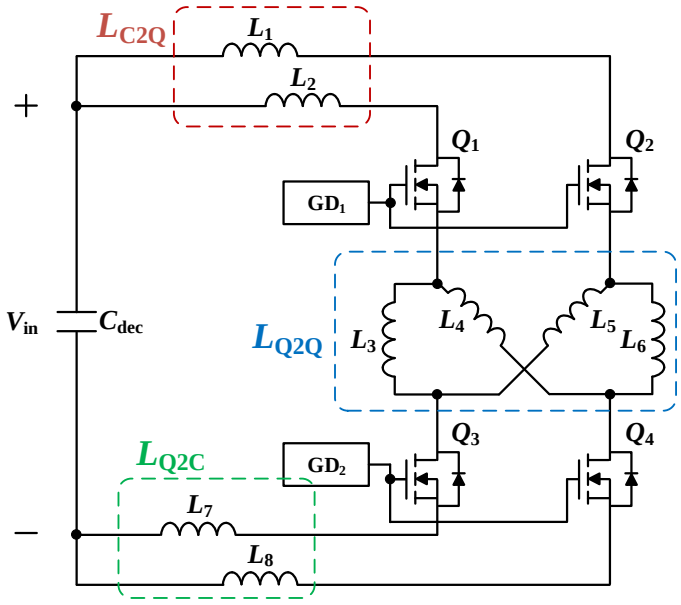
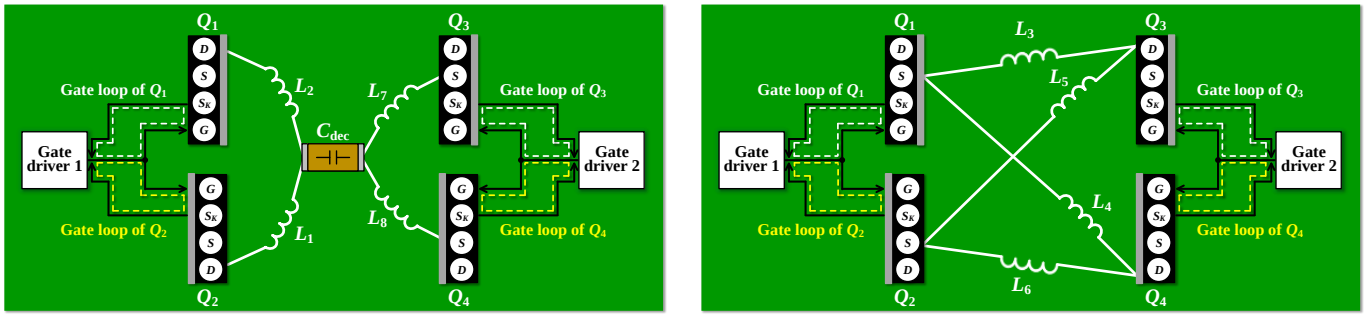


Figure 8. Power loop inductance of parallel-connected SiC MOSFETs half-bridge leg.

The parasitic inductance of a half-bridge leg can be classified into three parts: the inductance L_{C2Q} from the decoupling capacitor C_{dec} to the high-side devices (Q_1 and Q_2), inductance L_{Q2Q} from the source of the high-side devices to drain of the low-side devices (Q_3 and Q_4), and inductance L_{Q2C} from the source of the low-side devices to C_{dec}. For the symmetry of the power loop, the path related to the inductance of each part (e.g., L_1 and L_2 of L_{C2Q}) must have the same length.

Figure 9 shows the structure of the proposed half-bridge switching power module and its parasitic inductance. In the proposed HBSPM, the high-side and low-side devices are horizontally symmetrical, and C_{dec} is located at the center. As shown in Figure 9a, the distance from the drain of Q_1 to C_{dec} is the same as that from the drain of Q_2 to C_{dec}; thus, L_1 and L_2 are the same. The same principle was applied to L_7 and L_8. Therefore, the inductances in L_{C2Q} and L_{Q2C} are symmetrical in the proposed structure. Figure 9b shows the inductance in L_{Q2Q}. As in the previous case, the inductances (L_3–L_6 and L_4–L_5) are symmetrical because the length of each path from the source of the high-side devices to the drain of the low-side devices is the same. Therefore, the proposed half-bridge switching power module satisfies the symmetry requirements in both the gate and power loops through the parallel connection structure in Figure 5 and the half-bridge arrangement in Figure 9.



(**a**) (**b**)

Figure 9. Proposed parallel-connected SiC MOSFETs half-bridge structure. (**a**) Bottom side. (**b**) Top side.

This structural symmetry has a positive impact on the performance of the switching power module. The symmetrical design minimizes parasitic inductance, reducing switching losses and increasing power transmission efficiency. This is particularly advantageous for high-speed switching applications, contributing to reduced power losses and increased overall system reliability. Therefore, the structure of the HBSPM proposed in this study offers an efficient and reliable solution for high-performance power electronics systems.

2.4. Practical Structure with Heatsink

Figure 10 shows the practical structure of the proposed switching power module. As shown in Figure 10a, two gate drivers and six capacitors (C_1–C_6) are located at the bottom side of the HBSPM. To ensure that C_{dec} can carry the current during switching transients, it must have a sufficient current rating. As a result, six capacitors are used in parallel for C_{dec}. The $+V_{in}$ plane connected to the drain of the high-side devices and the $-V_{in}$ plane connected to the source of the low-side devices exist at the bottom side. As shown in Figure 10b, the switching devices are located on the top side of the HBSPM, and there is a V_{out} plan connecting the source of the high-side devices and the drain of the low-side devices, which is the output of the HBSPM. The devices on the top side were bent towards the PCB for ease of attaching the heatsink; Q_1 and Q_3 were bent to the left, and Q_2 and Q_4 were bent to the right. In this structure, the heatsink can be attached easily because the lead frames of all devices face the opposite direction of the PCB, as shown in Figure 10c. Thus, the proposed HBSPM improves current-balancing through a symmetrical structure and can be designed as a heatsink-integrated module to achieve high efficiency and high-power density.

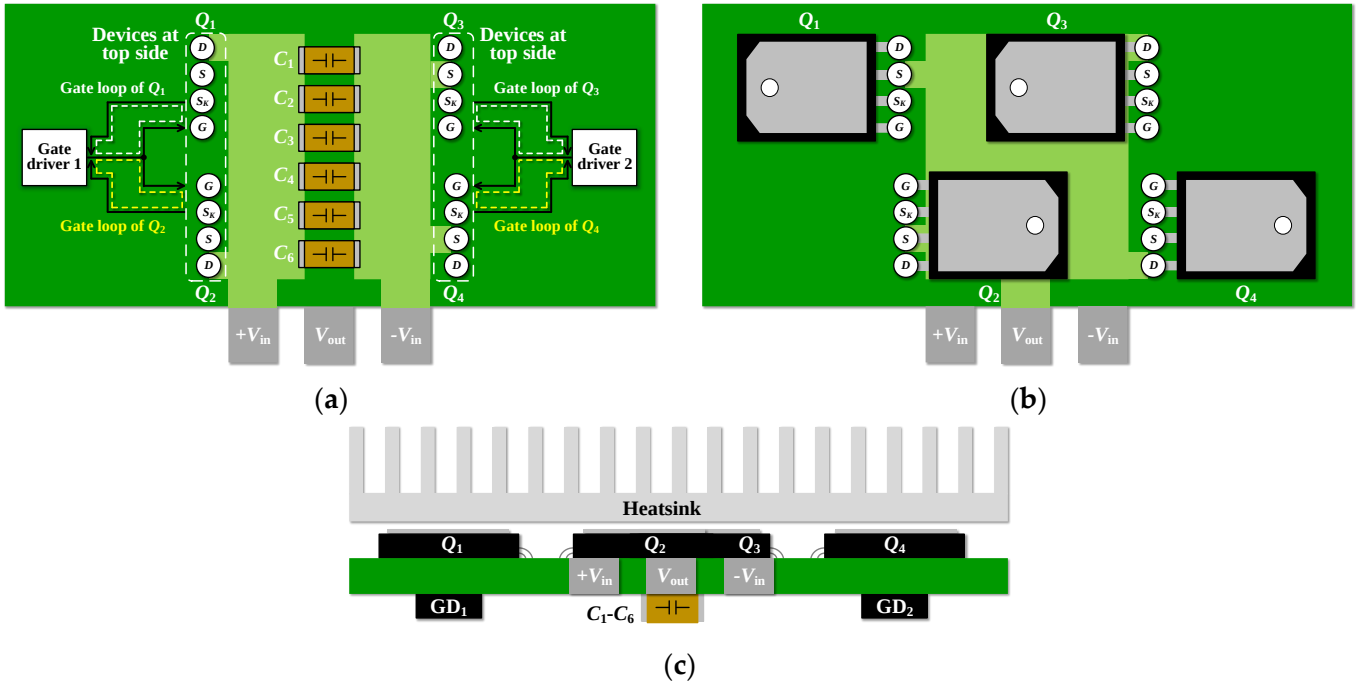


Figure 10. Practical structure of the proposed switching power module (**a**) Bottom side. (**b**) Top side. (**c**) Side view with heatsink.

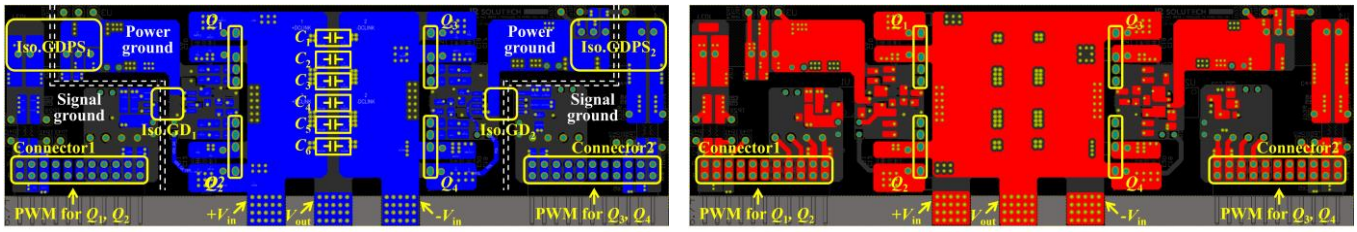
3. Design of the Proposed Half-Bridge Switching Power Module

Section 3 delves into the significance of maintaining symmetry and low values in the inductance of parallel switches, as proposed in Section 2. This study implements such inductance symmetry through PCB layout design, and measures and verifies the parasitic inductance using the ANSYS Q3D simulation tool. The objective is to empirically ascertain the impact of inductance symmetry on the overall performance of the system within a parallel switch configuration. This chapter provides a detailed description of the PCB

layout design techniques and the measurement and verification process using ANSYS Q3D, thereby reiterating the importance of inductance symmetry suggested in Section 2.

3.1. PCB Layout of the Proposed Switching Power Module

Figure 11 shows the PCB layout of the proposed HBSPM based on a 1200 V SiC MOSFET, C3M0032120K. As shown in Figure 11a, the GDPS, the GD for each side device, and the decoupling capacitors are located on the bottom side of the HBSPM, and the signal and power grounds are separated by the insolated ICs. As shown in Figure 11b, on the top side, only the bent devices and other low-profile passive elements are located because the heatsink must be attached. A PWM signal was applied to the device through Connector1 and Connector2.



(**a**) (**b**)

Figure 11. PCB layout of the proposed half-bridge switching power module. (**a**) Bottom side. (**b**) Top side.

3.2. Gate Loop Inductance of Proposed Switching Power Module

Figure 12 shows the gate loops of the low-side parallel-connected devices in PCB layout shown in Figure 11. In the proposed HBSPM, the gate resistance is divided into common gate resistance and individual gate resistance to mitigate the impact of parasitic inductances, including those in the PCB layout. While the proposed structure provides symmetry for the parasitic inductance of the PCB, it can be challenging to account for all parasitic components in practical circuit designs. These components can vary even among the same device model, and manufacturers may not provide detailed information about them. Nonetheless, by separating the common gate resistance and individual gate resistance between devices connected in parallel, it is possible to reduce the effects of reactance in the gate loop and compensate for any imbalances.

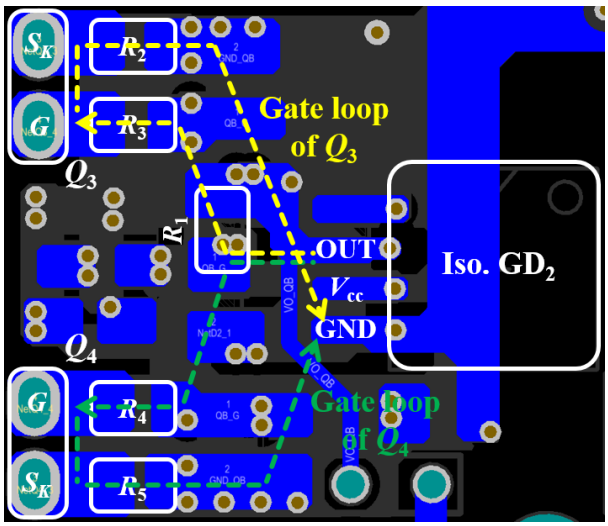


Figure 12. Gate loops of low-side parallel-connected devices.

In the proposed HBSPM, the gate loop of Q_3 is formed through the common gate resistance R_1 at the output of the gate driver, gate resistance R_3, and source resistance R_2 of Q_3. The gate loop of Q_4 is formed through R_1, gate resistance R_4, and source resistance R_5. R_1 adjusts the overall switching speed, and R_2–R_5 are added with a small resistance of 1 Ω to reduce the effect of reactance in the gate loop of parallel-connected devices.

Table 1 summarizes the simulated gate loop inductances of the proposed HBSPM using ANSYS Q3D. As listed in Table 1, the gate loop inductances of Q_3 and Q_4 are 18.35 nH and 15.95 nH, respectively, which is an error of approximately 13%. This error is unavoidable because it is impossible to achieve perfect symmetry because of the position of the output and ground pins of the gate driver. In the proposed HBSPM, the effect of an unavoidable inductance mismatch is minimized by separating the gate resistance from the common gate resistance and the additional resistance such as R_2–R_5.

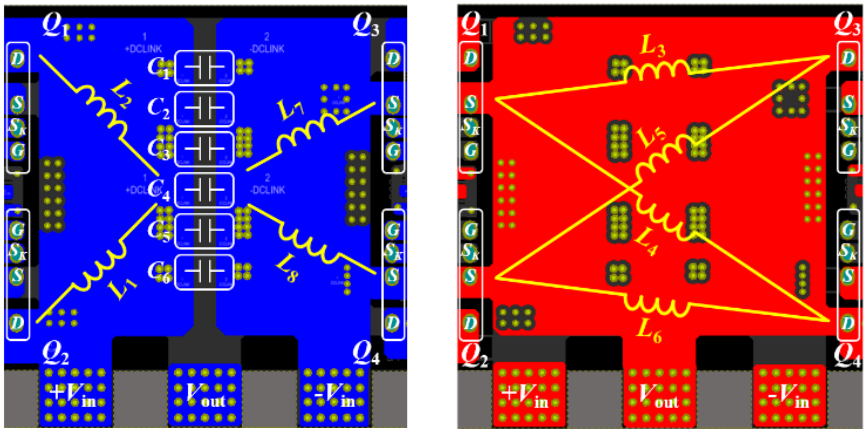
Table 1. Gate loop inductance simulation result.

Parameters	Values
Gate loop inductance of Q_3	18.35 nH
Gate loop inductance of Q_4	15.95 nH

3.3. Power Loop Inductance of Proposed Switching Power Module

Figure 13 shows the power loop inductance of the designed HBSPM. As mentioned in Section 2, the power loop inductance of each part should be symmetrical as

$$\begin{cases} L_1 = L_2 \\ L_3 = L_6 \\ L_4 = L_5 \\ L_7 = L_8 \end{cases} \quad (1)$$



(**a**) (**b**)

Figure 13. Power loop inductance of a designed half-bridge switching power module. (**a**) Bottom side. (**b**) Top side.

Otherwise, because six decoupling capacitors are used in the proposed HBSPM, L_1, L_2, L_7, and L_8 must be specifically expressed as shown in Figure 14. Accordingly, the condition satisfying the symmetry of the power loop inductance can be expressed as

$$\begin{cases} L_{1x} = L_{2x} \\ L_3 = L_6 \\ L_4 = L_5 \\ L_{7x} = L_{8x} \end{cases} \quad (2)$$

where L_{nx} represents the xth inductance of L_n, n = 1, 2, 4, and 8, and x = a, b, c, d, e, and f.

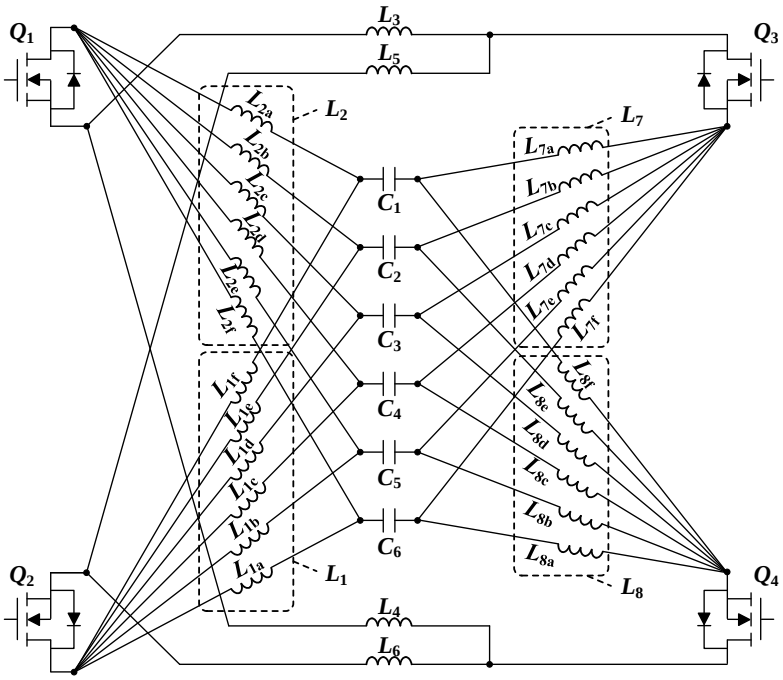


Figure 14. Detailed power loop inductance configuration.

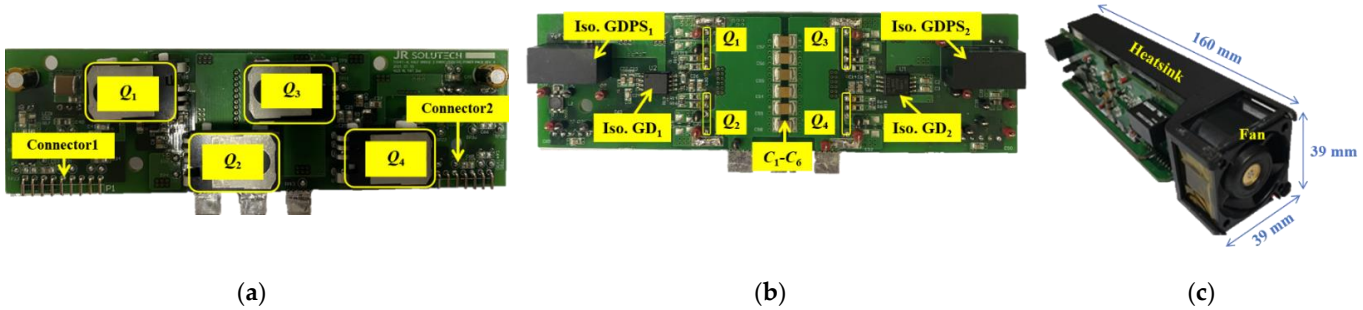
Table 2 lists the simulated power loop inductance of the proposed HBSPM using ANSYS Q3D. As shown in Table 2, the parasitic inductances of each part are almost the same. The inductance simulation results in Tables 1 and 2 show that the designed HBSPM has a symmetrical power loop structure as well as a gate loop.

Table 2. Power loop inductance simulation result.

Parts	Parameters	Values	Parameters	Values
L_{C2Q}	L_{1a}	1.13 nH	L_{2a}	1.22 nH
	L_{1b}	2.57 nH	L_{2b}	2.55 nH
	L_{1c}	4.22 nH	L_{2c}	4.10 nH
	L_{1d}	5.84 nH	L_{2d}	5.74 nH
	L_{1e}	7.80 nH	L_{2e}	7.54 nH
	L_{1f}	9.80 nH	L_{2f}	9.47 nH
L_{Q2Q}	L_3	4.57 nH	L_6	4.83 nH
	L_4	9.03 nH	L_5	9.45 nH
L_{Q2C}	L_{7a}	0.54 nH	L_{8a}	0.88 nH
	L_{7b}	1.12 nH	L_{8b}	0.90 nH
	L_{7c}	1.46 nH	L_{8c}	1.31 nH
	L_{7d}	2.56 nH	L_{8d}	2.09 nH
	L_{7e}	3.06 nH	L_{8e}	3.90 nH
	L_{7f}	4.83 nH	L_{8f}	4.55 nH

3.4. Developed Switching Power Module with Cooling System

Figure 15 shows the developed half-bridge switching power module with a cooling system. Figure 15a,b show the top and bottom sides of the switching power module before the heatsink is attached. Figure 15c depicts the HBSPM with the heatsink and fan. A housing is used for the HBSPM with a heatsink to optimize the flow of the fan, and the total volume is 39 mm × 39 mm × 160 mm.



(**a**) (**b**) (**c**)

Figure 15. Developed half-bridge switching power module based on parallel-connected SiC MOSFETs. (**a**) Top side. (**b**) Bottom side. (**c**) HBSPM with a cooling system.

4. Experimental Result

The performance of the proposed half-bridge switching power module is verified under two experimental conditions. First, a double-pulse test (DPT), wherein the high-side devices were turned off and a double pulse was applied to the low-side devices, was performed to verify the current-balancing of parallel-connected SiC MOSFETs during transient switching. Considering the maximum current of 80 A for the application, the proposed HBSPM performs a double-pulse test (DPT) at 40 A for the parallel-structured low-side device. In the first pulse, the low-side devices are turned on at 0 A and turned off at 40 A. At this juncture, the off-state of the low-side devices at 40 A is analyzed. After the low-side devices stabilize, they are turned on again at 40 A during the second pulse. This procedure allows the energy stored in the load inductor to flow back into the low-side devices, during which the on-state of the low-side devices at 40 A is also analyzed.

Second, a full-bridge LLC resonant converter was designed using the proposed HB-SPM, and the conduction and switching losses of parallel-connected devices were measured and compared.

Figure 16 shows the double-pulse test circuit of the proposed switching power module, and the system parameters are listed in Table 3. Figure 17 shows the transient waveforms of the low-side devices under a gate-source voltage of +15/−5 V, input voltage of 300 V, and a drain current of 40 A. V_{gs} and V_{ds} of Q_3 and Q_4 are measured using a Tektronix TPP0500B passive probe (Beaverton, OR, USA), and I_d is measured using a Rogowski coil SS-284A with a 20 mV/A ratio.

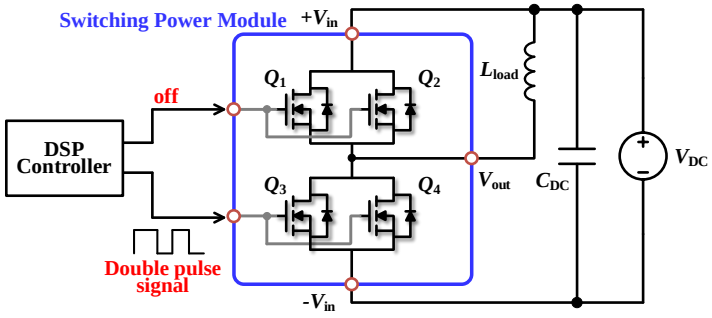


Figure 16. Double-pulse test circuit of the proposed HBSPM.

Table 3. System parameters of the DPT circuit.

Parameters	Values
Gate-source voltage	+15/−5 V
Input voltage	300 V
Load inductance	30 µH
Drain current of each device	40 A

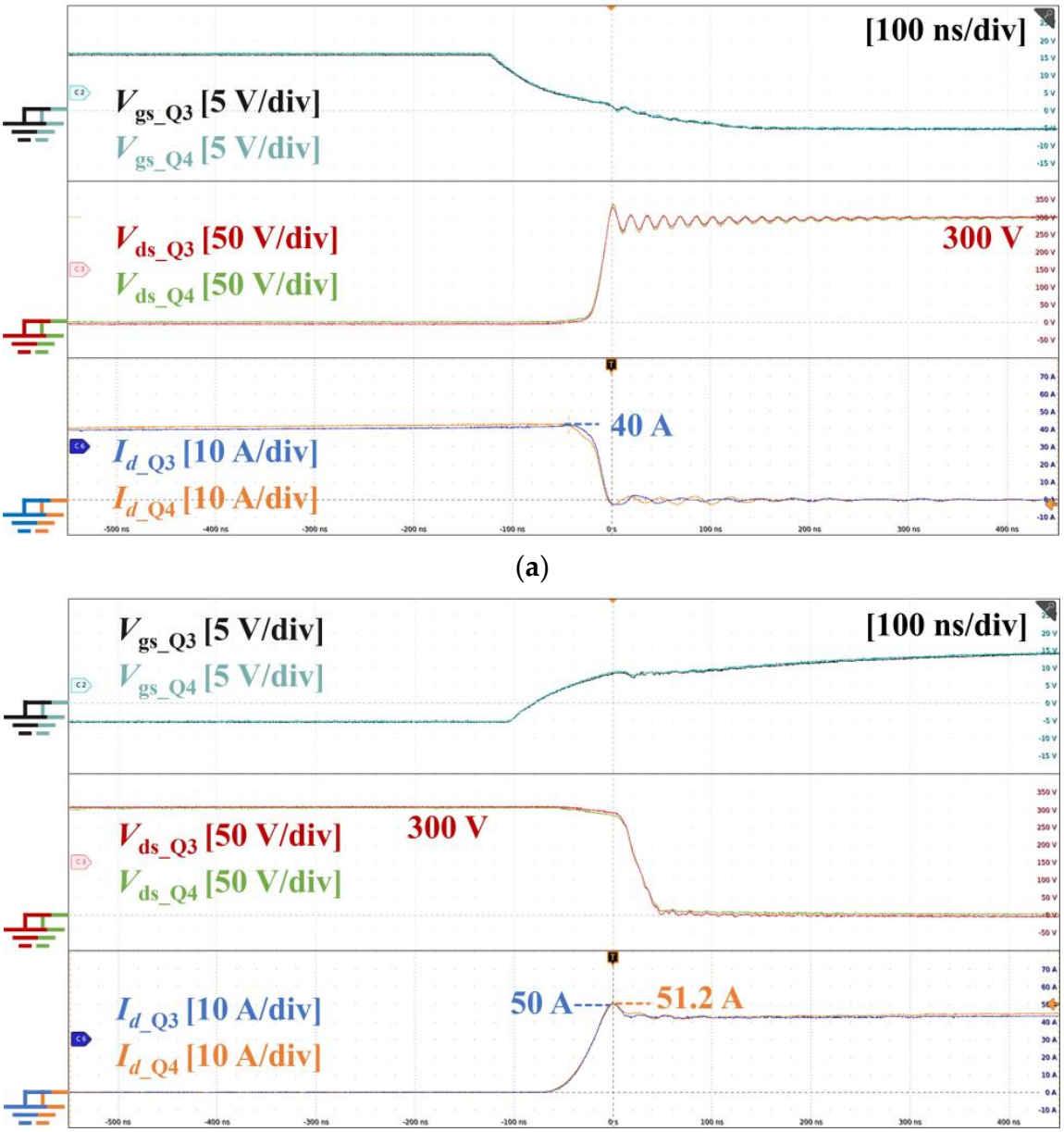


Figure 17. Experimental waveforms of the double-pulse test. (**a**) Turn-off transient. (**b**) Turn-on transient.

As shown in Figure 17a, the V_{gs}, V_{ds}, and I_d of parallel-connected devices are almost the same at turn-off transient. At the turn-on transient in Figure 17b, the V_{gs} and V_{ds} of Q_3 and Q_4 are also almost the same; however, the drain currents are slightly different because the gate loop inductance of Q_3 is slightly larger than that of Q_4. However, the peak currents of Q_3 and Q_4 are 50 A and 51.2 A, respectively; the error is only 2.34%.

Figure 18 shows the calculated switching energies of Q_3 and Q_4 based on the experimental results in Figure 17. The turn-on energy Eon of Q_3 is 718 µJ, and the turn-off energy Eoff of Q_3 is 70.1 µJ; therefore, the total switching energy E_{tot} of Q_3 is 788.1 µJ. By the same principle, the E_{tot} of Q_4 is 786.1 µJ. The total switching energy error between the two devices is only 0.25%, which indicates that the proposed switching power module has excellent current-balancing performance through the symmetry of the gate and power loop inductances without additional components.

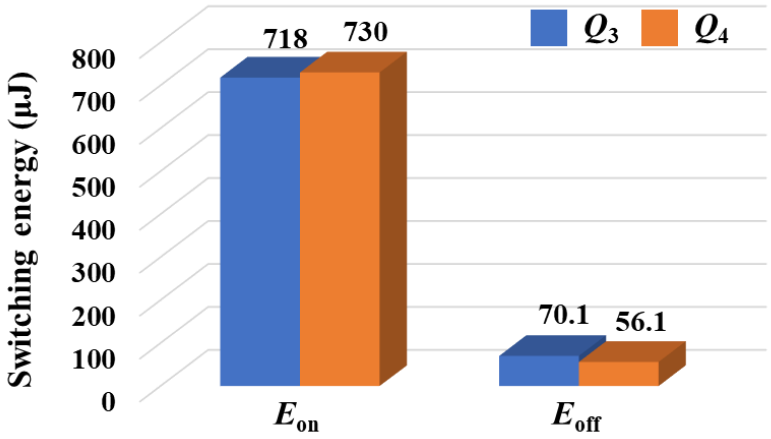


Figure 18. Comparison of switching energy between parallel-connected devices.

Figure 19 shows that a full-bridge LLC resonant converter is designed using the proposed HBSPM to verify current-balancing at the steady state. The full-bridge LLC resonant converter consists of two HBSPMs, a resonant inductor L_r, a resonant capacitor C_r, a transformer TR, and rectifier diodes. The system parameters of the LLC converter are presented in Table 4. Figure 20 shows the V_{gs}, V_{ds}, and I_d of Q_3 and Q_4 in the steady state of the LLC resonant converter. Similar to the results in Figure 17, the V_{gs} and V_{ds} of the two devices are almost the same, and there are slight differences in the drain current of the two devices in the conduction period. However, the magnitude of the RMS current for each device is 20.56 A and 21.04 A, with an error of only 2.28%.

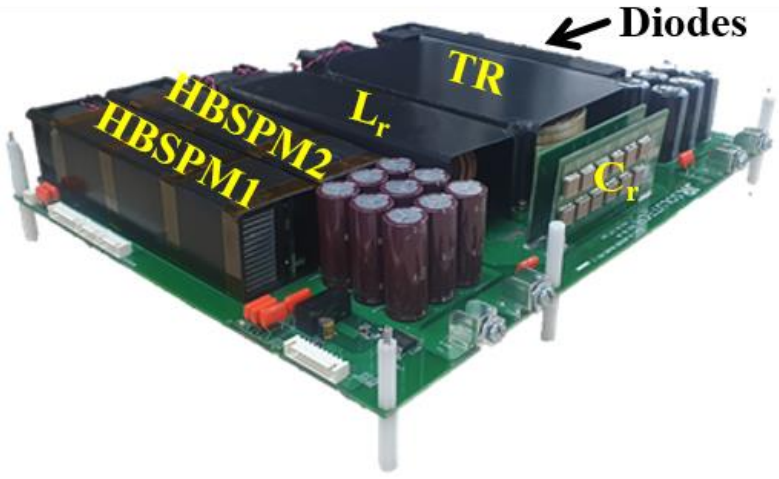


Figure 19. Full-bridge LLC resonant converter based on the proposed HBSPM.

Table 4. System parameters of full-bridge LLC resonant converter.

Parameters	Values
Input voltage	158 V
Input current	45.9 A
Input power	7.25 kW
Resonant inductance	3 μH
Resonant capacitance	825 nF
Magnetizing inductance	10.5 μH
Switching frequency	105 kHz

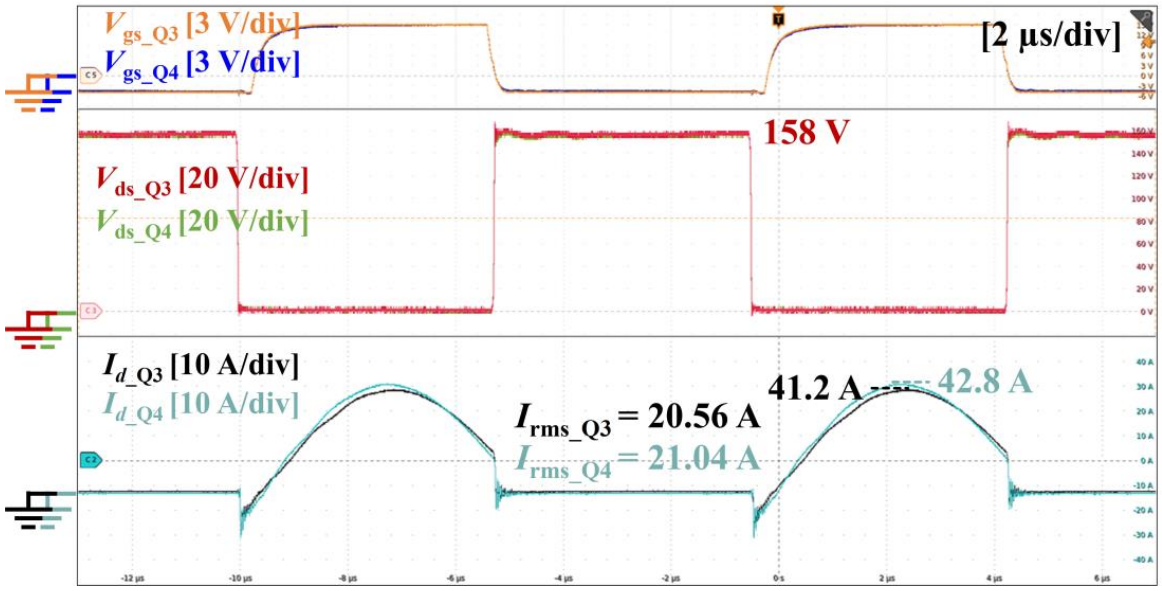


Figure 20. Experimental waveforms of full-bridge LLC resonant converter based on the proposed HBSPM.

Figure 21 shows the calculated conduction loss P_{con} and the turn-off switching loss P_{off} for Q_3 and Q_4 based on the experimental results in Figure 20. The turn-on switching loss is not shown in Figure 21 because the LLC resonant converter performs zero-voltage switching. As shown in Figure 21, the P_{con} of Q_3 is 13.53 W and the P_{off} of Q_3 is 6.65 W; therefore, the total power loss P_{tot} of Q_3 is 20.18 W. The P_{tot} of Q_4 is 20.58 W by the same principle. The total power loss error between the two devices is only 1.94%.

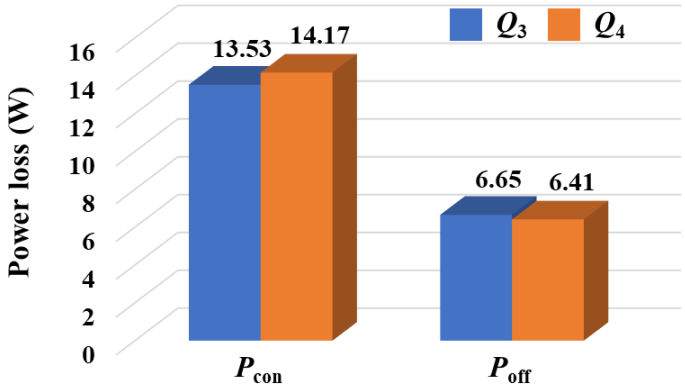


Figure 21. Comparison of power loss between the parallel-connected devices.

These experimental results show that the proposed half-bridge switching power module based on parallel-connected SiC MOSFETs has excellent current-balancing performance and achieves a balance of conduction and switching losses between parallel-connected devices.

5. Conclusions and Discussion

A half-bridge switching power module based on parallel-connected SiC MOSFETs was proposed. The effect of the parasitic inductance of the gate and power loops on the switching characteristics of parallel-connected devices was analyzed. A parallel connection structure that can achieve the symmetry of the gate loop while minimizing the magnitude of inductance was proposed. Based on the proposed parallel connection structure, a half-bridge structure that can achieve the symmetry of the power loop was also proposed. In addition, the proposed switching power module can improve the power density of the

power converter by not only achieving symmetry but also enabling a heatsink-integrated design. The symmetry of the proposed switching power module was verified by measuring the gate and power loop inductances using ANSYS Q3D. The double-pulse test results showed excellent current-balancing of the proposed switching power module. Furthermore, the parallel-connected devices of the proposed switching power module exhibited only a 1.94% power loss error in the resonant converter experiment.

The proposed HBSPM effectively suppresses current imbalance by balancing the parasitic inductance of the PCB through a symmetrical structure. However, the impact of parasitic inductance from passive and active devices other than the PCB remains a challenge to be resolved. In this study, the gate loop inductance imbalance was mitigated by using individual gate resistance, but applying the same method to the power loop is challenging. While there are existing solutions for current-balancing, many of them face technical limitations, such as a trade-off between current-balancing and switching characteristics. These challenges can make it difficult to achieve optimal performance in high-power applications. Therefore, future research is necessary to address the imbalance caused by the parasitic inductance of packages in power loop.

Furthermore, since the proposed structure is based on the Transistor Outline(TO) package, directly applying it to the Surface Mount Device(SMD) package is difficult. Nonetheless, the methodology for balancing the current remains the same. By ensuring the symmetry of the gate loop and considering the power loop symmetry of the half-bridge structure, configuring the PCB layout can achieve good current balance performance.

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