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Highly Robust Atomic Layer Deposition-Indium Gallium Zinc Oxide Thin-Film Transistors with Hybrid Gate Insulator Fabricated via Two-Step Atomic Layer Process for High-Density Integrated All-Oxide Vertical Complementary Metal-Oxide-Semiconductor Applications

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Highly reliable atomic layer deposition (ALD)-derived In-Ga-Zn-O thin-film transistors with high field-effect mobility (μ_{FE}) and hydrogen (H) resistivity are crucial for the semiconductor industry. Herein, a hybrid Al_2O_3 gate insulator (GI) is proposed that is designed by controlling the plasma-enhanced ALD and thermal ALD processes in situ to demonstrate robust characteristics. A hybrid GI is applied to the top-gate geometry of an $In_{0.71}Ga_{0.08}Zn_{0.21}O$ active layer. The optimal device exhibits exceptional electrical characteristics, including a threshold voltage of 0.37 V, μ_{FE} of 150.7 $cm^2 V s^{-1}$, subthreshold swing of 64.0 mV $decade^{-1}$, and hysteresis of 0.02 V. It demonstrates high resistance to H annealing and reliable positive bias temperature stress, as well as changes in V_{TH} shifts of −0.43 and 0.00 V, respectively. The excellent electrical characteristics and high robustness of the device can be attributed to the precise control of H, oxygen, and carbon species within the upper region of the hybrid GI. The achievement of robust device characteristics enables the design of a novel vertical complementary metal-oxide-semiconductor inverter that exhibits a voltage gain of 44.7 V V^{-1} and a noise margin of 87.5% at a 10 V supply voltage.

1. Introduction

In recent years, amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs) have garnered significant attention owing to their high field-effect mobility (μ_{FE}), steep subthreshold swing (SS), and exceptionally low leakage current.[1–3] In addition, the advantages of a-IGZO TFTs such as low fabrication cost, large area uniformity, and relatively low-temperature fabrication (≤400 °C) have resulted in the commercialization of various display products.[4–6] Recently, a-IGZO TFTs have received attention in the semiconductor industry because of their high compatibility with vertical structures for achieving high-density integration and processes in memory, which is known as the post-Von Neumann architecture. However, the main challenge in this field is to achieve excellent step coverage and thickness precision of thin films within complex three-dimensional (3D) structures for high-density integration. Therefore, novel atomic layer deposition (ALD) techniques are indispensable in the semiconductor industry.[7–9] Researchers are actively investigating the potential application of ALD-derived vertical TFT stacking technology for high-density monolithic devices such as 3D complementary metal-oxide-semiconductor (CMOS), dynamic random-access memory, and NAND flash memory.[10–13]

In general, semiconductor memory devices operate based on current derived from the gate voltage. Therefore, channels with high mobility (on-current) and reliable bias stability are necessary to guarantee low-voltage operation and long-term use. Several groups have extensively investigated the relationship between

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the mobility and reliability of a-IGZO TFTs and agreed that oxygen (O) species such as O-vacancy (V_O), O interstitials (O_i), and peroxide (O_2^{2-}) govern the abovementioned properties.[14–19] In addition, several researchers have reported that hydrogen (H) determines the mobility and stability of a-IGZO TFTs because they behave not only as donor-like states (H_i^+, H_O^+, and V_OH), but also as bistable centers (H_i^-, H_O^-, and M–H).[20–23] These O and H species can be incorporated adjacent to the a-IGZO layer during the fabrication process of a-IGZO TFTs because significant amounts of H and O are resolved in the buffer layer, gate insulator (GI), and passivation layers.[24,25]

Another crucial requirement for channels in semiconductor devices is the ability to tolerate H incorporation. H treatment was employed to enhance the dry etching capabilities and regulate the defects of the insulation material during the fabrication process.[26,27] Consequently, the underlying a-IGZO TFTs were inevitably subjected to H incorporation, which eventually resulted in a negative threshold voltage (V_{TH}) shift. To enhance resistance to H diffusion, researchers have attempted to utilize Al_2O_3 materials with inherent H diffusion barrier properties.[28] Furthermore, C and O species present in Al_2O_3 have been reported to bond chemically with H, thereby enhancing its H diffusion barrier properties.[29] Hence, an Al_2O_3 material with precisely controlled amounts of C and O species that serve as an effective H-diffusion barrier adjacent to the a-IGZO layer must be employed.

In this study, we propose an approach for obtaining ALD-derived a-IGZO TFTs that demonstrate both bias stability and H incorporation, in addition to high mobility. An ALD-Al_2O_3 GI is implemented in a top gate-bottom contact (TG-BC) structure to obtain self-passivation properties for the a-IGZO layer. Here, the ALD-Al_2O_3 GI is deposited via plasma-enhanced ALD (PE-ALD, O_2 plasma) and thermal ALD (T-ALD, O_3) with distinct reactivity differences to precisely modulate the O, H, and C species within the Al_2O_3 layer. By considering the effect of reactants for ALD-Al_2O_3 on device characteristics, we design a hybrid Al_2O_3 structure by controlling the reactants in situ. The achievement of robust device characteristics using T-ALD Al_2O_3 with optimal thickness enables the development of a novel vertically stacked CMOS inverter designed for high-density devices.

2. Results and Discussion

2.1. Comparison of ALD-Al_2O_3 Film Properties Prepared by O_2 Plasma and O_3 Reactants

In ALD, many reactants are used to obtain Al_2O_3, including O_2 plasma, H_2O, H_2O_2, and O_3. In this study, we focused on the relatively stable O_2 plasma and O_3 reactants for semiconductor applications. **Figure 1**a shows a schematic illustration of the ALD-Al_2O_3 process using O_2 plasma (PE-ALD) and O_3 (T-ALD) reactants. To facilitate the oxidation of trimethylaluminum (TMA) ligands, the O_2 plasma ignition and O_3 dose time were set as 1 and 5 s, respectively, at a temperature of 200 °C. Figure 1b illustrates the electrical characteristics of 15-nm-thick Al_2O_3 deposited via PE-ALD and T-ALD on metal–insulator–metal (MIM)

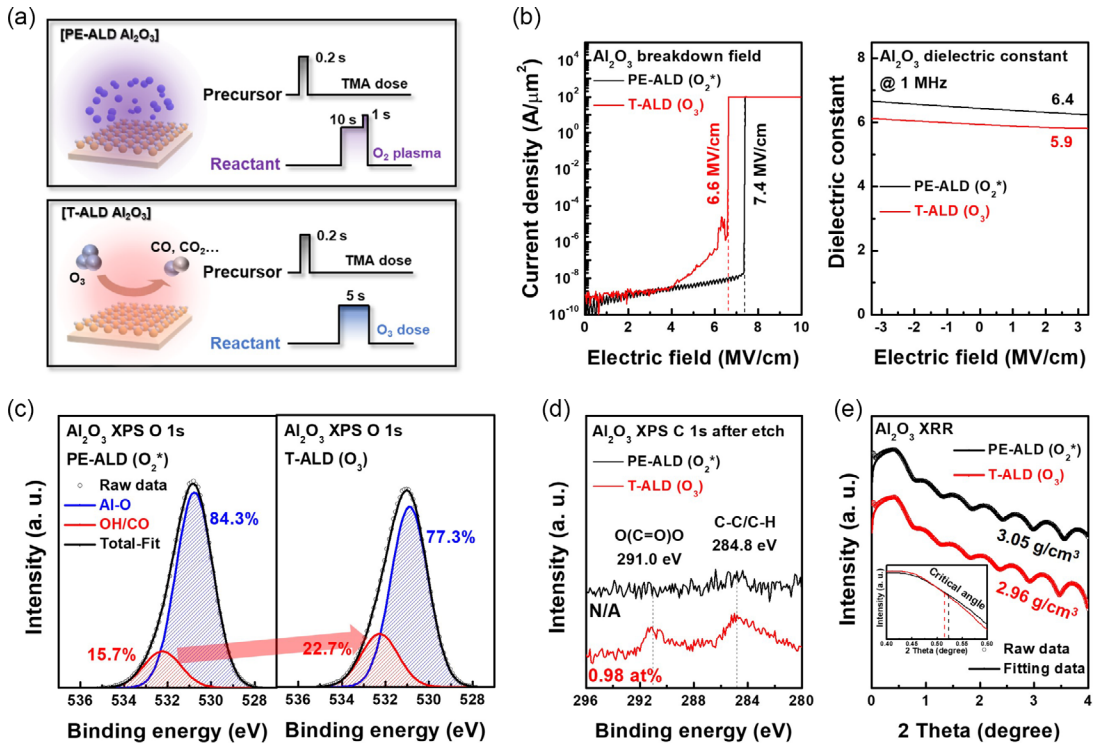

Figure 1. a) Schematic illustration of PE-ALD and T-ALD processes to achieve Al_2O_3 films. b) Breakdown field and dielectric constant of the Al_2O_3 films extracted from MIM structure. XPS c) O 1s and d) C 1s spectra of the Al_2O_3 films. e) X-Ray reflectometry (XRR) spectra of the Al_2O_3 films and comparison of the critical angle (inset).

structures. The PE-ALD Al_2O_3 demonstrated a slightly higher hard breakdown electrical field compared with the T-ALD Al_2O_3 (PE-ALD:7.4 MV cm^{-1}, T-ALD:6.6 MV cm^{-1}). Furthermore, the dielectric constants of the PE-ALD Al_2O_3 were higher than those of the T-ALD Al_2O_3 (PE-ALD:6.4, T-ALD:5.9). Variations in the electrical characteristics of Al_2O_3 have been reported to be strongly associated with the chemical bonding states and presence of C impurities.[30,31] To gain insight into the changes in the electrical characteristics based on the reactants, we conducted an X-Ray photoelectron spectroscopy (XPS) analysis. As shown in Figure 1c, the XPS O 1s peaks were deconvoluted using two Gaussian fits, with binding energy-entered peaks at 530.84 ± 0.07 eV (Al–O) and 532.26 ± 0.02 eV (OH/CO).[32,33] Compared with the results of the PE-ALD Al_2O_3, the Al–O peak decreased from 84.3% to 77.3%, whereas the OH/CO peak increased from 15.7% to 22.7% in the T-ALD Al_2O_3. These results are supported by the XPS C 1s spectra of the Al_2O_3 bulk region obtained via Ar^+ etching, as shown in Figure 1d. The C content was not analyzed in the PE-ALD Al_2O_3 samples; meanwhile, the T-ALD Al_2O_3 samples clearly contained approximately 1 at% C with C–O, C–C, and C–H bonding states.[34,35] This resulted in a decrease in film density in the T-ALD Al_2O_3 (2.96 g cm^{-3}) compared with the case in the PE-ALD Al_2O_3 (3.05 g cm^{-3}), as illustrated in Figure 1e. Because the reactivity of O_3 is lower than that of O_2 plasma, the observed C impurity in the T-ALD Al_2O_3 was presumed to have originated from the residual methyl (CH_3) ligand of the TMA precursor.[36,37] Therefore, the variation in the electrical characteristics of Al_2O_3, depending on the reactants used, might have been caused by residual C impurities within the grown film.

2.2. Electrical Properties of ALD-IGZO TFTs Depending on Reactants Used for Al_2O_3 GI Deposition

To identify the effects of the reactants for ALD-Al_2O_3 on the device characteristics, TG-BC a-IGZO TFTs were fabricated, as shown in **Figure 2**a. The a-IGZO active layer was identically deposited with a thickness of 10 nm via PE-ALD; the sole discrepancy between the two devices was the utilization of O_2 plasma and O_3 reactants for the deposition of the Al_2O_3 GI. Figure 2b shows the transfer characteristics of the devices with an Al_2O_3 GI grown via PE-ALD and T-ALD (hereinafter denoted as PE-ALD and T-ALD devices, respectively). The PE-ALD and T-ALD devices demonstrated V_{TH} of 0.49 and −3.81 V, μ_{FE} of 111.2 and 56.9 cm^2 Vs^{-1}, SS of 65.1 and 74.9 mV decade^{-1}, and hysteresis of 0.02 and 0.02 V, respectively. These results indicate that the PE-ALD device performed better than the T-ALD device. In previous research, a well-designed a-IGZO active layer

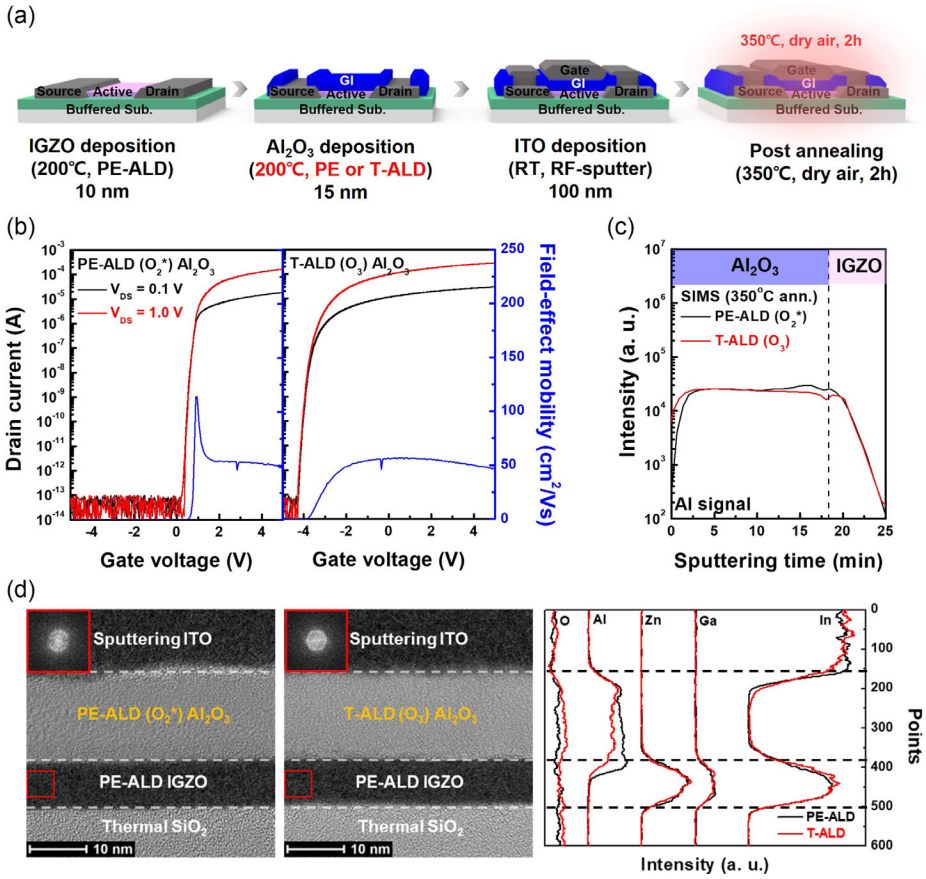

Figure 2. a) Schematic illustration of TG-BC ALD-IGZO fabrication process. b) Transfer characteristics and μ_{FE} of the devices with Al_2O_3 deposited via PE-ALD and T-ALD. The average value of electrical properties was obtained by measuring 10 devices with a size of 1×1 inch. c) SIMS depth profile analysis of Al in Al_2O_3/IGZO stacked films. d) Cross-sectional TEM images and EDS line scans of Al_2O_3/IGZO stacked films.

has been identified as a crucial factor in achieving excellent electrical characteristics.[38,39] Nevertheless, since the only difference among these devices is the Al_2O_3 GI deposition method, it is necessary to understand how the GI deposition method influences electrical characteristics. Many researchers have reported significant effects on the characteristics of devices subjected to periodic application of O_2 plasma treatment at the active layer during GI deposition via PE-ALD in a top-gate geometry.[40–42] To investigate whether the discrepancy in the electrical characteristics between the PE-ALD and T-ALD devices was associated with the O_2 plasma treatment applied to the a-IGZO layer, we performed O_2 plasma treatment prior to the T-ALD Al_2O_3 GI deposition. Figure S1a, Supporting Information, shows a schematic illustration of the fabrication process of the O_2 plasma-treated T-ALD Al_2O_3 device. Considering the cumulative time of the O_2 plasma used for PE-ALD Al_2O_3 deposition, the a-IGZO was subjected to the same O_2 plasma conditions for 140 s prior to the deposition of T-ALD Al_2O_3. Figure S1b, Supporting Information, shows a comparison of the transfer characteristics with and without O_2 plasma treatment before T-ALD Al_2O_3 deposition. As shown, the O_2 plasma treatment before T-ALD Al_2O_3 deposition resulted in a slight positive shift of 0.38 V in V_{TH}. However, the electrical characteristics of the O_2 plasma-treated device differed significantly from those of the PE-ALD device. This result indicates that whereas O_2 plasma treatment during PE-ALD Al_2O_3 GI deposition can assist in adjusting the V_{TH} value, other factors significantly affect the device performance. Figure 2c shows the secondary ion mass spectrometry (SIMS) depth profiles of Al in the Al_2O_3/IGZO stacked films. Notably, the Al signal at the interface between Al_2O_3 and a-IGZO in the stacked film with PE-ALD Al_2O_3 was higher than that of the T-ALD Al_2O_3. To observe this more clearly, we performed a transmission electron microscopy (TEM)-energy dispersive spectroscopy (EDS) analysis of the stacked film. Figure 2d shows the cross-sectional TEM images and EDS line scans of the PE-ALD and T-ALD Al_2O_3 stacked films. Both the TEM images and fast Fourier transform patterns of the a-IGZO (inset) revealed similar results for the stacked films, where a smooth interface was indicated between Al_2O_3 and a-IGZO, as well as a diffuse ring. However, in the case of the stacked film with PE-ALD Al_2O_3, the Al element was presumed to have resolved at the a-IGZO surface area as well as appeared predominantly at the interface between Al_2O_3 and a-IGZO, as compared with the case involving the T-ALD Al_2O_3. In our experiment, because the deposition temperatures of both PE-ALD and T-ALD Al_2O_3 were the same, the result above cannot be explained by the difference in the adsorbed TMA precursors. Several researchers have reported that the TMA precursor exhibits high reactivity in ligand exchange reactions, which can result in a partially etched underlying IGZO layer during chemical reactions.[43,44] Therefore, the difference in the Al signal between the stacked films with PE-ALD and T-ALD Al_2O_3 likely originates from the additional energy provided by the O_2 plasma reactant, not the O_3 reactant, which facilitates enhanced chemical reactions. Al has a higher affinity for oxygen compared with In, Ga, and Zn. Consequently, doping IGZO with Al can potentially reduce the V_O concentration, thus resulting in suppressed carriers and defects.[45,46] Additionally, the Al_2O_3/IGZO stacked films were subjected to SIMS analysis to investigate the variations in O and H in the IGZO active layer, as shown in Figure S2a, b, Supporting Information, respectively. The O signal in the a-IGZO layer exhibited negligible changes, whereas the intensity of H at the interface between Al_2O_3 and a-IGZO for the PE-ALD Al_2O_3 was lower than that for the T-ALD Al_2O_3. Generally, H species in IGZO serve as carriers because they appear in the forms of H_i^+ and H_O^+. However, an excessive H concentration in oxide semiconductors can result in the formation of deep acceptor-like bistable centers (H_i^-, H_O^-, and M–H), leading to the degradation of device characteristics.[20,21] Therefore, the combination of resolved Al and accumulated H at the interface between Al_2O_3 and a-IGZO might determine the discrepancy in electrical characteristics between the PE-ALD and T-ALD devices.

2.3. Hybrid Al_2O_3 GI Design Using a Two-Step in Situ ALD Process

Based on the electrical characteristics of the PE-ALD device, we designed hybrid Al_2O_3 GI structures through the in situ control of O_2 plasma and O_3 reactants. This approach was employed to obtain insights into the effects of alterations in the bulk GI on the device characteristics. **Figure 3**a shows a schematic illustration of the hybrid Al_2O_3 GI structure deposited on the a-IGZO layer. The overall thickness of the Al_2O_3 GI remained at 15 nm. In this case, as the bottom thickness of the PE-ALD Al_2O_3 film decreased, the top thickness of the T-ALD Al_2O_3 film increased. Devices A, B, C, and D denote devices with T-ALD/PE-ALD Al_2O_3 thicknesses of 0/15, 6/9, 12/3, and 15/0 nm, respectively. Figure S3a,b, Supporting Information. shows the transfer and output characteristics of devices with hybrid Al_2O_3 GI structures, respectively. The representative properties of devices B and C are shown in Figure 3b. The key electrical parameters are listed in **Table 1** and their variations are compared in Figure 3c. As shown, the electrical characteristics exhibited significant variations as the top thickness of the T-ALD Al_2O_3 layers increased. Subsequently, the V_{TH} shifted negatively from devices A to D, with device D exhibiting a particularly high degree of V_{TH} shift. Furthermore, device B exhibited a significantly higher increase in μ_{FE} compared with device A, whereas μ_{FE} decreased from devices B to D. Meanwhile, devices C and D, whose mobility reduced significantly, indicated degraded SS. To understand the primary factors affecting the changes in the key electrical parameters, we performed a technology computer-aided design (TCAD) simulation to extract the active-layer density of states (DOS). Figure S4, Supporting Information, presents the TCAD fitting results for the devices with hybrid Al_2O_3 GI structures, and representative results for devices B and C are shown in Figure 3d. The obtained TCAD parameters are listed in Table S1, Supporting Information. Notable changes in the carrier concentration ($n_{carrier}$), acceptor-like tail state (N_{TA}), and Gaussian donor state (N_{GD}) are shown in Figure 3e. The variations in the TCAD parameters revealed a close relationship between the V_{TH}, μ_{FE}, and SS values and $n_{carrier}$, N_{TA}, and N_{GD}, respectively. As shown in Figure 2, the resolved Al element at the interface between Al_2O_3 and a-IGZO is likely to affect the changes in the TCAD parameters between devices A and D. However, we did not consider this to be a significant factor in devices A, B, and C because they

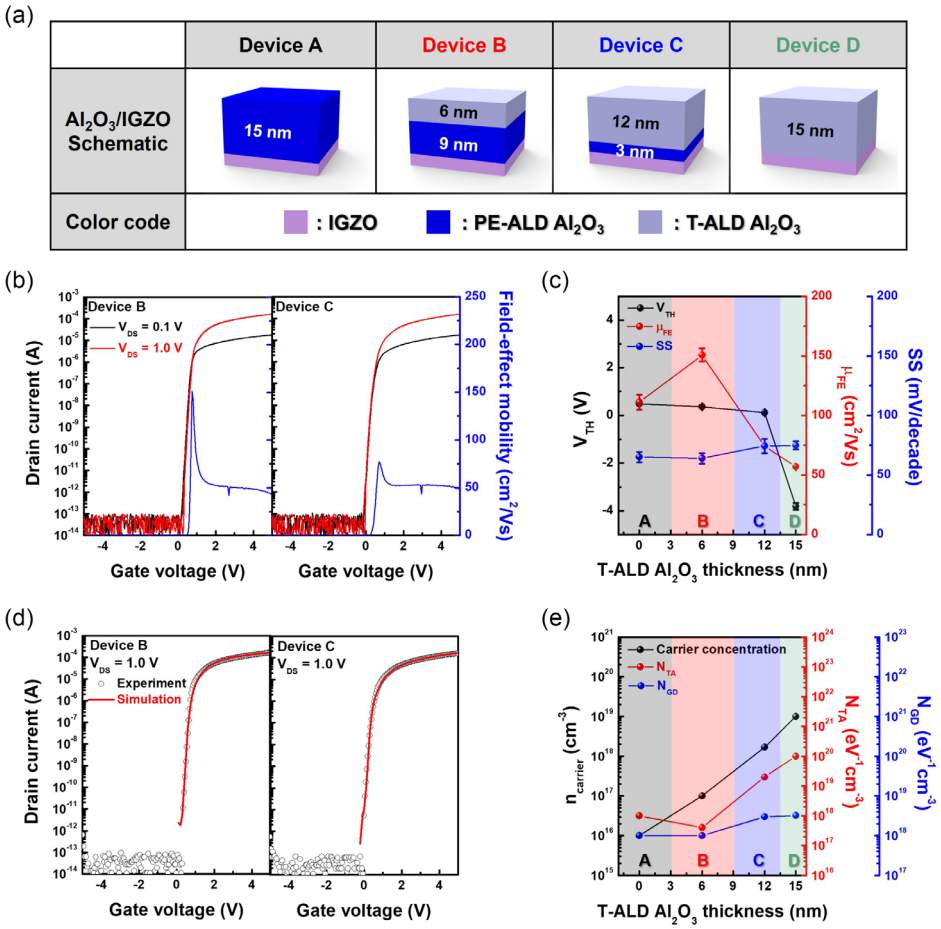

Figure 3. a) Schematic illustration of hybrid Al_2O_3 GI deposited by in situ controlling PE-ALD and T-ALD processes. b) Transfer characteristics and μ_{FE} of the devices with hybrid Al_2O_3 GI and c) variations in key electrical parameters. The average and standard deviation values of electrical properties were extracted by measuring ten devices with a size of 1 ×1 in. d) Simulation results obtained using TCAD for transfer characteristics of devices with hybrid Al_2O_3 GI, and e) representative changes in DOS extracted from TCAD result.

Table 1. Comparison of device key parameters of ALD-IGZO TFTs with hybrid Al_2O_3 GI. The average and standard deviation values of electrical properties were extracted by measuring 10 devices with a size of 1×1 in.

	V_{TH} [V]	μ_{FE} [$cm^2 Vs^{-1}$]	SS [mV $dec.^{-1}$]	Hysteresis [V]
Device A	0.49 ± 0.04	111.2 ± 6.2	65.1 ± 4.4	0.02 ± 0.02
Device B	0.37 ± 0.06	150.7 ± 5.5	64.0 ± 4.4	0.02 ± 0.02
Device C	0.12 ± 0.02	74.3 ± 6.1	72.7 ± 3.9	0.02 ± 0.02
Device D	-3.81 ± 0.14	56.9 ± 3.6	74.9 ± 3.6	0.02 ± 0.01

comprised the same PE-ALD Al_2O_3 component at the bottom of the hybrid Al_2O_3 GI. We observed that the H intensity was different in both Al_2O_3 and a-IGZO, depending on the ALD-Al_2O_3 deposition method, as shown in Figure S2, Supporting Information,. This implies that the T-ALD Al_2O_3 contained a higher amount of H than the PE-ALD Al_2O_3, and that a greater amount of H diffused from Al_2O_3 to a-IGZO in the stacked film with T-ALD Al_2O_3 during the annealing process. The correlation between the H content in Al_2O_3 and a-IGZO is consistent with our results. Considering the observed negative V_{TH} shift with an increase in $n_{carrier}$ from devices A to C, it is believed that the H content in a-IGZO would increase from device A to C owing to the higher proportion of H-resolved T-ALD Al_2O_3. In oxide semiconductors, H is primarily considered a shallow donor with the bonding status of H_i^+, H_O^+, and V_OH.[20–23] Furthermore, these H states can passivate the localized trap and tail states adjacent to the conduction band minimum (CBM).[47,48] However, a few groups have claimed that H can appear as deep acceptor-like bistable centers (H_i^-, H_O^-, and M–H) when the Fermi energy level (E_F) is close to that of the CBM.[20,21,49] Hence, the decrease in N_{TA} observed in device B compared with that in device A is attributable to the passivation effect on the tail states located near the CBM owing to its appropriate H content. However, the significant increases in N_{TA} and N_{GD} observed in device C, which is expected to contain an excess of H in a-IGZO, is likely due to the coexistence of acceptor-like H bistable centers caused by the elevation of E_F arising from the excess H content.

2.4. Hydrogen Resistivity and Bias Stability of ALD-IGZO TFTs with Hybrid Al_2O_3 GI

Considering the compatibility with the semiconductor device fabrication process, the devices with hybrid Al_2O_3 GI were annealed at 300 °C for 2 h under a pressure of 10 Torr using 100% H_2 concentration gas. **Figure 4**a shows the transfer characteristics of the devices before and after H_2 annealing. To clearly observe the effects of the H-annealing process, the variations in the key electrical parameters before and after H_2 annealing were compared, as shown in Figure 4b. Device A exhibited significant changes in the V_{TH}, μ_{FE}, and SS values following H_2 annealing. However, the variations in these values decreased from devices A to C; eventually, device D showed minimal changes, except for its μ_{FE}. To investigate the changes in the electrical parameters, we performed a SIMS depth profile analysis of H in the Al_2O_3/IGZO stacked films fabricated via different Al_2O_3 deposition methods, i.e., PE-ALD and T-ALD, as shown in Figure 4c. The H intensity in the a-IGZO region increased after the H_2 annealing process in the stacked film with Al_2O_3 deposited via PE-ALD as compared with the case for the Al_2O_3 deposited by T-ALD. Therefore, the degraded electrical characteristics observed in device A are believed to be caused by the increased $n_{carrier}$, N_{TA}, and N_{GD} values resulting from the higher concentration of H species in the a-IGZO layer, as shown in Figure 3e. Because of the increased top thickness of the T-ALD Al_2O_3 in the hybrid GI, the amount of H incorporated into a-IGZO after H_2 annealing decreased gradually from device A to D. However, one must understand the reason contributing to the reduced incorporation of H into the a-IGZO in the T-ALD Al_2O_3 compared with that in the PE-ALD Al_2O_3, in addition to the slight increase in μ_{FE} of device D after H_2 annealing.

The barrier properties to H_2 gas of the Al_2O_3 films obtained via PE-ALD and T-ALD were evaluated using a constant-volume/variable pressure system (time lag), as shown in **Figure 5**a. The evaluation involved monitoring the changing vacuum level over time while supplying high-pressure H_2 gas at 100% concentration from the top through the thin film to the bottom. To obtain more accurate information, 15-nm-thick Al_2O_3 films were deposited on a polyimide (PI) substrate, which is known to exhibit high permeation properties for H_2 gas. During the Al_2O_3 deposition via PE-ALD and T-ALD, the barrier properties of H_2 gas may be affected by variations in the PI surface properties. Hence, a 1 nm common layer of T-ALD Al_2O_3 was applied to both samples. Figure 5b shows a comparison of the H_2 barrier properties of the Al_2O_3 films deposited using PE-ALD and T-ALD. The T-ALD Al_2O_3 showed a lower H_2 permeability than the PE-ALD Al_2O_3, which is attributed to the high H_2 solubility and low H_2 diffusivity of the T-ALD Al_2O_3 film. This indicates that externally supplied H can readily dissolve within the T-ALD Al_2O_3 film, effectively inhibiting its diffusion toward the underlying layer. The presence of C and O species in the Al_2O_3 has been reported to enhance the barrier properties of H.[29] To confirm the changes in these species, the distributions of C and O species in the Al_2O_3 deposited using PE-ALD and T-ALD were observed via SIMS analysis. Figure S5a,b,

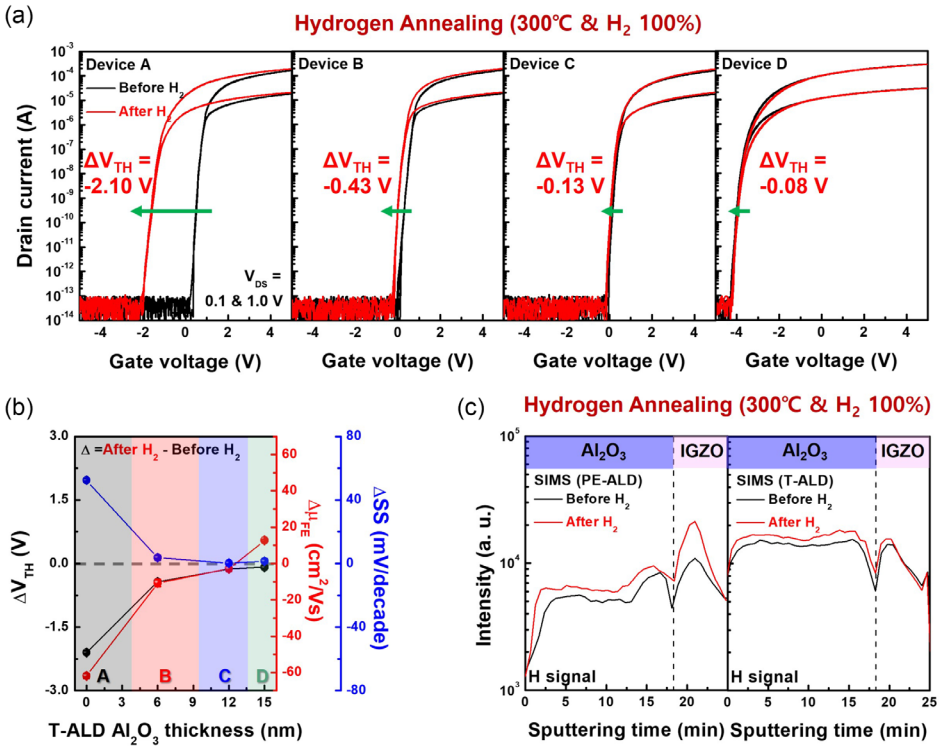

Figure 4. a) Transfer characteristics and b) changes in key electrical parameters of devices with hybrid Al_2O_3 GI before and after H_2 annealing. The average and standard deviation values of electrical properties were extracted by measuring ten devices with a size of 1 ×1 in. c) SIMS depth profile analysis of H in Al_2O_3/IGZO stacked films before and after H_2 annealing.

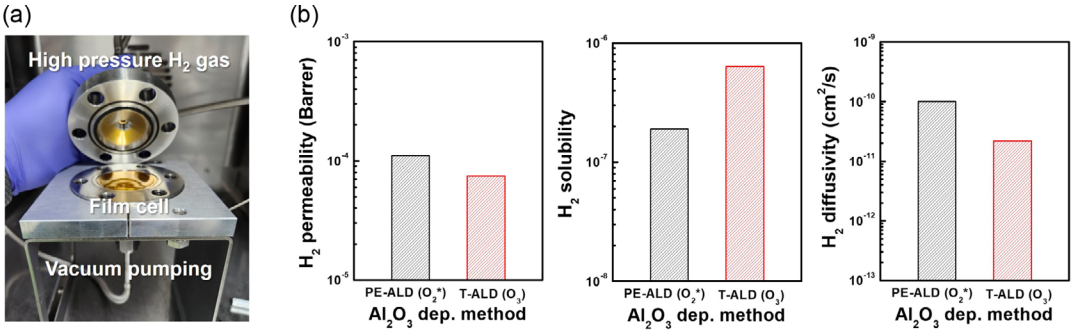

Figure 5. a) Photographs showing the time-lag system for evaluating the H_2 barrier properties of the Al_2O_3 films. b) H_2 barrier properties (permeability, solubility, and diffusivity) of Al_2O_3 films deposited via PE-ALD and T-ALD.

Supporting Information, shows the C and O signals of the Al_2O_3 films before H_2 annealing. The T-ALD Al_2O_3 exhibited higher amounts of C and O species than the PE-ALD Al_2O_3. This indicates that the H incorporated from the ambient environment into the T-ALD Al_2O_3 formed chemical bonds with the C and O elements, thus resulting in excellent H barrier properties. Hence, the lower incorporation of H into a-IGZO in the stacked film with T-ALD Al_2O_3 compared with that in the film with PE-ALD Al_2O_3 (see Figure 4c) was due to the presence of C and O species caused by limited O_3 reactivity at 200 °C for oxidizing the TMA precursor.[36,37] In addition, because the channel region of the upper a-IGZO was in contact with the well-H-resolved T-ALD Al_2O_3, the slight increase in μ_{FE} of device D after H_2 annealing is attributable to the improved carrier transport within the active channel layer.

Reliable bias stability must be ensured to guarantee the long-term use of semiconductor devices. Therefore, the devices were stressed at a gate field of ± 2 MV cm^{-1} at a temperature of 95 °C for 10 000 s. **Figure 6**a shows the transfer characteristics of the devices as a function of positive bias temperature stress (PBTS) time. Device A exhibited a positive V_{TH} shift of +0.46 V, whereas device B demonstrated a negligible V_{TH} shift of 0.00 V. Notably, the abnormal negative V_{TH} shift increased from −0.33 V in device C to −0.65 V in device D. Many groups have reported that the positive V_{TH} shift of oxide-based TFTs in PBTS environments is closely related to the O-related defects (e.g., V_O, O_i, and O_2^{2-})

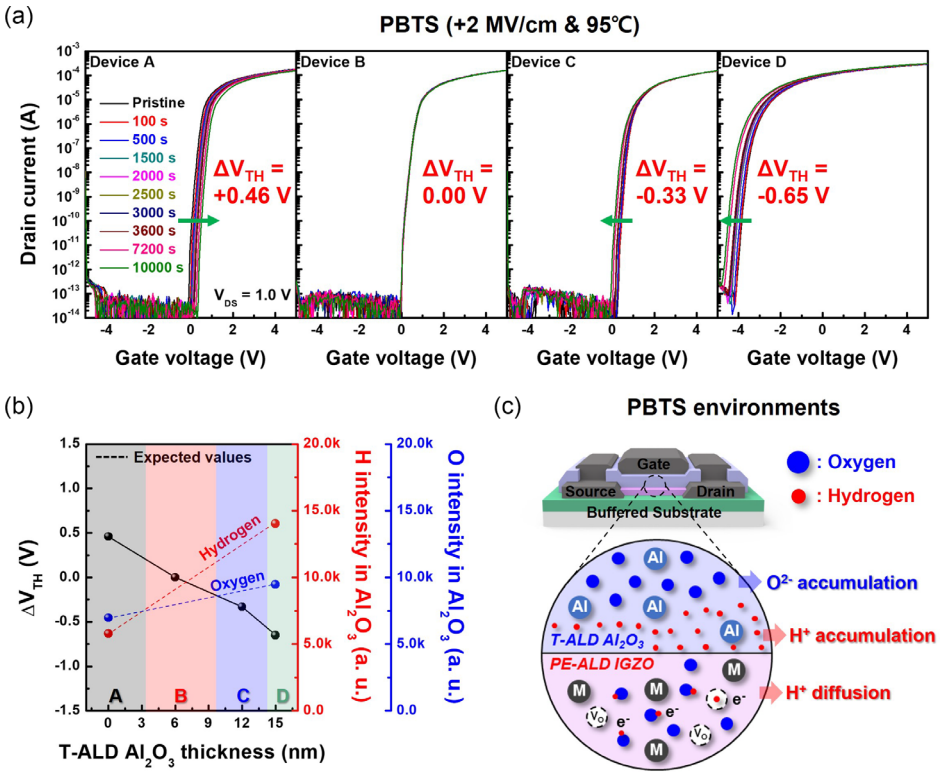

Figure 6. a) PBTS stability of devices with hybrid Al_2O_3 GI. b) Changes in V_{TH} shift after PBTS stability of devices with hybrid Al_2O_3 GI and expected values of H and O species in hybrid Al_2O_3 GI. c) Schematic illustration of migration of H and O species within T-ALD Al_2O_3 GI in PBTS environments.

in the active layer.[14–19] More specifically, among the V_O species, neutral V_O (V_O^{0+}) and 2+-charged V_O (V_O^{2+}) were identified, and the transition from V_O^{2+} to V_O^{0+} under PBTS conditions induced charge trapping. However, in some cases, devices with excess H and O species in the GI may exhibit negative V_{TH} shifts in the PBTS environment.[42,50–52] To understand the origins of the V_{TH} shifts, we compared the amounts of H and O species obtained via SIMS analysis of Al_2O_3 deposited using PE-ALD and T-ALD, as shown in Figure S2, Supporting Information. Figure 6b shows the V_{TH} shift under the PBTS conditions, in addition to the corresponding expected values of the H and O species within the GI of the devices. Considering the higher SIMS intensity of the H and O species in the T-ALD Al_2O_3 compared with that in the PE-ALD Al_2O_3, the amounts of H and O species are expected to increase progressively from devices A to D. Generally, these H and O species can exist as O^{2-} and H^+ within Al_2O_3. As shown in Figure 6c, in the case of a device with H- and O-rich T-ALD Al_2O_3, charged H and O species are likely to actively migrate within Al_2O_3 because of the positive gate bias and thermal energy in PBTS environments. Specifically, the accumulation of H^+ species at the interface between the GI and active layer can result in the generation of electron image charges at the active layer.[41] Furthermore, the diffusion of H^+ from the GI into the active layer, as facilitated by the donor-like states of H (H_i^+ and H_O^+) in oxide semiconductors, results in electron generation.[20,21] In addition to H^+ migration, O^{2-} species accumulate at the interface between the gate and GI, thus potentially serving as a screen for positive gate biases.[41] Therefore, it is believed that the transition from a positive to a negative V_{TH} shift in the devices in PBTS environments occurs predominantly because of the increased proportion of H- and O-rich T-ALD Al_2O_3. Figure S6, Supporting Information, shows the negative bias temperature stress (NBTS) results of the devices. As shown, the abnormal positive V_{TH} shifts from +0.10 V in device A to +0.49 V in device D increased gradually. In contrast to the case under the PBTS condition, H^+ is likely to accumulate at the interface between the gate and GI, whereas O^{2-} accumulates at the interface between the GI and active layer, thus resulting in a positive V_{TH} shift under NBTS conditions. Considering the increase in positive V_{TH} shifts from devices A to D in NBTS environments, we can conclude that the abnormal V_{TH} shift under the P/NBTS condition is related closely to the amounts of H and O species within the GI.

2.5. Evaluations of All-Oxide ALD-Vertical CMOS Inverter Implemented with Hybrid Al_2O_3 GI

Owing to the reliable H incorporation and bias stability exhibited by device B, we applied the latter to a novel vertically stacked CMOS structure integrated with a p-type ALD-SnO TFT to achieve high-density devices. **Figure 7**a shows a schematic illustration and the fabrication process of the ALD-vertical CMOS

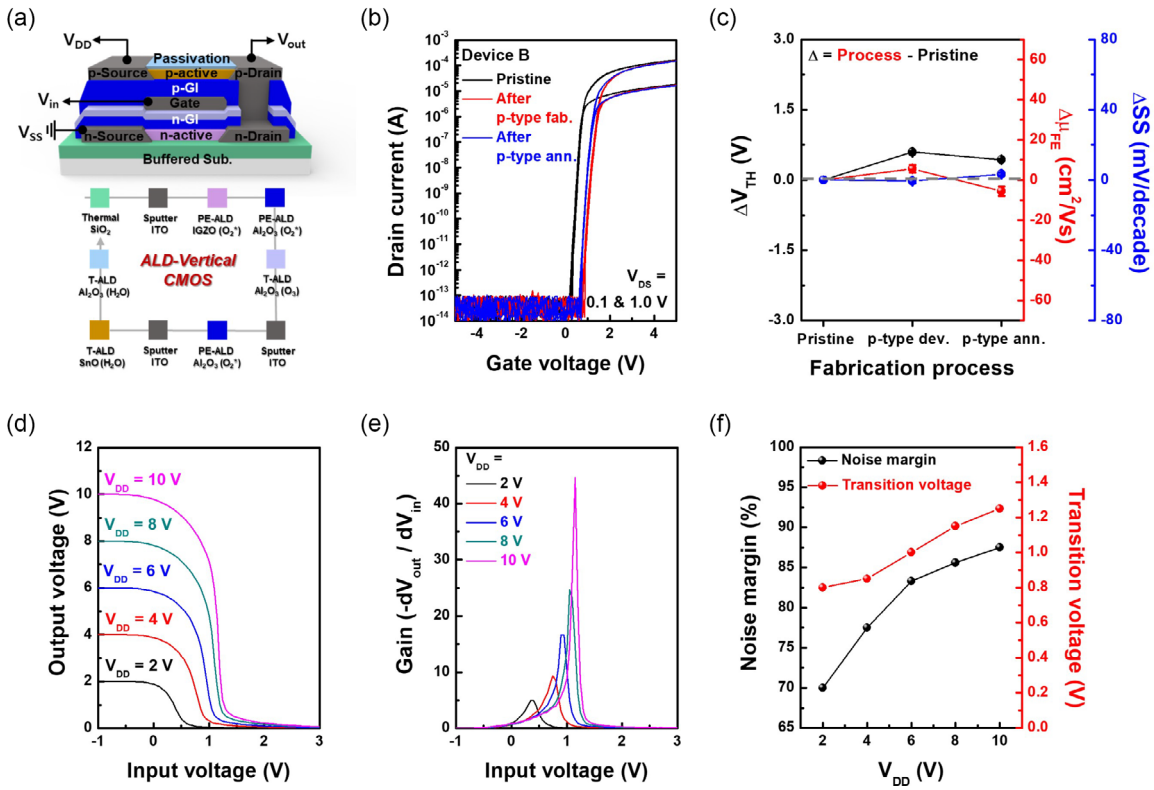

Figure 7. a) Schematic illustration of vertically stacked CMOS inverter and fabrication process. b) Comparison of transfer characteristics and c) variations in key electrical parameters of underlying n-type IGZO TFT based on the fabrication process of p-type SnO TFT. The average and standard deviation values of electrical properties were extracted by measuring ten devices with a size of 1 × 1 in. d) VTCs and e) voltage gain of vertical CMOS inverter as a function of V_{in} with increasing V_{DD}. f) Noise margin and transition voltage versus V_{DD}.

using device B. To confirm the changes in the electrical characteristics of the underlying n-type IGZO TFT, device B was measured through a step-by-step process that involved pristine measurements, followed by the fabrication and subsequent postannealing of a p-type SnO TFT. Figure 7b shows the transfer characteristics of the underlying n-type IGZO TFT based on the p-type SnO TFT fabrication process. The variations in the key electrical parameters are summarized in Figure 7c. The variations in V_{TH}, μ_{FE}, and SS were calculated to be +0.59 V, +5.6 $cm^2 Vs^{-1}$, and −0.6 mV $decade^{-1}$, respectively, after the fabrication of the p-type SnO TFT, which might have been affected by the incorporation of O radicals into the active layer during the deposition of p-type GI via PE-ALD. After the p-type SnO TFT was fabricated, RTA was performed at 300 °C for 5 min under an N_2 ambient to activate the p-type SnO TFT. Figure S7a, Supporting Information, shows that the SnO TFT exhibits conventional p-type characteristics with reasonable V_{TH}, μ_{FE}, and SS values of −1.74 V, 0.86 $cm^2 Vs^{-1}$, and 141 mV $decade^{-1}$, respectively. Because of the deposition of the p-type SnO active layer and Al_2O_3 in situ passivation layer using T-ALD with an H_2O reactant, the underlying n-type IGZO TFT was exposed to a significant amount of H during the postannealing processes. However, no significant changes in the electrical characteristics were observed in the p-type SnO TFT after postannealing processes were performed. The V_{TH}, μ_{FE}, and SS varied by −0.16 V, +11.1 $cm^2 Vs^{-1}$, and 3.9 mV $decade^{-1}$, respectively, which is attributable to the excellent tolerance of the H incorporation of device B with the hybrid Al_2O_3 GI, as shown in Figure 4a. Figure 7d,e shows the voltage transfer characteristics (VTCs) and voltage gain of the all-oxide ALD vertically stacked CMOS inverter as a function of the input voltage (V_{IN}), respectively. Based on the VTCs of the CMOS with a supply voltage (V_{DD}) ranging from 2 to 10 V, the CMOS exhibited clear rail-to-rail inverter output curves. The voltage gain ($-dV_{out}/dV_{in}$) increased with V_{DD} and exhibited a maximum value of 44.7 $V V^{-1}$ at a V_{DD} of 10 V (Figure S7b, Supporting Information. Figure 7f shows the noise margin and transition voltage extracted from the output voltage (V_{out}) as a function of V_{in}. The noise margin was calculated as follows

$$\text{Noise margin}\ (\%) = \frac{NM_H + NM_L}{V_{DD}} \quad (1)$$

where NM_H and NM_L are the high and low noise margins, respectively. The NM_H and NM_L were calculated using the logical high-output voltage ($V_{OH} = V_{DD}$)–input voltage (V_{IH}) and logical low-input voltage (V_{IL})–output voltage ($V_{OL} = 0$ V), respectively. The V_{IH} and V_{IL} values were determined from the high and low input voltage values at the −1 $V V^{-1}$ gain value, respectively. NM_H and NM_L as a function of V_{DD} are presented in Figure S7c, Supporting Information,. In addition, the transition voltage was extracted from V_{in}, where $V_{in} = V_{out}$. An increase in the noise margin and a positive shift in the transition voltage were observed as V_{DD} increased. The noise margin and transition voltage exhibited reasonable values of 87.5% and 1.25 V, respectively, at a $V_{DD} = 10$ V.

3. Conclusion

We successfully fabricated TG-BC ALD-IGZO TFTs that demonstrated bias stability, H incorporation, and extremely high mobility through hybrid GI deposition via in situ PE-ALD and T-ALD processes. To precisely modulate H, C, and O species within the Al_2O_3 layer, we designed a hybrid Al_2O_3 GI structure by adopting in situ PE-ALD and T-ALD processes. The device with a hybrid Al_2O_3 GI exhibited exceptional electrical characteristics, including a V_{TH} of 0.37 V, μ_{FE} of 150.7 $cm^2 Vs^{-1}$, SS of 64.0 mV $decade^{-1}$, and hysteresis of 0.02 V at a specific T-ALD Al_2O_3 thickness of 6 nm. The passivation effect on the tail states located near the CBM is attributed to the diffusion of the appropriate H content from the GI into the active layer. We annealed the fabricated devices at 300 °C for 2 h under a pressure of 10 Torr using 100% H_2 concentration gas. The device with a hybrid Al_2O_3 GI exhibited a reduced degree of negative V_{TH} shifts from −2.10 to −0.08 V as the T-ALD Al_2O_3 thickness increased. In addition, the devices were tested for PBTS stability under a gate field of +2 MV cm^{-1} at a temperature of 95 °C for 10 000 s. The devices exhibited a transition from positive to negative V_{TH} shifts under PBTS stability as the thickness of the T-ALD Al_2O_3 increased. These results were primarily attributed to the increase in H, C, and O species in the hybrid GI with the T-ALD Al_2O_3 thickness. Device B with excellent electrical characteristics indicates variations in the V_{TH} shift of −0.43 and 0.00 V for the H_2 annealing process and PBTS stability, respectively. Finally, device B was utilized in a novel vertically stacked CMOS inverter to achieve high-density devices. The all-oxide vertical CMOS exhibited clear inverter characteristics, such as a voltage gain of 44.7 $V V^{-1}$ and a noise margin of 87.5% at a V_{DD} of 10 V.

4. Experimental Section

ALD-IGZO Active Layer Deposition: To obtain the IGZO active layer, we utilized a lateral flow-type PE-ALD system with a radio frequency (RF) (13.56 MHz) direct capacitance-coupled plasma (CCP) source (ISAC Research Inc.) in a 6″ × 6″ chamber. During deposition, a constant flow of argon (Ar) (purity: 99.999%) was maintained in the chamber to regulate the operating pressure at 1.2 Torr using a throttle valve. The In, Ga, and Zn precursors used were (3-dimethylaminopropyl)dimethylindium (DADI), trimethylgallium (TMGa), and diethylzinc (DEZ). Considering the vapor pressures of the precursors, the canister temperatures for DADI and TMGa were adjusted to 55 and 15 °C, respectively. The DADI precursor was transported to the reaction chamber via Ar as a carrier gas. The chemical reaction was realized using oxygen (O_2) (purity: 99.999%) plasma with a power of 100 W at 200 °C. Supercycling was employed to deposit the active IGZO layer. The cation composition of IGZO, as determined via X-Ray fluorescence spectrometry (XRF), was confirmed to be $In_{0.71}Ga_{0.08}Zn_{0.21}O$.

ALD-Al_2O_3 GI Deposition: A vertical flow-type ALD chamber (ISAC Research Inc.) measuring 6″ × 6″ was used to deposit the Al_2O_3 film. The ALD chamber was equipped with a RF (13.56 MHz) direct CCP source. Ar (purity: 99.999%) was used as the carrier gas during the deposition process. The operating pressure was set to 1.2 Torr for the PE-ALD process and 350 mTorr for the T-ALD process using a throttle valve. TMA was used as the Al precursor. To oxidize the TMA precursor, either O_2 (purity: 99.999%) plasma with a power of 100 W or ozone (O_3) with a concentration of 200 g m^{-3}, generated via an O_3 generator (CN-1, Ozonetech Co.), was employed at a temperature of 200 °C. The durations of O_2 plasma ignition and O_3 dosing were set to 1 and 5 s, respectively. To evaluate

the electrical properties of Al_2O_3 deposited via the PE-ALD and T-ALD processes, we fabricated MIM structures. These structures were fabricated on a highly boron-doped Si wafer with an Al_2O_3 layer deposited on it. Additionally, a 100-nm-thick indium tin oxide (ITO) electrode was applied using RF sputtering. The ITO electrode was patterned to cover a 100 μm × 100 μm area using conventional photography methods. A schematic illustration of the ALD-Al_2O_3 process is shown in Figure 1a.

TG-BC ALD-IGZO TFTs Fabrication: The device fabrication process began with the ultrasonic cleaning of a thermally-grown 100 nm-thick SiO_2 buffered substrate using acetone, ethanol, and deionized water, in that particular sequence. To define the source and drain regions, a 100 nm-thick ITO electrode was deposited using RF sputtering and then patterned via photolithography. Subsequently, a 10 nm-thick IGZO active layer was deposited via PE-ALD. The active layer was then defined using conventional photolithography followed by wet etching. For the GI, a 15 nm-thick Al_2O_3 was deposited using PE-ALD, T-ALD, as well as in situ PE-ALD and T-ALD processes, and contact holes for the source/drain were created via wet etching. To deposit the gate electrode, a 100 nm-thick ITO electrode was deposited and patterned via photolithography. The channel width and length of the fabricated device were 40 and 20 μm, respectively. Finally, the devices were postannealed at 350 °C for 2 h under dry air (O_2 21%/N_2 79%, purity: 99.999%). The fabrication process of the TG-BC ALD-IGZO TFTs is shown in Figure 2a.

Fabrication of Vertically Stacked All-Oxide ALD CMOS Inverter: A vertically stacked CMOS inverter integrated with a p-type ALD-SnO TFT was fabricated to achieve high-density devices. For the bottom gate-bottom contact p-type SnO TFT, a 15 nm-thick layer of Al_2O_3 was deposited using PE-ALD to serve as the GI on the n-type device. The n-type device was an IGZO TFT with a hybrid GI composed of Al_2O_3 layers deposited using T-ALD and PE-ALD with thicknesses of 6 and 9 nm, respectively. Next, the contact hole for the n-type drain electrode was created via wet etching, and a 100 nm-thick ITO electrode was deposited via RF sputtering. The in situ ALD-stacked 10 and 7 nm-thick Al_2O_3/SnO layers were deposited as capping and p-type channel layers, respectively. The detailed fabrication process and deposition conditions of the p-type in situ Al_2O_3/SnO device are available in our previous report.[53] The contact holes, electrodes, and active layers were defined using photolithography. A schematic illustration of the fabricated vertical CMOS structure is shown in Figure 7a. The inverter characteristics were obtained with channel width and length of 40/60 and 40/20 μm for the n-type IGZO and p-type SnO TFTs, respectively.

Characterization: The cation atomic composition of IGZO was determined via energy-dispersive XRF (ARL QUANT'X, Thermo Scientific). The chemical bonds of O and C in the Al_2O_3 bulk region were analyzed using XPS (K-alpha$^+$, Thermo Fisher Scientific) with a monochromatic aluminum (Al) Kα (1486.6 eV) source. The density of the deposited Al_2O_3 films, which were fabricated via PE-ALD and T-ALD, was obtained via grazing incidence-XRR (SmartLab, Rigaku) using a Cu-Kα (1.5405 Å) target. To investigate the variations in the Al, O, H, and C signals in the Al_2O_3/IGZO stacked films, dynamic SIMS (IMS-7 F_Auto, CAMECA, UK) was conducted using a cesium (Cs^+) ion source at 6 keV. Cross-sectional information regarding the Al_2O_3/IGZO stacked films were obtained via TEM and EDS line scans using high-resolution TEM (Talos F200X, Thermo Fisher Scientific). TCAD was used to identify the relationship between the electrical characteristics and DOS. The gas permeation properties were evaluated using a constant-volume/variable pressure system (time lag, Airrane). The film was subjected to a 100% H_2 gas with a pressure of 6500 Torr at a temperature of 35 °C. The measurements were terminated when the downstream pressure reached 2 Torr. The electrical characteristics of the devices were evaluated in a dark environment using a TOP Engineering S3000 electrical parameter analyzer. The dielectric constant of Al_2O_3 was measured using an Agilent 4284 A precision LCR meter.

Statical Analysis: The V_{TH} was determined using the constant-current method, characterized by $V_{TH} = V_{GS}@I_{DS} = \left(\frac{W}{L}\right) \times 100\text{pA}$, where V_{GS} is the gate voltage, I_{DS} is the drain current, W is the channel width, and L is the channel length. The μ_{FE} of the transistors was estimated by the linear transfer characteristics as $\mu_{FE} = g_{m(max)} \times \left(\frac{L}{W}\right) \times \frac{1}{C_{ox}} \times \frac{1}{V_{DS}}$, where $g_{m(max)}$ is the maximum transconductance, C_{ox} is the oxide capacitance of the GI, and V_{DS} is the drain voltage. The SS was calculated using the following equation: $SS = \frac{d(V_{GS})}{d\log(I_{DS})}$. The hysteresis was extracted by the difference of V_{TH} between the forward and reverse sweep of the transfer curve. These key electrical parameters are expressed in the format of "average ± standard deviation". The average and standard deviation values of electrical properties were extracted by measuring ten devices with a size of 1 ×1 in.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

atomic layer deposition, hydrogen resistivity, oxide semiconductors, stability, thin-film transistors, vertical complementary metal-oxide-semiconductor inverter

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[1] T. Kamiya, H. Hosono, *NPG Asia Mater.* **2010**, *2*, 15.
[2] J. S. Park, W.-J. Maeng, H.-S. Kim, J.-S. Park, *Thin Solid Films* **2012**, *520*, 1679.
[3] T. Kamiya, K. Nomura, H. Hosono, *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305.
[4] Y. Hara, T. Kikuchi, H. Kitagawa, J. Morinaga, H. Ohgami, H. Imai, T. Daitoh, T. Matsuo, *J. Soc. Inf. Disp.* **2018**, *26*, 169.
[5] J. F. Wager, *Inf. Disp.* **2014**, *30*, 26.
[6] K. Kato, H. Kobayashi, H. Shishido, T. Isa, T. Aoyama, Y. Jimbo, R. Hodo, K. Kusunoki, H. Kunitake, S. Yamazaki, *J. Soc. Inf. Disp.* **2022**, *30*, 690.
[7] H. C. M. Knoops, S. E. Potts, A. A. Bol, W. M. M. Kessels, *Handb. Cryst. Growth* **2015**, 1101.
[8] R. G. Gordon, D. Hausmann, E. Kim, J. Shepard, *Chem. Vap. Deposition* **2003**, *9*, 73.
[9] K. Arts, H. Thepass, M. A. Verheijen, R. L. Puurunen, W. M. M. Kessels, H. C. M. Knoops, *Chem. Mater.* **2021**, *33*, 5002.

[10] W. Tang, Z. Wang, Z. Lin, L. Feng, Z. Liu, X. Li, P. D. Ye, X. Guo, M. Si, *2022 Int. Electron Devices Meet. IEEE* **2022**, p. 483, https://doi.org/10.1109/IEDM45625.2022.10019410.
[11] X. Duan, K. Huang, J. Feng, J. Niu, H. Qin, S. Yin, G. Jiao, D. Leonelli, X. Zhao, Z. Wang, W. Jing, Z. Wang, Y. Wu, J. Xu, Q. Chen, X. Chuai, C. Lu, W. Wang, G. Yang, D. Geng, L. Li, M. Liu, *IEEE Trans. Electron Devices* **2022**, *69*, 2196.
[12] X. Duan, K. Huang, J. Feng, Y. Sun, C. Lu, C. Chen, G. Jiao, X. Lin, J. Shao, S. Yin, J. Sheng, Z. Wang, W. Zhang, X. Chuai, J. Niu, W. Wang, Y. Wu, W. Jing, Z. Wang, J. Xu, G. Yang, D. Geng, L. Li, M. Liu, *2022 IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, IEEE, Piscataway, NJ **2022**, 296.
[13] S. Choi, M. Kang, Y.-H. Song, *Electronics* **2023**, *12*, 2945.
[14] A. Janotti, C. G. Van De Walle, *Appl. Phys. Lett.* **2005**, *87*, 122102.
[15] A. Janotti, C. G. Van de Walle, *Phys. Rev. B* **2007**, *76*, 165202.
[16] W. H. Han, Y. J. Oh, K. J. Chang, J.-S. Park, *Phys. Rev. Appl.* **2015**, *3*, 044008.
[17] K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* **2011**, *99*, 093507.
[18] H.-H. Nahm, Y.-S. Kim, D. H. Kim, *Phys. Status Solidi RRL* **2012**, *249*, 1277.
[19] S. Choi, J. Park, S.-H. Hwang, C. Kim, Y.-S. Kim, S. Oh, J. H. Baeck, J. U. Bae, J. Noh, S.-W. Lee, K.-S. Park, J.-J. Kim, S. Y. Yoon, H.-I. Kwon, D. H. Kim, *Adv. Electron. Mater.* **2022**, *8*, 2101062.
[20] H.-H. Nahm, C. H. Park, Y.-S. Kim, *Sci. Rep.* **2014**, *4*, 4124.
[21] Y. Kang, B. Du Ahn, J. H. Song, Y. G. Mo, H.-H. Nahm, S. Han, J. K. Jeong, *Adv. Electron. Mater.* **2015**, *1*, 1400006.
[22] G. Li, A. Abliz, L. Xu, N. André, X. Liu, Y. Zeng, D. Flandre, L. Liao, *Appl. Phys. Lett.* **2018**, *112*, 253504.
[23] M. Nakashima, M. Oota, N. Ishihara, Y. Nonaka, T. Hirohashi, M. Takahashi, S. Yamazaki, T. Obonai, Y. Hosaka, J. Koezuka, *J. Appl. Phys.* **2014**, *116*, 213703.
[24] T. Toda, D. Wang, J. Jiang, M. P. Hung, M. Furuta, *IEEE Trans. Electron Devices* **2014**, *61*, 3762.
[25] K.-L. Han, K.-C. Ok, H.-S. Cho, S. Oh, J.-S. Park, *Appl. Phys. Lett.* **2017**, *111*, 063502.
[26] G. Franz, *Phys. Status Solidi RRL* **1997**, *159*, 137.
[27] T. Seo, H. Park, G. Jeon, J. Yun, S. Park, S. Seong, Y. Chung, *ACS Appl. Electron. Mater.* **2020**, *2*, 3320.
[28] W. Wu, X. Lei, S. Zhong, B. Sun, C. Ouyang, *Appl. Surf. Sci.* **2020**, *531*, 147263.
[29] Y. Lee, T. Nam, S. Seo, H. Yoon, I.-K. Oh, C. H. Lee, H. Yoo, H. J. Kim, W. Choi, S. Im, J. Y. Yang, D. W. Choi, C. Yoo, H.-J. Kim, H. Kim, *ACS Appl. Mater. Interfaces* **2021**, *13*, 20349.
[30] D. Liu, S. J. Clark, J. Robertson, *Appl. Phys. Lett.* **2010**, *96*, 032905.
[31] M. Uenuma, K. Takahashi, S. Sonehara, Y. Tominaga, Y. Fujimoto, Y. Ishikawa, Y. Uraoka, *AIP Adv.* **2018**, *8*, 105103.
[32] A. Pirkle, S. McDonnell, B. Lee, J. Kim, L. Colombo, R. M. Wallace, *Appl. Phys. Lett.* **2010**, *97*, 082901.
[33] H. Choi, S. Lee, H. Jung, S. Shin, G. Ham, H. Seo, H. Jeon, *Jpn. J. Appl. Phys.* **2013**, *52*, 035502.
[34] K. S. Yoo, D.-G. Kim, S. Lee, W.-B. Lee, J.-S. Park, *Ceram. Int.* **2022**, *48*, 18803.
[35] S. Pletincx, L. Trotochaud, L. L. Fockaert, J. M. C. Mol, A. R. Head, O. Karslloğlu, H. Bluhm, H. Terryn, T. Hauffman, *Sci. Rep.* **2017**, *7*, 45123.
[36] V. R. Rai, V. Vandalon, S. Agarwal, *Langmuir* **2010**, *26*, 13732.
[37] S. D. Elliott, G. Scarel, C. Wiemer, M. Fanciulli, G. Pavia, *Chem. Mater.* **2006**, *18*, 3764.
[38] Y.-S. Kim, H.-J. Oh, J. Kim, J. H. Lim, J.-S. Park, *Small Methods* **2023**, *7*, 2300549.
[39] D.-G. Kim, H. Choi, Y.-S. Kim, D.-H. Lee, H.-J. Oh, J. H. Lee, J. Kim, S. Lee, B. Kuh, T. Kim, H. Y. Kim, J.-S. Park, *ACS Appl. Mater. Interfaces* **2023**, *15*, 31652.
[40] J. B. Ko, S.-H. Lee, K. W. Park, S.-H. K. Park, *RSC Adv.* **2019**, *9*, 36293.
[41] C. H. Choi, T. Kim, S. Ueda, Y.-S. Shiah, H. Hosono, J. Kim, J. K. Jeong, *ACS Appl. Mater. Interfaces* **2021**, *13*, 28451.
[42] S.-I. Cho, J. B. Ko, S. H. Lee, J. Kim, S.-H. K. Park, *J. Alloys Compd.* **2022**, *893*, 162308.
[43] J. Li, Y. Zhang, J. Wang, H. Yang, X. Zhou, M. Chan, X. Wang, L. Lu, S. Zhang, *ACS Appl. Mater. Interfaces* **2023**, *15*, 8666.
[44] S. Lee, M. Kim, G. Mun, J. Ko, H.-I. Yeom, G.-H. Lee, B. Shong, S.-H. K. Park, *ACS Appl. Mater. Interfaces* **2021**, *13*, 40134.
[45] J. Park, Y. Lim, M. Jang, S. Choi, N. Hwang, M. Yi, *Mater. Res. Bull.* **2017**, *96*, 155.
[46] S.-H. Lee, K. Kwon, K. Kim, J. S. Yoon, D.-S. Choi, Y. Yoo, C. Kim, S. Kang, J. H. Kim, *Materials* **2019**, *12*, 137.
[47] Y. Hanyu, K. Abe, K. Domen, K. Nomura, H. Hiramatsu, H. Kumomi, H. Hosono, T. Kamiya, *J. Disp. Technol.* **2014**, *10*, 979.
[48] H.-J. Jeong, Y.-S. Kim, S.-G. Jeong, J.-S. Park, *ACS Appl. Electron. Mater.* **2022**, *4*, 1343.
[49] N. On, Y. Kang, A. Song, B. Du Ahn, H. D. Kim, J. H. Lim, K.-B. Chung, S. Han, J. K. Jeong, *IEEE Trans. Electron Devices* **2017**, *64*, 4965.
[50] D.-G. Kim, W.-B. Lee, S. Lee, J. Koh, B. Kuh, J.-S. Park, *ACS Appl. Mater. Interfaces* **2023**, *15*, 36550.
[51] Y.-H. Chang, M.-J. Yu, R.-P. Lin, C.-P. Hsu, T.-H. Hou, *Appl. Phys. Lett.* **2016**, *108*, 033502.
[52] M.-H. Kim, J. Park, J.-H. Lim, D.-K. Choi, *Phys. Status Solidi RRL* **2019**, *216*, 1900297.
[53] H.-M. Kim, S.-H. Choi, H. U. Lee, S. B. Cho, J.-S. Park, *Adv. Electron. Mater.* **2023**, *9*, 2201202.