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Comparison of Bi-Directional Topologies for On-Board Charger: A 10.9 kW High-Efficiency High Power Density of DC-DC Stage

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Abstract: In recent years, the trend in power electronics has been toward high-efficiency and high-power-density converters. Additionally, this trend has allowed electric vehicles to accommodate larger batteries, which necessitate bi-directional capabilities not only for driving but also for vehicle to grid (V2G), etc. This article proposes a comparative analysis of GaN-based bi-directional topologies, namely the dual active bridge (DAB) converter and the CLLC converter. To ensure a fair analysis of the proposed topologies, prototypes with the same target of efficiency above 97.5% and a power density of 5.5 kW/L have been constructed. This research can support the adoption of 10.9 kW bi-directional topologies in GaN-based on-board chargers (OBCs) for EVs.

Keywords: DC-DC converter; electric vehicles; on-board charger; dual active bridge converter; CLLC resonant converter

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1. Introduction

Major agreements such as the Paris Agreement and COP 28 have been signed to solve the problem of climate change caused by carbon and greenhouse gas (GHG) emissions [1–13]. In particular, the road transportation sector is highly dependent on fossil fuels and accounts for about 77% of global transport-related GHG emissions [6]. For this reason, the Inland Transportation Commission (ITC) of UNECE recommended the adoption of EVs [5,6], so the demand for EVs is increasing [4]. In addition, the high efficiency and high power density of the EVs' power conversion system are important to reduce energy consumption [9–29]. High efficiency can reduce energy loss in the process of transmitting power and increase the stability of the system through less heat generation. Also, since EVs are equipped with batteries, high power density is required due to spatial limitations.

Several studies have been carried out on on-board chargers (OBCs) [14–25], but they focus on unidirectional power conversion. Recently, OBCs were adopted with a bi-directional topology, such as vehicle to grid (V2G) and vehicle to load (V2L), to use energy efficiently. Representative bi-directional topologies are dual active bridge (DAB) and CLLC converters. These topologies have the advantages of wide input/output voltage range and low voltage stress, so they are widely adopted in OBCs.

In [26], a 3.3 kW/500 kHz DAB was proposed as the OBC DC-DC stage. It was designed as follows to satisfy the requirements of a high efficiency and high power density:

1. Bare-Die SiC MOSFETs of 4 mm × 6 mm size were applied instead of a conventional packaged switch. The developed switch module has low switching loss and low oscillations due to its low parasitic composition, which can operate at high frequency.
2. The volume was reduced by using the leakage inductance of a planar transformer without using an additional inductor. Zero voltage switching (ZVS) was achieved in the battery voltage range of 250–380 V, and the final prototype had a power density of

5.44 kW/L. Using a DAB, up to 98% efficiency was satisfied in the constant power (CP) section.

In [28], bi-directional power conversion was reviewed by applying CLLC. In order to increase the efficiency and power density, the following proposal was made:

1. Loss reduction was produced through soft switching and synchronous rectification (SR). Through SR driving, the efficiency increased by up to 1.7%.
2. An integrated transformer using leakage inductance was proposed. As a result, efficiencies of 97.5% and 97.3% were satisfied in grid to vehicle (G2V) and V2G.

In [30], a 1 kW OBC system using SiC MOSFETs was implemented with both a DAB and CLLC designed as a full-bridge and half-bridge, respectively. However, additional inductors were designed without the transformer's leakage inductance.

The abovementioned articles have been studied on only one topology or comparing two topologies without the same constraints such as high power density. In addition, the design directions for each conventional topology have not been compared and presented. Therefore, this article proposes a comparative analysis of typical DAB and CLLC converters in charging mode at 5.5 kW/L and, 10.9 kW using the transformer's leakage inductance. Section 2 provides a theoretical analysis of the conventional DAB and CLLC converters. Section 3 discusses the design direction of each topology and each transformer. The experimental results and an analysis of the experimental results are provided in Sections 4 and 5, respectively. Finally, Section 6 provides the conclusion of this article.

2. Operation Principles

This article focuses on the charging of the dual active bridge (DAB) and CLLC converters. Figure 1 shows each topology which has a similar structure. But the CLLC includes a resonant capacitor C_R in tanks on each side The tanks on each side are expressed as A to D in Figure 1. This section discusses the operating principle of each topology and a comparative analysis.

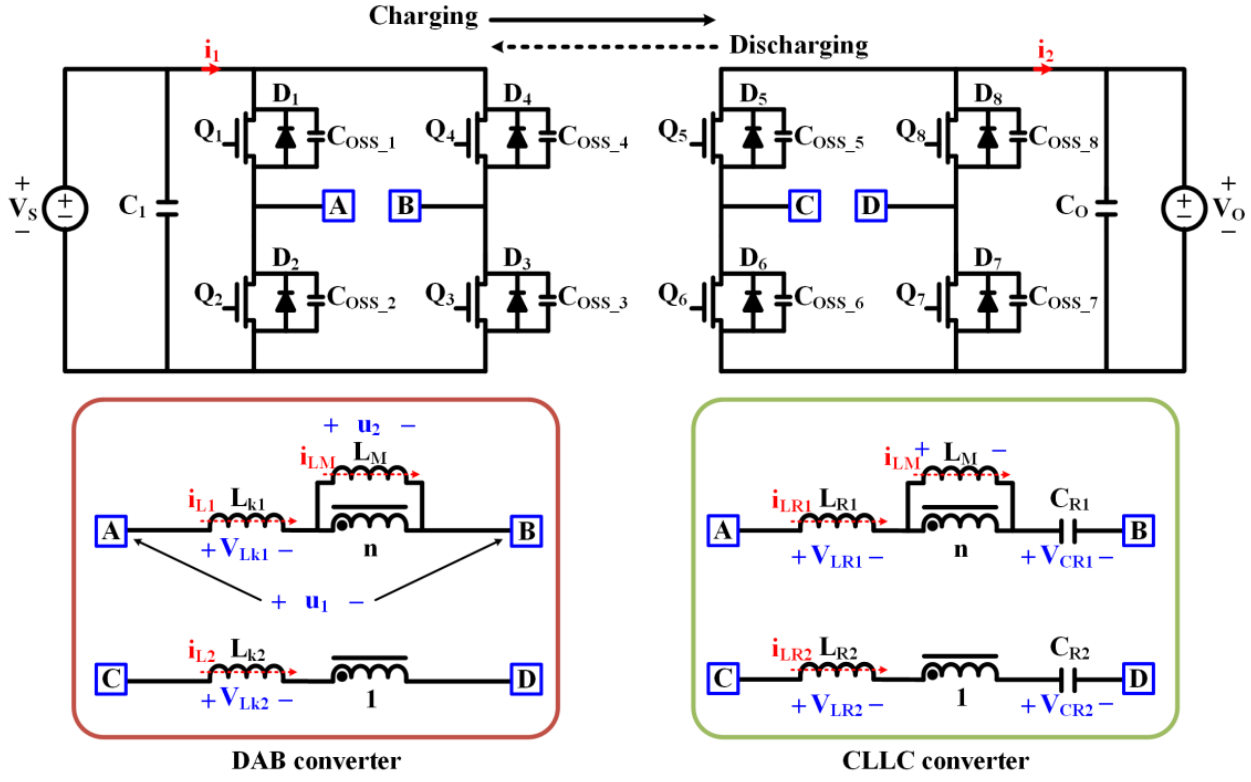


Figure 1. The circuit diagram of each topology.

2.1. DAB Converter

The DAB has the advantage of bi-directional power conversion with a few components. As shown in Figure 2, the power is transferred through the equivalent leakage inductance L_{eq}, which is $L_{eq} = L_{k1} + L_{k2}/n^2$. L_{eq} can be designed with lower inductance than hard-switching topologies such as buck converters and boost converters. Therefore, the DAB can achieve high power density while ensuring isolation.

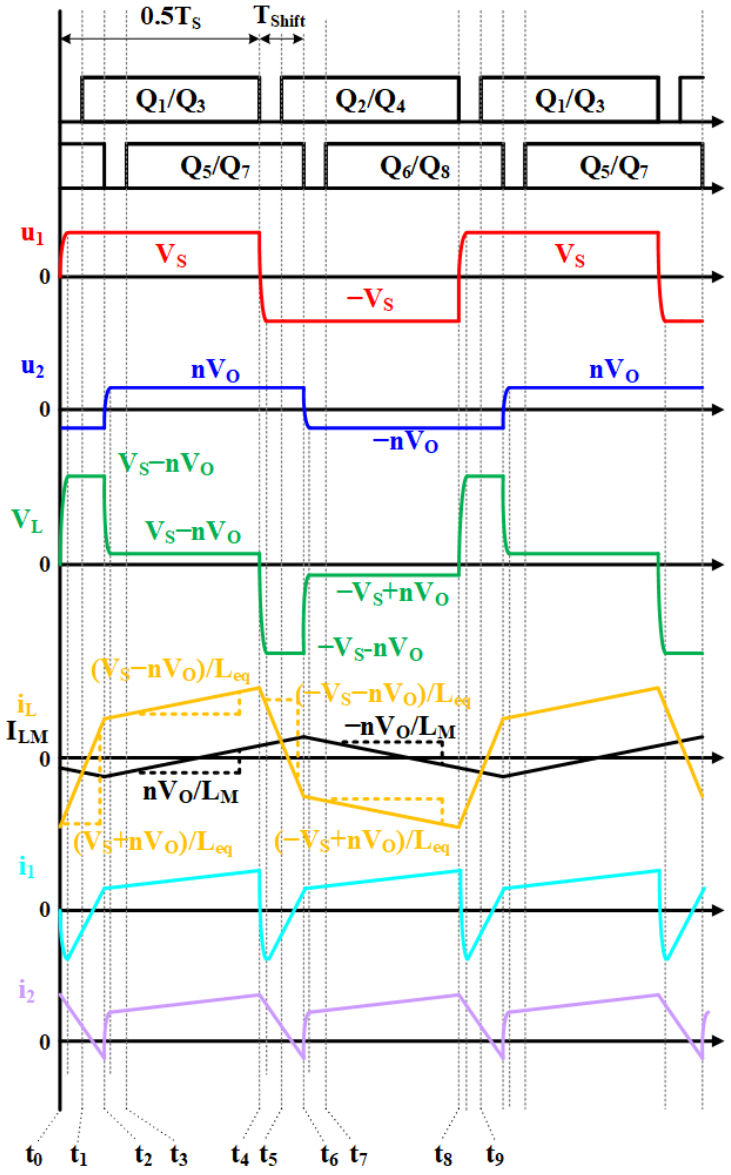


Figure 2. The key waveforms of DAB.

For ease of mode analysis in the DAB, the following assumptions are made:

1. The input and output voltage V_S, V_O is constant.
2. The output capacitance C_O is very large.
3. The magnetizing inductance L_M is significantly larger than the L_{eq}.
4. The duty cycle of the DAB is denoted as D_{DAB} and is defined as $T_{shift}/0.5T_S$.
5. The range of D_{DAB} is 0 to 0.5.

Mode 1 [t_0–t_2]: In Mode 1, Q_1, Q_3, Q_6 and Q_8 are in the turn-on state during the interval $t_1 - t_2$. The voltage $V_S + nV_O$ is applied to L_{eq}, and the secondary projected voltage u_2 is $-nV_O$, applied to L_M; i_L and i_{LM} increase/decrease linearly, where n is a turn ratio. In

this case, the slope of i_L is $(V_S+nV_O)/L_{eq}$. During the interval t_0–t_1, primary side ZVS can be achieved if the current $i_L(t_0)$ is negative.

Mode 2 [t_2–t_4]: In Mode 2, Q_1, Q_3, Q_5 and Q_7 are in the turn-on state. The voltage V_S-nV_O is applied to L_{eq}, and the secondary reflected voltage u_2 is equal to nV_O and is applied to L_M; both i_L and i_{LM} increase linearly. In this case, the slope of i_L is $(V_S-nV_O)/L_{eq}$. During the interval t_2–t_3, secondary ZVS can be achieved when the value of $i_L(t_2)$ is positive.

Mode 3 [t_4–t_6] is omitted because it is symmetric to that in Mode 1.

The output power P_O and gain M of the DAB can be derived as follows:

$$P_O = \frac{nV_SV_O}{2f_sL_{eq}}D_{DAB}(1-D_{DAB}) = \frac{V_O^2}{R_L} \tag{1}$$

$$M = \frac{V_O}{V_s} = \frac{1}{n}\cdot\frac{R_L}{2f_sL_{eq}}D_{DAB}(1-D_{DAB}) \tag{2}$$

f_s is the switching frequency. The soft-switching conditions in a DAB are shown in Figure 3. ZVS is achieved on both the primary and secondary sides when the $i_L(t_0)$ is negative and $i_L(t_2)$ is positive. Therefore, design points should not be included in the highlighted part of the curve below. If the design satisfies these conditions but lacks sufficient ZVS energy, switch turn-on loss may occur. It is important to satisfy the energy equation for ZVS during the period in which the switch is turned off. The equation is derived as follows:

$$\frac{1}{2}L_{eq}\left(i_{L,toff}\right)^2 \geq \frac{1}{2}(4C_{oss})V^2 \tag{3}$$

where C_{oss} is the output capacitance in FETs. In Equation (3), V is calculated as the input and output voltages, respectively.

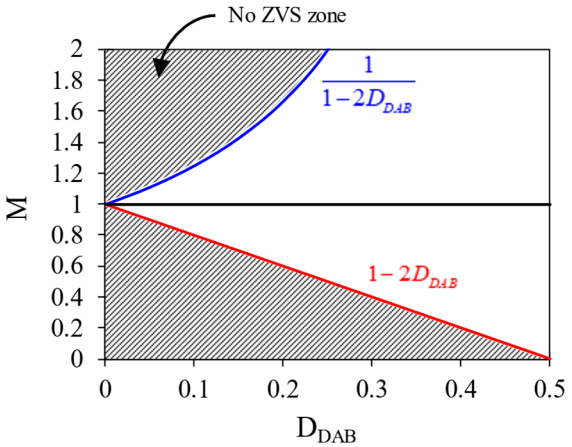


Figure 3. ZVS region as M and D_{DAB}.

2.2. CLLC Converter

As shown in Figure 1, the CLLC consists of two resonant inductors and two resonant capacitors positioned on both the primary and secondary sides. The capacitors store energy and transfer it during the switching intervals, and the inductors form resonant circuits to achieve ZVS. Similarly to the DAB, the CLLC's inductance can be substituted by the transformer's leakage inductance. CLLC has a wide range of control of the battery voltage and facilitates soft switching of all switches over the entire load range.

For ease of mode analysis in the CLLC, the following assumptions are made:

1. The input and output voltage V_S, V_O is constant.
2. The output capacitance C_O is very large.

3. Instead of secondary side FETs switching, operation relies on the body diode, which is considered ideal.

The key waveforms in the boost operation of CLLC are shown in Figure 4a. In this operation, the switching frequency f_s is lower than the resonant frequency f_r ($f_s < f_r$: below region).

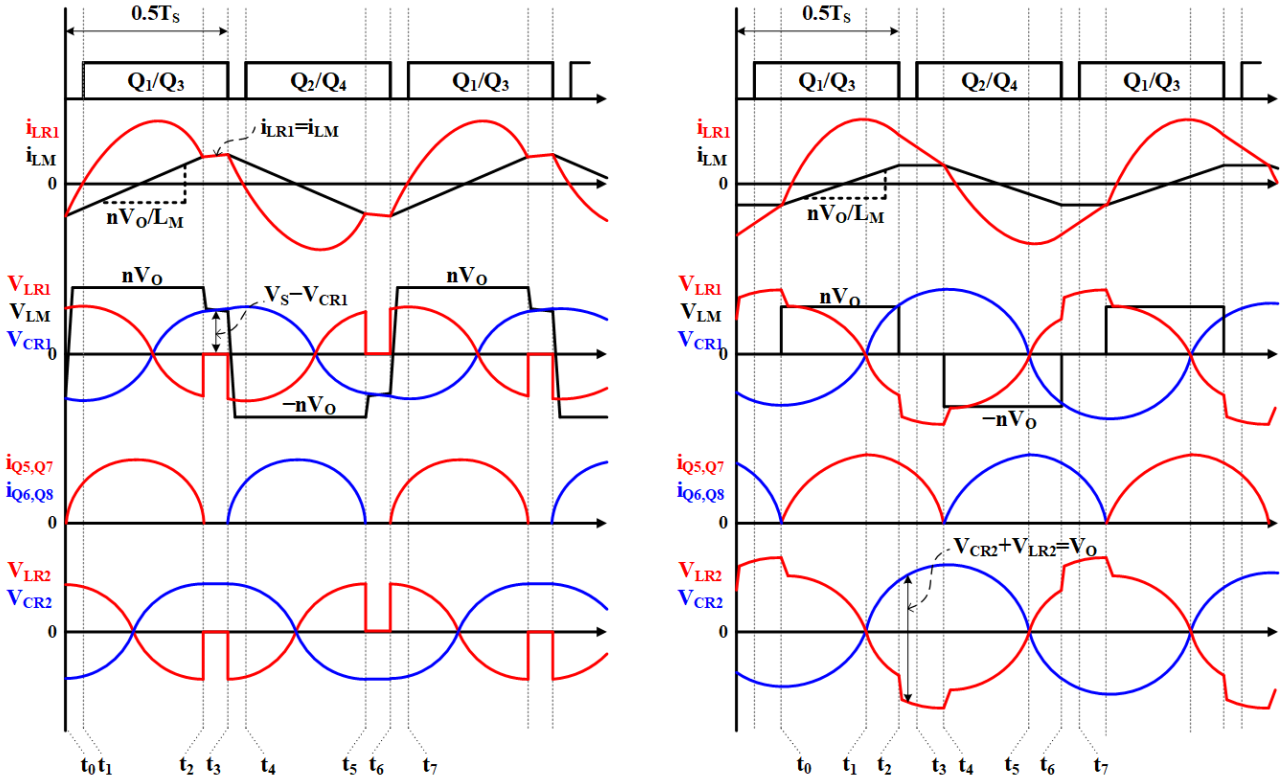


Figure 4. The key waveforms of CLLC: (**a**) boost operation; (**b**) buck operation.

Mode 1 [t_0–t_2]: In Mode 1, Q_1 and Q_3 are in the turn-on state and Q_2 and Q_4 are in the turn-off state during the interval t_1–t_2. The current i_{Q5} is $i_{LR1} - i_{LM}$, nV_O is applied to L_M, and i_{LM} increases linearly. During this mode, resonance occurs between the primary resonant inductance L_{R1} and the primary side resonant capacitor C_{R1}, and L_M does not participate in the resonance. f_r for this mode is given by Equation (4). Meanwhile, during the interval t_0–t_1, ZVS is achieved on the primary side.

$$f_r = \frac{1}{2\pi\sqrt{L_{R1}C_{R1}}} \tag{4}$$

Mode 2 [t_2–t_3]: In Mode 2, Q_1 and Q_3 are in the turn-on state and Q_2 and Q_4 are in the turn-off state. The current i_{LR1} is equivalent to i_{LM}, and V_{LM} is given by $V_S - V_{CR1}$. During this mode, resonance occurs due to L_{R1}, L_M and C_{R1}. The resonant frequency in Mode 2 of the boost operation $f_{r,boost}$ is derived by Equation (5). Within this interval, the slope of V_{LR2} and V_{CR2} is zero due to i_2, which corresponds to $i_{Q5,6,7,8}$.

$$f_{r,boost} = \frac{1}{2\pi\sqrt{(L_{R1} + L_M)C_{R1}}} \tag{5}$$

Mode 3 [t_3–t_5] is omitted because it is symmetric to that in Mode 1.

The key waveforms in the buck operation of CLLC are shown in Figure 4b. In this operation, the switching frequency f_s is higher than f_r ($f_s < f_r$: above region).

Mode 1 [t_0–t_2]: this mode is identical to Mode 1 of the boost operation.

Mode 2 [t_2–t_3]: In Mode 2, Q_1, Q_2, Q_3 and Q_4 are in the turn-off state. V_{AB} is switching from V_S to $-V_S$, resulting in V_{LM} being zero. Therefore, V_{CD}, which is $V_{LR2} + V_{CR2}$, equals V_O. During this mode, resonance occurs between L_{R1} and $4C_{oss}$, and L_M does not participate in the resonance. The resonant frequency in Mode 2 of buck operation $f_{r,buckt}$ is derived by Equation (6).

$$f_{r,buck} = \frac{1}{2\pi\sqrt{L_{R1}4C_{oss}}} \tag{6}$$

Mode 3 [t_3–t_4]: in Mode 3, Q_2 and Q_4 are in the turn-on state. Q_1 and Q_3 are in the turn-off state. As shown in Figure 4b, because i_{LR1} is greater than i_{LM}, i_2 flows through Q_5 and Q_7.

Mode 4 [t_4–t_6] is omitted because it is symmetric to that in Mode 1.

The gain M of the CLLC can be derived through an equivalent circuit which is shown in Figure 5 [30]. M can be derived as follows:

$$\begin{aligned} M = \left|\frac{V_O}{V_S}\right| &= \left|\frac{1}{n}\cdot\frac{Z_1}{sL_{R1}+1/sC_{R1}+Z_1}\cdot\frac{R_{ac}}{Z_2}\right| \\ &= \frac{1}{n}\cdot\frac{1}{\sqrt{\alpha^2+\beta^2}} \end{aligned} \tag{7}$$

where

$$\alpha = \frac{1}{K}\left\{K+1-\left(\frac{f_r}{f_s}\right)^2\right\} \tag{8}$$

$$\beta = Q\cdot\left\{2\cdot\frac{f_s}{f_r} - 2\cdot\frac{f_r}{f_s} + \frac{1}{K}\cdot\left(\frac{f_r}{f_s}\right)^3 + \frac{1}{K}\cdot\frac{f_s}{f_r} - \frac{2}{K}\cdot\frac{f_r}{f_s}\right\} \tag{9}$$

$$\begin{aligned} Z_1 = sL_M//\left(sL_{R2}+\frac{1}{sC_{R2}}+R_{ac}\right),\ Z_2 = sL_{R2}+\frac{1}{sC_{R2}}+R_{ac} \\ K = \frac{L_M}{L_{R1}},\ Q = \frac{1}{R_{ac}}\cdot\sqrt{\frac{L_{R1}}{C_{R1}}},\ f_r = \frac{1}{2\pi\sqrt{L_{R1}C_{R1}}} \end{aligned} \tag{10}$$

where Q is the quality factor and K is the inductance ratio. The ac-equivalent load resistance R_{ac} using the first harmonic approximation (FHA) [30,31] can be calculated as

$$R_{ac} = \frac{V_{O,FHA}}{I_{O,FHA}} = \frac{\frac{2\sqrt{2}}{\pi}\cdot nV_O}{\frac{\pi}{2\sqrt{2}}\cdot\frac{I_O}{n}} = \frac{8n^2}{\pi^2}R_O \tag{11}$$

where $V_{O,FHA}$ is the RMS value of V_O, which is the output voltage of the resonant network. $I_{O,FHA}$ is the RMS value of I_O, which is the output current of the resonant network.

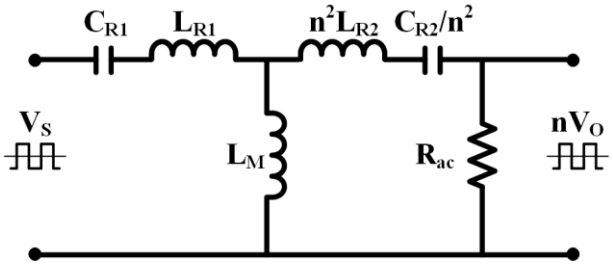


Figure 5. Equivalent circuit of CLLC in charging mode.

As in DAB, the CLLC in buck operation must achieve ZVS during the turn-off state, as specified in Equation (3). In Equation (3), L_{eq} is calculated as L_{R1}. Meanwhile, in the boost operation, soft switching is ensured [30] because the switching frequency f_s is lower than the resonant frequency f_r, and the dead time t_{dead} can be derived as

$$t_{dead} \geq 16C_{oss}\cdot f_s\cdot L_M \tag{12}$$

2.3. Comparison in Operation Principle

The comparison between the DAB and CLLCs is specified in Table 1. A DAB has a few components and is low in design complexity. Since the DAB gain has the same ratio as the load as in Equation (2), it is easy to regulate the gain. However, the slight phase shift makes soft switching difficult under light load conditions. Therefore, modulation strategies such as dual phase shift (DPS) and triple phase shift (TPS) have been proposed for soft switching under full load conditions [32–35]. This article has adopted the traditional modulation method, a single phase shift (SPS), to focus on the conventional DAB topology. In contrast, the CLLC requires more components than the DAB. The design complexity of the CLLC is higher than that of the DAB because the gain of the CLLC depends on the Q and K factors [30]. Modulation of CLLC is frequency control and soft switching is achievable under full load conditions [13,36,37]. Furthermore, the CLLC maintains an ideal secondary side switching boundary, resulting in higher efficiency than the DAB. Meanwhile, the typical modulation strategy of the CLLC is synchronization rectification (SR) driving [36–40]. Reference [37] proposes a dual-active-synchronization (DAS) modulation strategy to address current distortion. However, as mentioned above, this article focuses on the comparison between conventional DAB and CLLC; thus, typical SR driving is applied. The SR driving in this article is shown in Figure 6. In the below region, the secondary side switch synchronizes with the turn-on of the primary side switch and turns off earlier than the primary side. In the above region, the secondary side switch synchronizes with the turn-off of the primary side switch. To minimize the conduction loss of the body diode of the secondary side switch, it should be timed to coincide with the zero-crossing moment of the secondary current. However, as this is another research topic [39,40], this article adopts a simplified SR driving that allows for the interval of the secondary side body diode turn-on. As mentioned, this article adopts the simple and typical bi-directional topologies and control method. A more advanced control method could reduce the secondary side switch losses in the CLLC.

Table 1. Comparison of DAB and CLLC.

Item	DAB	CLLC
Number of components	A few	A lot
Design complexity	Low	High
Soft-switching range	Limited	Full
Modulation control	Phase shift	Frequency

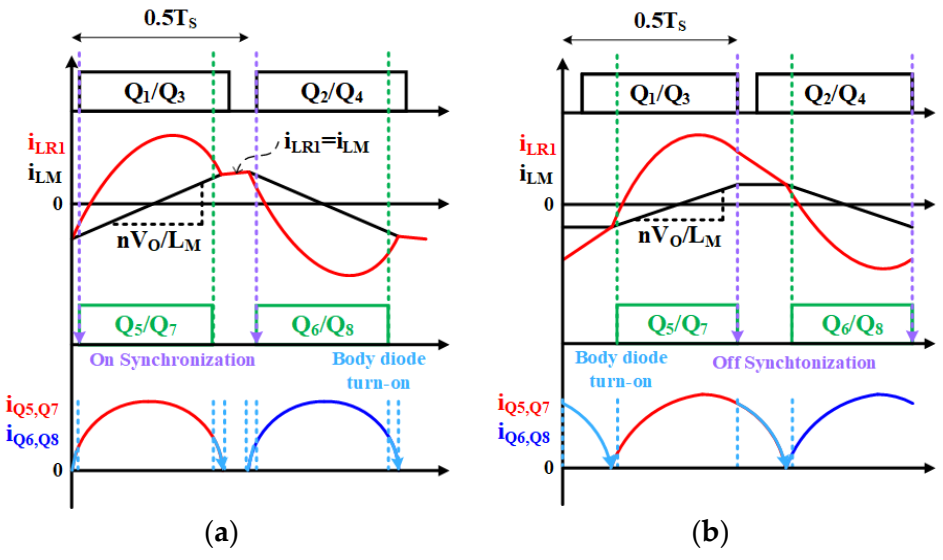


Figure 6. Modulation method in CLLC convert: (**a**) in below region; (**b**) in above region.

3. Design Considerations

3.1. Design Direction—Design Parameters

A simple configuration of the system and the battery specifications are illustrated in Figure 7. It consists of a one-phase PFC, a DC-DC converter, and a battery. Since the main purpose of this article is to the DC-DC stage, the design process started with the output of the PFC stage. The specification of battery is shown in the blue box of Figure 7. Also, the overall specifications and target of the OBC system are detailed in Table 2. If the DC-DC stage operates with only one module in the 400 V-class battery system, it can generate a high RMS current which can damage the FETs. To avoid damaging the FETs, the DC-DC stage consists of two parallel modules, as shown in the red dash box of Figure 7. This configuration is essential because conduction loss is proportional to the square of the current. Also, the feature of this article is that both topologies use the transformer's leakage inductance without additional inductors. On the other hand, the switching loss is limited to 24 W, which is a value that considers a margin of 1/20 of the power dissipation P_D at 100 °C of GS66516B (Infineon, Munich, Germany).

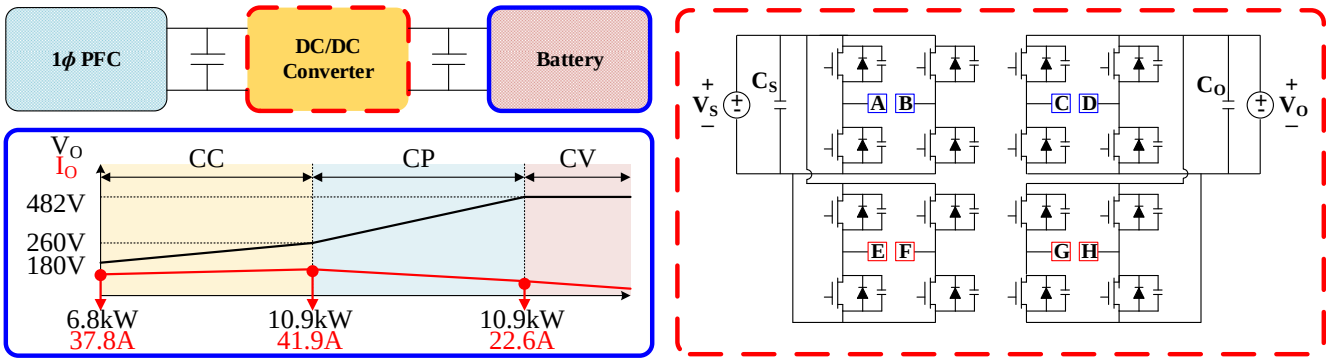


Figure 7. Simple configuration of OBC DC-DC stage.

Table 2. System specifications and targets of OBC.

Parameter	Value	Unit	Note
Rated Power P_O	10.9	kW	-
Input Voltage Range V_S	450~520	V_{dc}	-
Output Voltage Range V_O	180~482	V_{dc}	-
Maximum Output Current I_O	41.9	A_{rms}	-
Charging Method	CC-CV	-	-
Target Efficiency	97.5	%	@Vo = 340 V
Product of GaNFET	GS66516B	-	-
Target Power Density	5.5	kW/L	Except for PFC

The DAB and CLLCs are designed based on Table 2. Before proceeding with the design of each topology, it is essential to understand the design direction of each converter. The design parameters of the DAB can be selected as n, L_{eq}, f_s, and the D_{DAB} is based on Equation (1). Figure 8 shows the i_{Leq} curve obtained by regulating the design parameters. To confirm the change in the curve, the condition should be selected where D_{DAB} is the greatest. It is the endpoint of the constant current (CC) region which is V_S = 450 V and V_O = 260 V, as shown in Figure 7. The reference design parameters in Figure 8 are as follows: n is 1, L_{eq} is 9.6 µH, and f_s is 250 kHz. The characteristics are analyzed when n increased or when L_{eq} or f_s decreased relative to the reference, and the analysis for each case is presented in Table 3. The ZVS of the secondary side switches tends to be unachieved when the n is increasing, L_{eq} is decreasing, or f_s is decreasing. To identify the optimal design parameters, each of the three design parameters were individually increased or decreased to find the appropriate design point. When designing the D_{DAB} range from

0.1 to 0.4 with a margin of less than 0.5, it is necessary to design a ZVS that satisfies all switches to minimize the loss. Therefore, the optimal design parameter of the DAB is selected as the reference value when considering the input/output range, D_{DAB} range, and ZVS achievement.

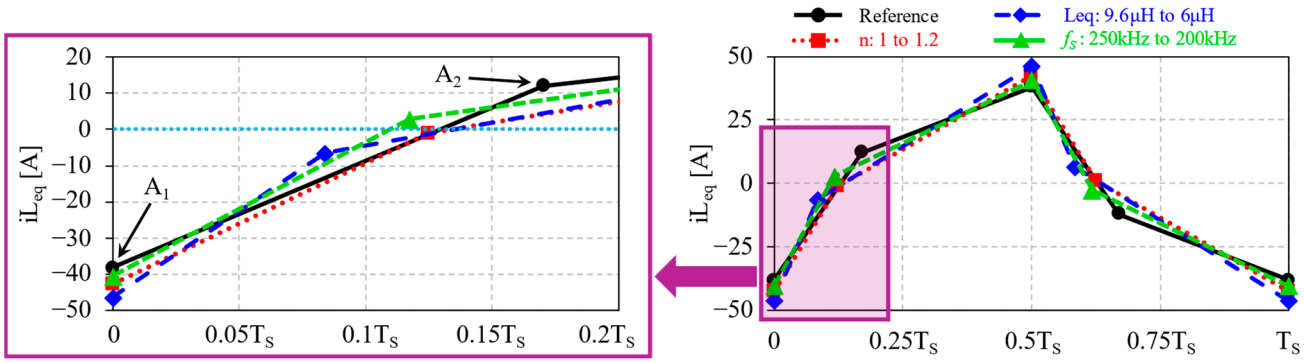


Figure 8. Regulating design parameters in DAB.

Table 3. Value of regulating design parameters in DAB.

Item	D_{DAB}	Primary Side RMS in FETs	Secondary Side RMS in FETs	ZVS Achievement Of Secondary Side
$n \uparrow$	Decrease	Increase	Decrease	Toward bad
$L_{eq} \downarrow$	Decrease	Decrease	Decrease	Toward bad
$f_s \downarrow$	Decrease	Decrease	Decrease	Toward bad

The design parameters of the CLLC may be selected as n, f_s, the resonant frequency f_r, the magnetizing inductance L_M, the primary leakage inductance L_{R1}, the inductance ratio K, the quality factor Q, and the ac-equivalent load resistance R_{ac} based on Equations (7)–(11). In this case, the design parameters in the resonant tank, such as L_R and C_R, can be derived as

$$\begin{cases} L_R = L_{R1} = n^2 L_{R2} \\ C_R = C_{R1} = C_{R2}/n^2 \end{cases} \quad (13)$$

Due to the large number of design parameters, it is important to identify the direction of the design. Therefore, the design direction was confirmed by regulating the design parameters of the CLLC as shown in Table 4 and Figure 9. The reference design parameter in Figure 9a is as follows: n is 1.2, L_M is 35 μH, L_R is 7.7 μH, C_R is 82 nF, and f_r = 250 kHz. If n is set to 1, the CLLC will operate in the buck operation, which causes increasing switching loss by using a high switching frequency. Therefore, n in this paragraph is set to 1.2—a number greater than 1 for design direction. Figure 9a is a reference gain curve. Additionally, the different two gain slopes indicate the inductive and capacitive regions, with ZVS achievement in the inductive region [30]. Therefore, the design direction should aim at the inductive region. Figure 9b shows the case where n and K are constant, but L_R and L_M increase at once. In (b), the slope increases in the below region compared to (a) and decreases in the above region. This means Q becomes high. The increased L_M leads to reduced $i_{LM,Max}$, thus decreasing switch turn-off loss in the below region. Figure 9c shows the effects of increasing L_R while keeping n and L_M constant. C_R is reduced to maintain f_r, resulting in increased V_{CR}, and the capacitive region becomes wider, complicating the selection of a design point. Figure 9d shows increasing L_M while keeping n and L_R constant. In this case, the slope increases in both the below and above regions. Like (b), this leads to reduced turn-off loss. Figure 9e shows increasing only n while keeping other design parameters. In (e), Q becomes low as n increases. This means the required switching frequency range will be wide. In summary, the changing trend of the gain curve has been confirmed by regulating design parameters such as K and Q. In each case, the loss varies

depending on the required switching frequency range, so a design with proper design parameters is needed.

Table 4. Value of regulating design parameters in CLLC.

Item / Figure 9	n	K	L_R [μH]	L_M [μH]
(a)	1.2	4.54	7.7	35
(b)	Constant (=1.2)	Constant (=4.54)	Twice (=15.4)	Twice (=70)
(c)	Constant (=1.2)	Low (=2.27)	Twice (=15.4)	Constant (=35)
(d)	Constant (=1.2)	High (=9.09)	Constant (=7.7)	Twice (=70)
(e)	Increased (=1.4)	Constant (=4.54)	Constant (=7.7)	Constant (=35)

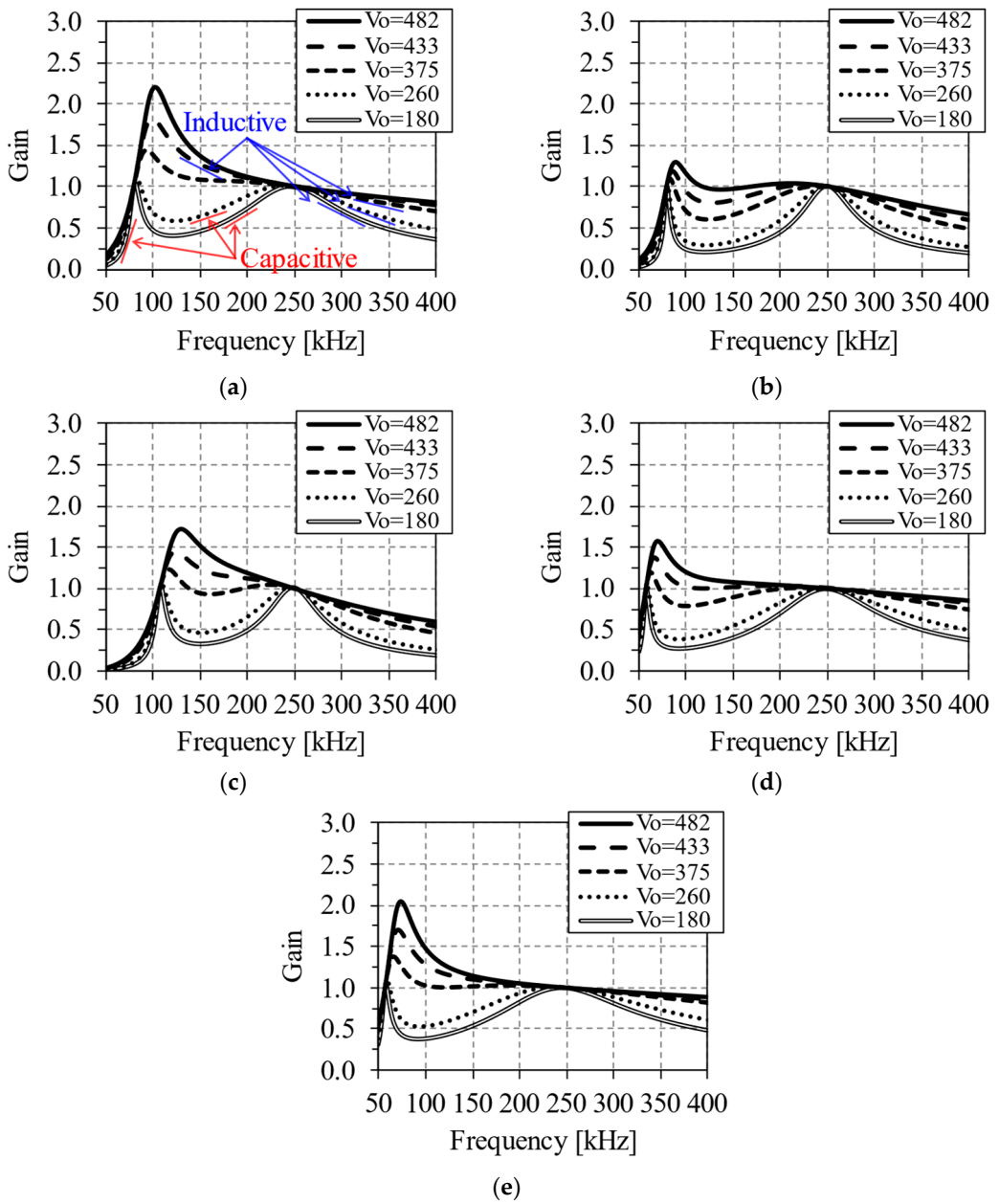


Figure 9. Regulating design parameters in CLLC: (**a**) reference gain curve; (**b**) constant n and K, increased L_R and L_M; (**c**) constant n and L_M, increased L_R; (**d**) constant n and L_R, increased L_M; (**e**) increased n and constant others.

3.2. Design Direction About Transformer

The design direction for the DC transformer (DCX) of each topology was analyzed. The DAB when the turn ratio n is 1, L_{eq} and the f_r should be selected to satisfy the required D_{DAB} range and ensure ZVS for all switches. Increasing L_{eq} and f_r can reduce switching loss. However, these factors are not only related to switching loss but also to the DCX size. To reduce the DCX size, a smaller L_{eq} and higher f_s should be chosen. However, an excessively small L_{eq} can lead to unachieved ZVS, resulting in increased switching loss. Conversely, too high f_s increases turn-off loss. This also increases the RMS current, leading to higher conduction loss in the switches, and demands a larger wire diameter in the DCX. Additionally, an overly high f_s can increase core loss. Therefore, the final DAB design parameters are presented in Table 5. These parameters are the result of analysis according to the design direction to satisfy the required power density and efficiency.

Table 5. Final design parameters of DAB.

Parameter	Value	Unit
Turn ratio n	1 (9:9)	-
Switching frequency f_s	250	kHz
Inductance L_{eq}	9.6	μH
Range of duty cycle D_{DAB}	0.318~0.125	-

Similarly, the DCX of the CLLC should be designed with the same method as the DAB. As shown in Figure 9b,d, adopting the below region can reduce switching loss, but it requires a larger DCX cross sectional area. Given the limited power density, it is not feasible to increase the core size. Therefore, it is important to select the range of the above region while satisfying the limited switching loss, which is the abovementioned 24 W. Consequently, the final CLLC design parameters and gain curve are shown in Table 6 and Figure 10. The input/output voltage range by the final design of each topology is shown in Figure 11.

Table 6. Final design parameters of CLLC.

Parameter	Value	Unit
Turn ratio n	1.2 (12:10)	-
Resonant frequency f_s	200	kHz
Magnetizing inductance L_M	35	μH
Pri. resonant inductance L_{R1}	7.5	μH
Pri. resonant capacitance C_{R1}	84	nF
Range of frequency	160~307	kHz

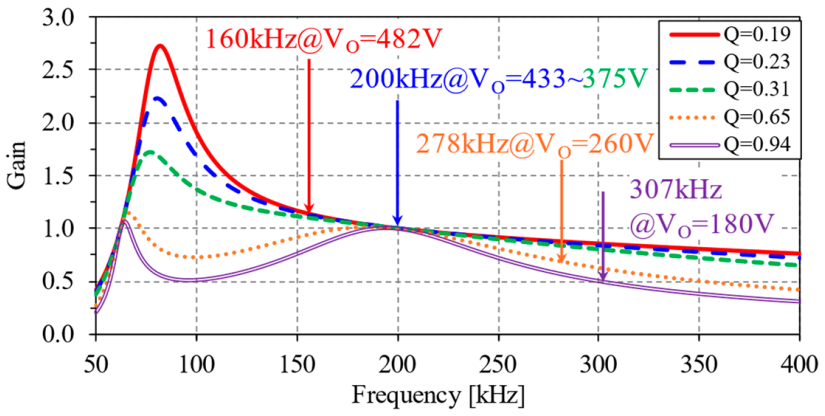
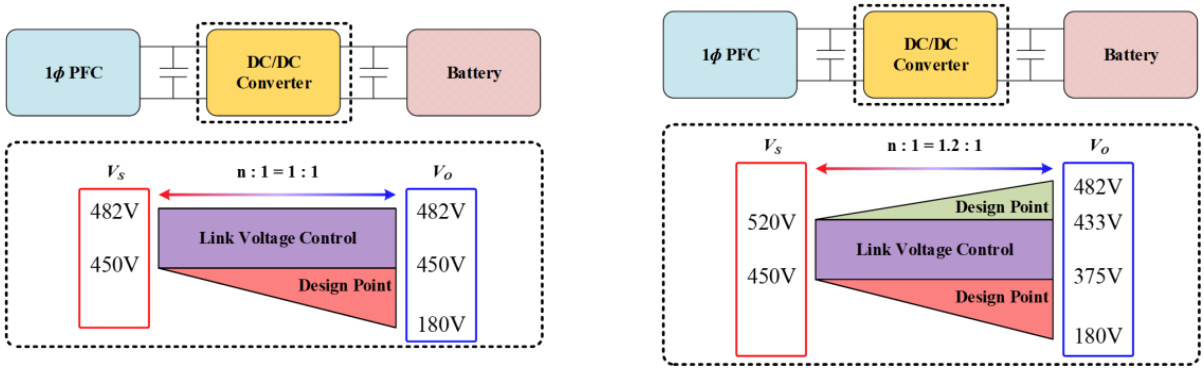


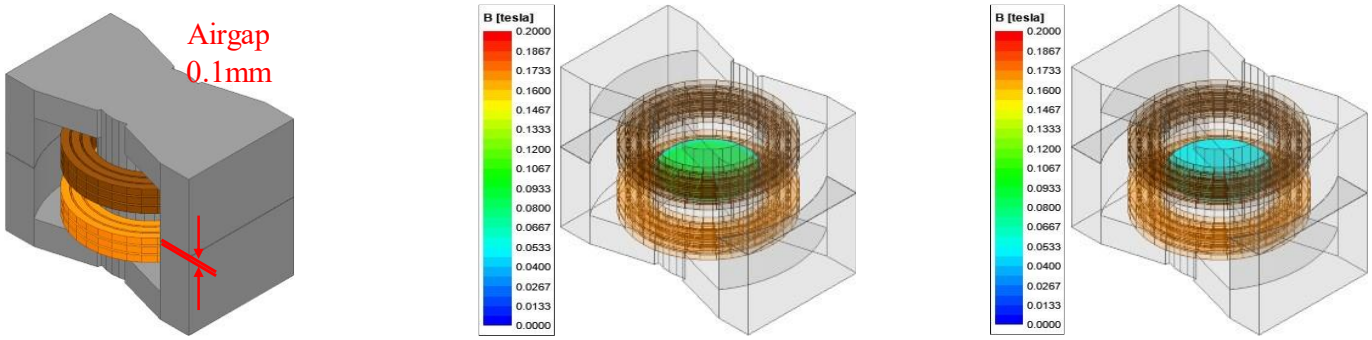
Figure 10. Gain curve of CLLC.



(**a**) (**b**)

Figure 11. Configuration of system and input/output voltage range in dotted boxes regarding each topology: (**a**) DAB; (**b**) CLLC.

Based on the previous design specifications, the DAB has adopted a separated winding structure for the DCX to utilize the leakage inductance, as shown in Figure 12a. The specifications and simulation results of the DAB-DCX are presented in Table 7. The performance of the DAB-DCX is evaluated using an FEA-based simulation tool at points where core and winding losses are at their maximum. As shown in Figure 12b,c, the maximum magnetic flux density in the cross section of the central leg is 0.089 T under the maximum flux density condition, which occurs at the maximum output voltage (V_O = 482 V), and 0.057 T under the maximum current density condition, occurring when the output voltage V_O is 260 V. The results derived from theoretical calculations and those obtained through simulation are each documented in Table 8. Additionally, simulations could provide insights into losses due to the eddy effect, which are difficult to check through calculations alone.



(**a**) (**b**) (**c**)

Figure 12. Modeling and distributions of flux density in DAB-DCX: (**a**) modeling; (**b**) flux density at V_O = 482 V; (**c**) flux density at V_O = 260 V.

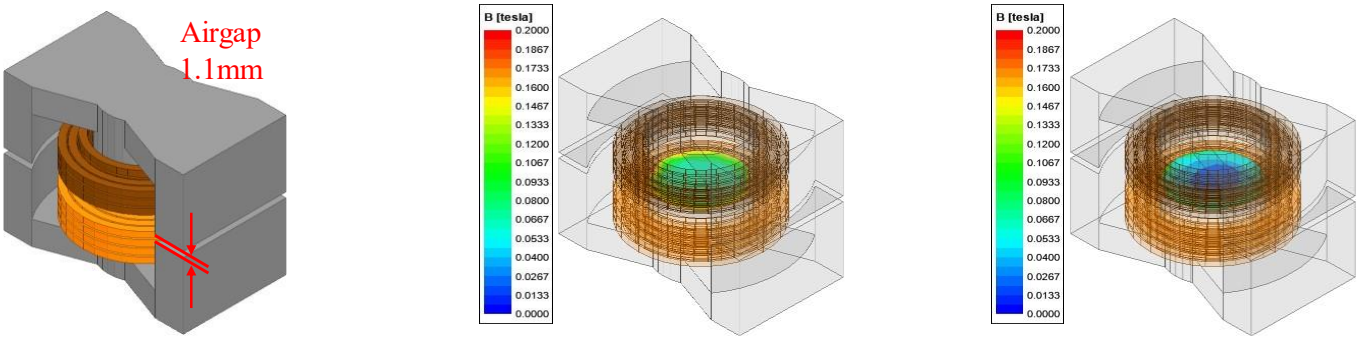
Table 7. Design specifications of DAB-DCX.

Parameter	Value	Unit
Core type	PQ6145	-
Core material	PM16	-
Area of cross section A_C	491	mm^2
Litz wire	0.04φ/3180	-
Magnetizing inductance L_M	225.7	μH
Eq. Leakage inductance L_{eq}	9.595	μH

Table 8. Results of theoretical calculations and simulations in DAB-DCX.

Parameter		Calculation	Simulation	Unit	Note.
B_{max}		0.109	0.089	T	V_O = 482 V
Core loss		7.80	7.48	W	
Winding loss	DC	1.60	1.33	W	
	Eddy	-	14.13	W	
B_{max}		0.059	0.057	T	V_O = 260 V
Core loss		1.1	1.74	W	
Winding loss	DC	5.60	5.12	W	
	Eddy	-	24.26	W	

To match the power density, the CLLC-DCX was designed using the same core as the DAB-DCX. As shown in Figure 13a, the winding structure is similar to DAB-DCX to utilize the DCX's leakage inductance. The airgap was regulated to control the magnetizing inductance. The specifications and simulation results of the CLLC-DCX are presented in Table 9. The DCX loss is confirmed under both maximum flux density and maximum current density conditions, with the flux density distribution shown in Figure 13b,c. Table 10 summarizes the flux density for each condition and compares the results from theoretical calculations and simulations in CLLC.



(**a**) (**b**) (**c**)

Figure 13. Modeling and distributions of flux density in CLLC-DCX: (**a**) modeling; (**b**) flux density at V_O = 482 V; (**c**) flux density at V_O = 260 V.

Table 9. Design specifications of CLLC-DCX.

Parameter	Value	Unit
Core type	PQ6145	-
Core material	PM16	-
Area of cross sec tion A_C	491	mm^2
Litz wire	$0.04\varphi/3180$	-
Magnetizing inductance L_M	34.63	μH
Pri. leakage inductance L_{R1}	7.71	μH
Sec. leakage inductance L_{R2}	5.19	μH

In conclusion, DAB and CLLC are designed under the same constraints, which are input/output voltage range and power density. DAB's design parameters are relatively few with n, f_s, and L_{eq}. A wide input/output range and ZVS can be satisfied through n is 1.

However, in CLLC, the design parameters are n, K, L_R, L_M, f_r, and the gain is very complicated. n is above 1 for the narrow frequency range because modulation control of CLLC is a switching frequency. Additionally, a minimum V_S = 450 V covers a wide V_O range which is from 180 V to 482 V. Moreover, by regulating the design parameters, all conditions must satisfy the inductive region to achieve ZVS for all switches. Additionally,

the f_r must be selected to ensure that the voltage stress on C_R is not high and that the size of the DCX is not excessively large. In addition, since it is disadvantageous in the switching loss caused by SR driving, an airgap was added to satisfy the L_R, L_M in the CLLC-DCX design, and the eddy loss of the winding due to the fringing effect is greater. In conclusion, from the analysis of the design, it is expected that DAB will be more efficient in the experiment than CLLC.

Table 10. Results of theoretical calculations and simulations in CLLC-DCX.

Parameter		Calculation	Simulation	Unit	Note.
B_{max}		0.154	0.147	T	V_O = 482 V
Core loss		8.84	10.06	W	
Winding loss	DC	2.75	2.55	W	
	Eddy	-	7.41	W	
B_{max}		0.051	0.066	T	V_O = 260 V
Core loss		2.5	2.58	W	
Winding loss	DC	6.61	5.49	W	
	Eddy	-	34.49	W	

4. Experimental Results

A prototype with a power density of 5.5 kW/L is manufactured. A photo of the DC-DC stage and testbed is shown in Figure 14. The input power supply used to drive the DC-DC stage is the AINUO ANEVH 4500-40(F) (Republic of Korea), and the electronic load is the PRODIGIT 34315E (Taiwan). Efficiency measurements are taken using the YOKOGAWA WT5000 (Japan). The YOKOGAWA GP10 (Japan) shows the temperature of switches. The GaNFETs were used which use GaN SYSTEMS GS66516B cooled using an insulated metal substrate (IMS) board, and each module of the power board was vertically mounted. A JOTEC HH-35 (Republic of Korea) chiller is used for cooling the GaN board. The inductance of the DCX was measured using HIOKI IM3533 (Japan). The measured inductance of the DCX and resonant capacitors is shown in Table 11. In the DAB-DCX, the magnetizing inductance is 213.5 µH, and the equivalent inductance is 9.2 µH. In the CLLC-DCX, the magnetizing inductance is 39.03 µH, and L_{R1} and L_{R2} are 5.85 µH and 6.86 µH, respectively. Therefore, the resonance frequency of the CLLC was regulated to 200 kHz by tuning the resonant capacitors, the C_{R1} was 108 nF and the C_{R2} was 92 nF. At this point, due to changes in Q and K, the switching range in the experiment differed from the designed switching range.

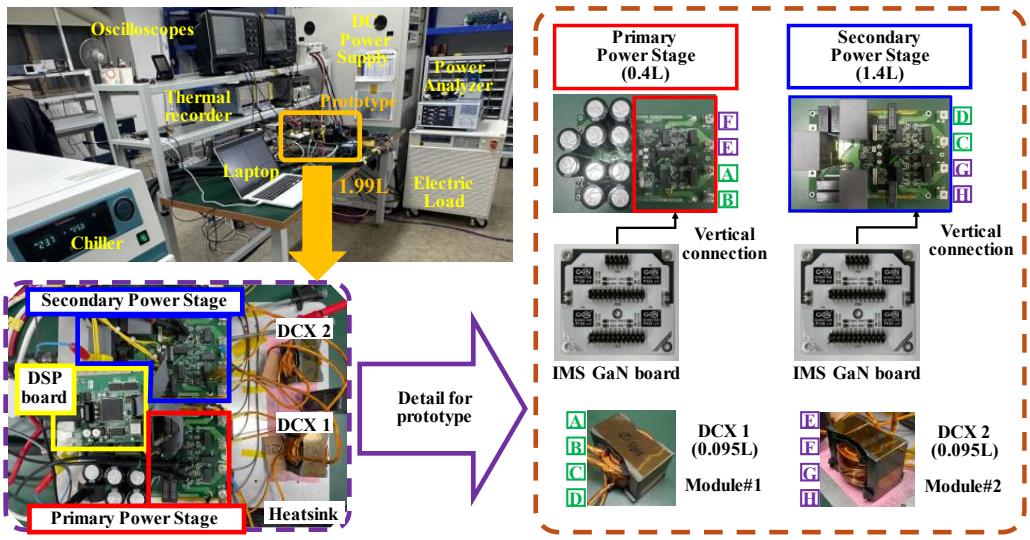


Figure 14. A photo of testbed.

Table 11. Prototype of specifications for each converter.

Parameter	Value	Unit	Note
Core type	PQ6145	-	-
Core material	PM16	-	-
Area of cross sec tion A_C	491	mm^2	-
Litz wire	$0.04\varphi/3180$	-	-
Magnetizing inductance L_M	213.5	μH	In DAB
Equivalent Inductance L_{eq}	9.2	μH	In DAB
Magnetizing inductance L_M	39.03	μH	In CLLC
Pri. resonant inductance L_{R1}	5.85	μH	In CLLC
Sec. resonant inductance L_{R2}	6.86	μH	In CLLC
Pri. resonant capacitance C_{R1}	108	nF	In CLLC
Sec. resonant capacitance C_{R2}	92	nF	In CLLC

To compare DAB and CLLC, experimental conditions with 400 V-battery specification are selected, as shown in Figure 15. The two reasons for selecting these conditions are as below. First, we compare each topology under the conditions of the minimum battery voltage (condition A), maximum current density (condition B), and flux density (condition D). Condition C is a nominal condition because it needs to be checked because it is in the middle of the CP. Second, this article proposes the OCB DC-DC stage for the 400 V-battery system. The abovementioned battery specification is produced by Hyundai, Tesla, Volkswagen, etc.

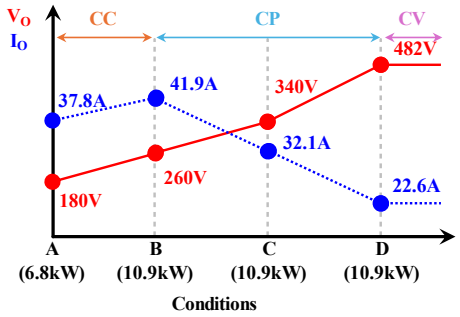


Figure 15. Experimental cases under 100% load condition.

Figure 16 illustrates the key waveforms under each condition for each topology under 100% load. In condition A, ZVS on the secondary side of the DAB is not achieved, as shown in Figure 16. The highlighted section in Figure 16a shows the gate-source and drain-source voltages of the secondary side. This occurred because the inductance of the DAB-DCX prototype is smaller than the designed value 9.6 μH, reducing the D_{DAB}. As verified in Section 2, even though $i_L(t_2)$ has a positive value, it does not satisfy Equation (3). On the other hand, the ZVS achievement under other conditions can be confirmed in Figure 17.

Figure 18 shows the key waveforms under each condition for CLLC under the 100% load condition. Figure 18a–c operate in the above region, where the turn-off current is large, enabling ZVS. On the secondary side, soft switching is possible because the body diode of the secondary side switch states turn-on. On the other hand, (d) operates in the below region. This waveform can be analyzed in relation to Section 2. In the below region, i_{LR1} and i_{LM} converge, making the turn-off current equal to i_{LM}. Based on the measured magnetizing inductance and switching frequency, the maximum value of i_{LM} is calculated to be about 22 A. The measurement points are changed to review this, as shown in Figure 19. Since sufficient energy is available to achieve ZVS, the ZVS of the primary side switch can be confirmed, as shown in Figure 19. The secondary side switch is synchronized with the turn-on of the primary side switch. The gate-to-source threshold $V_{gs(th)}$ of the GS66516B is 1.7 V, indicated by the dashed arrow in Figure 19. At this point, V_{CD} had reached 97% of the output voltage (482 V), meaning that the drain-to-source voltage of Q_6 and Q_8 had charged,

allowing Q_7 to achieve almost ZVS. Meanwhile, oscillation occurs when the secondary side gate is turned off. This is caused by the resonant inductor and the parasitic capacitance of the secondary side switches [40].

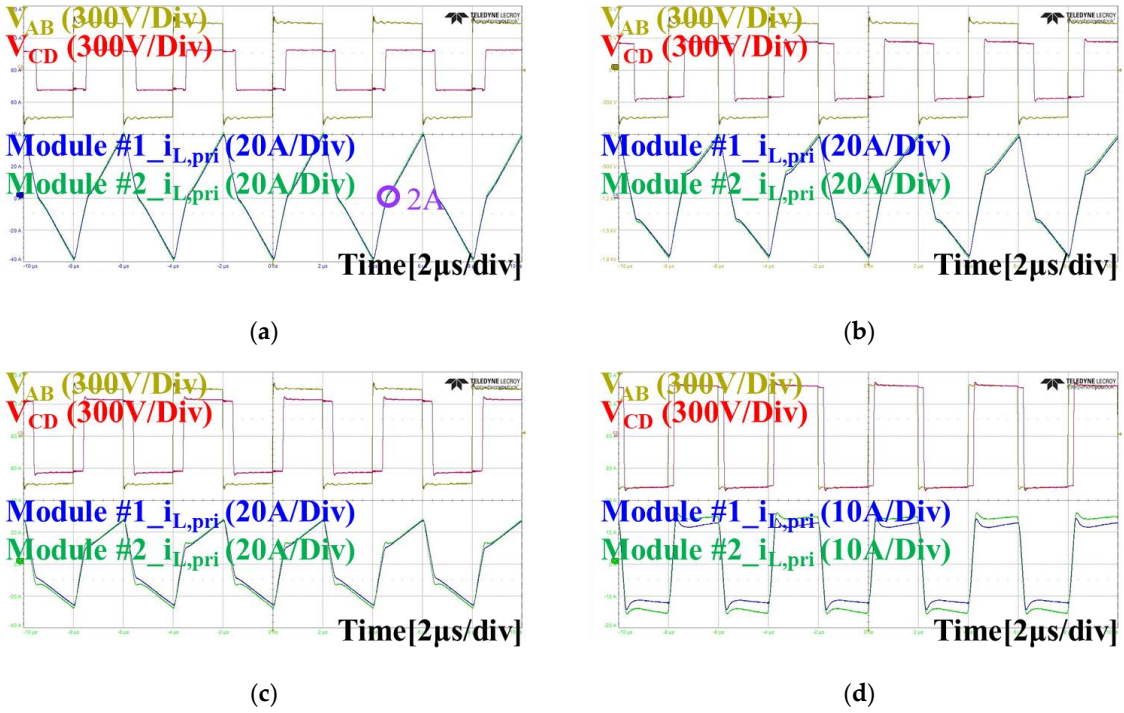


Figure 16. Operational key waveforms in DAB: (**a**) condition A at 39.24°; (**b**) condition B at 58.32°; (**c**) condition C at 36.72°; (**d**) condition D at 21.24°.

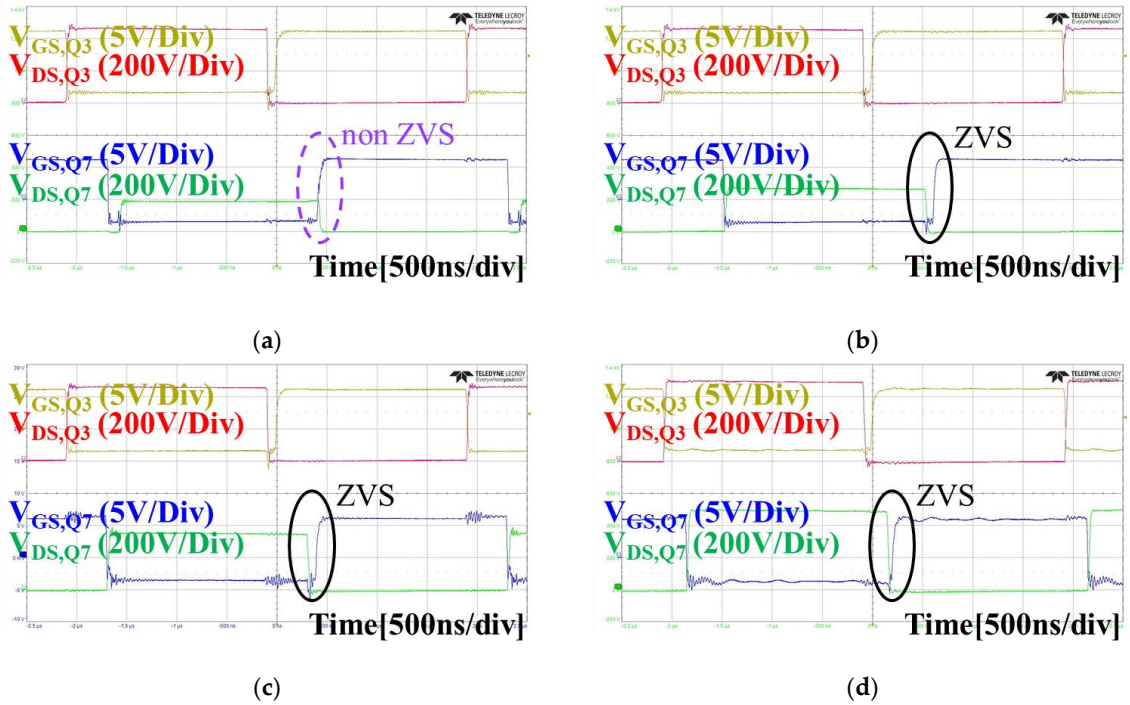


Figure 17. Operational key waveforms regarding ZVS achievement in DAB: (**a**) condition A; (**b**) condition B; (**c**) condition C; (**d**) condition D.

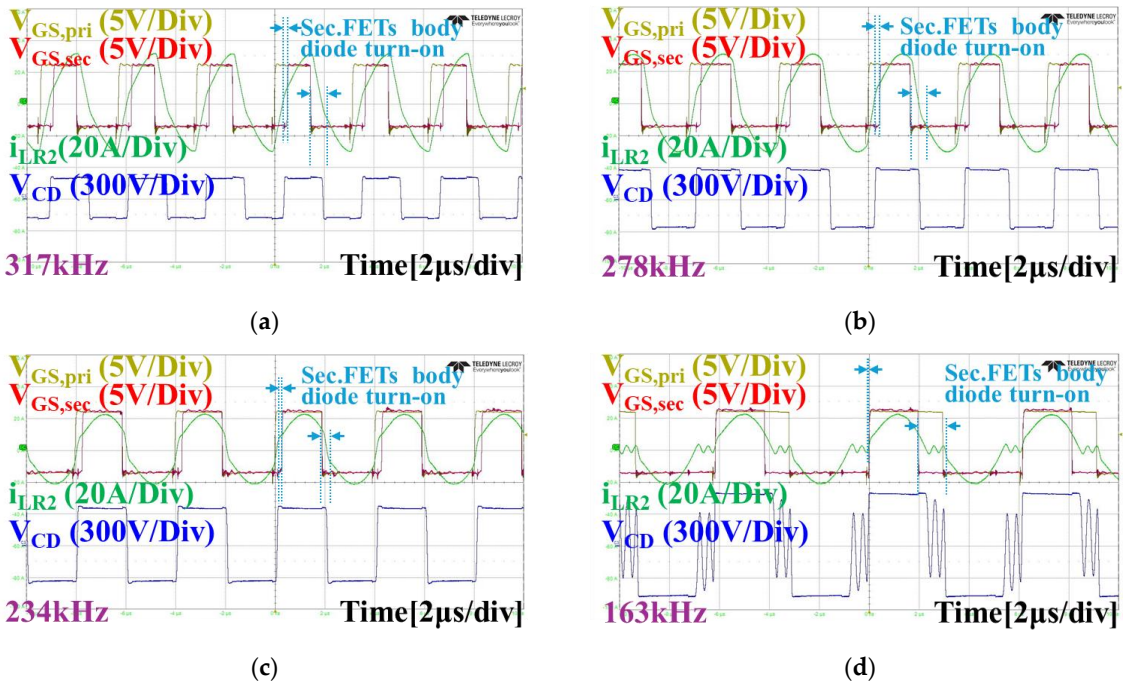


Figure 18. Operational key waveforms in CLLC: (**a**) condition A at 317 kHz; (**b**) condition at 278 kHz (**c**) condition C at 234 kHz; (**d**) condition D of CLLC at 163 kHz.

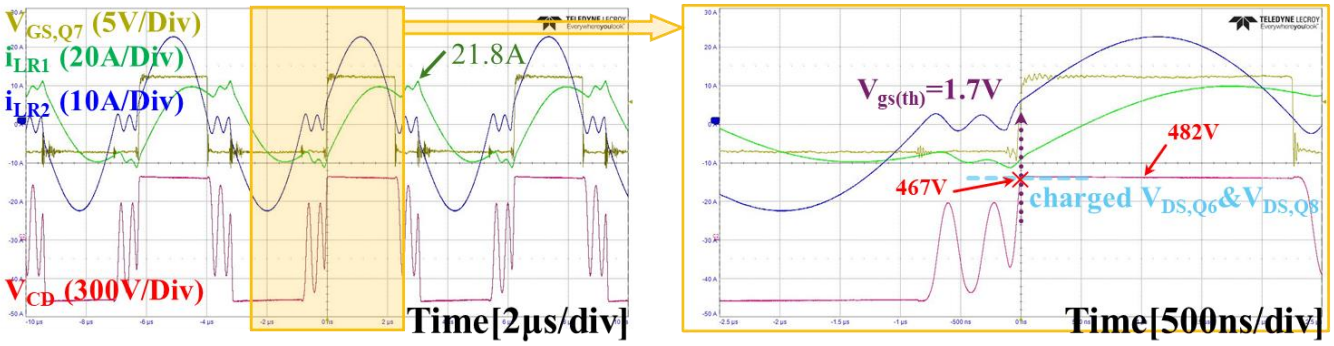


Figure 19. Operational key waveform at condition D in CLLC.

Figure 20 presents the efficiency graphs corresponding to each condition. Figure 21 shows the experimental efficiency under various load conditions. Additionally, Figure 22 shows the actual measurement efficiency of each topology at condition D. The load conditions are selected from 50% to 100% to observe the variation trend under light load. Overall, the DAB shows higher efficiency under 100% load. However, under light load, the CLLC has higher efficiency. The analysis of experimental results is presented in Section 5.

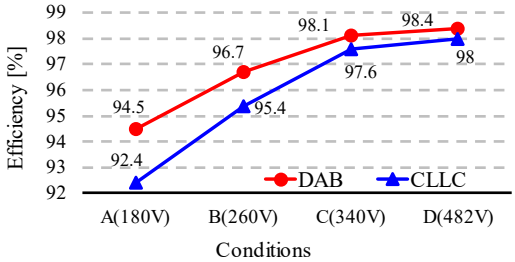


Figure 20. Efficiency by conditions and each topology under 100% load.

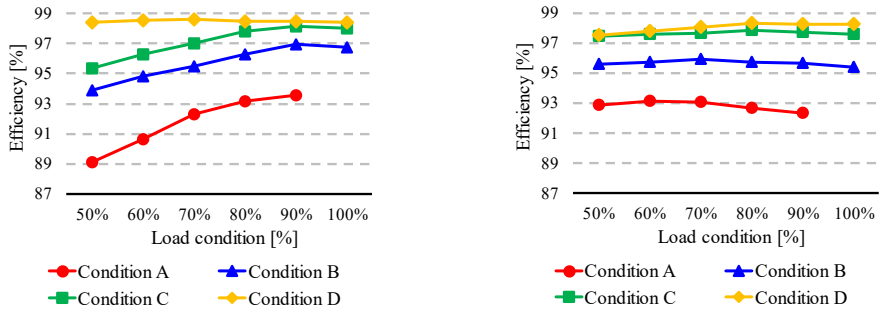


Figure 21. Efficiency of each topology by conditions and load conditions: (**a**) DAB; (**b**) CLLC.

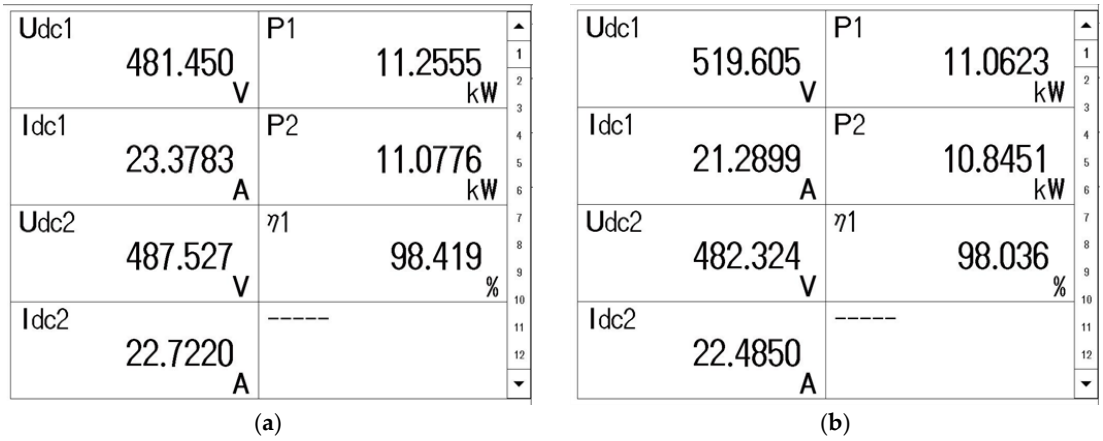


Figure 22. Efficiency at condition D using WT5000 under 100% load: (**a**) DAB; (**b**) CLLC.

5. Analysis of Experimental Results

5.1. Switch Loss

The blue dashed line in Figure 18 is the turn-on state of the secondary switches' body diode. It should be the conduction loss of the body diode. Therefore, the secondary side switches will have a higher switching loss. This loss is related to the heat. Figure 23 shows the maximum temperature of each side switch by each topology.

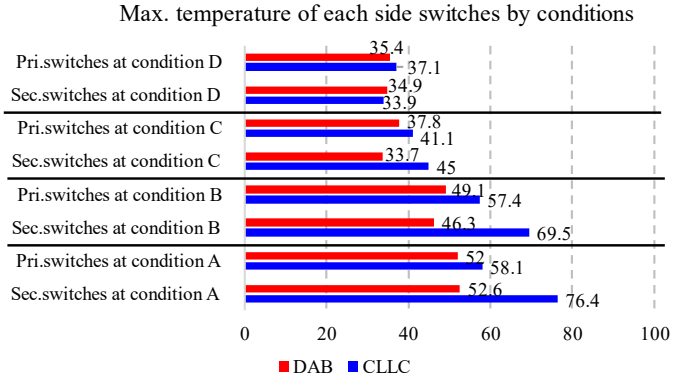
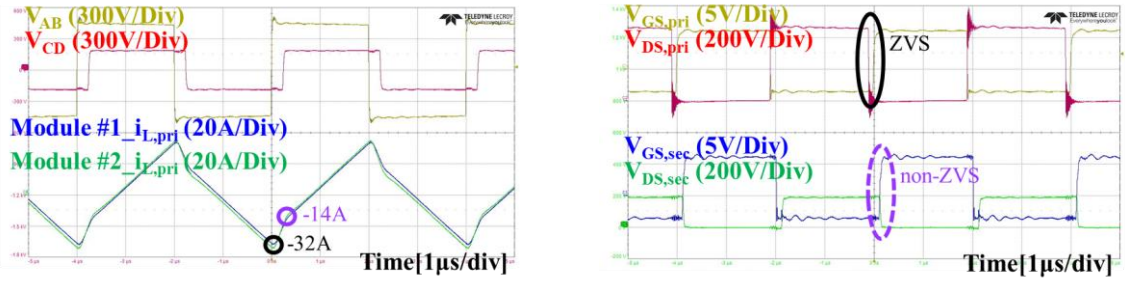


Figure 23. Maximum temperature of switches under 100%.

The CLLC, which is a resonant topology, has high current RMS value, so it has a higher temperature than the DAB. Meanwhile, ZVS was not achieved for the secondary side switches in condition A in the DAB because the equivalent inductance of the DAB-DCX prototype is smaller than the designed inductance. Nevertheless, the switch temperature of the DAB is lower. The switch temperature of CLLC is higher because the conduction loss

by the high-current RMS and body diode is larger than the turn-on loss. However, under light load conditions, the CLLC has a higher efficiency. As shown in Figure 24, the DAB does not achieve ZVS under light load conditions, resulting in increased turn-on loss for the secondary side switches. Meanwhile, the CLLC satisfies ZVS under light load conditions, resulting in lower losses.



(**a**) (**b**)

Figure 24. Operational key waveforms under 50% load in DAB: (**a**) voltage and current waveform of DAB-DCX; (**b**) gate-source and drain-source voltage of each side.

5.2. DCX Loss

CLLC-DCX causes a more significant winding loss due to the fringing effect caused by the airgap of 1.1 mm. This airgap is to satisfy the magnetizing and leakage inductance requirements. In contrast, the winding loss of the DAB-DCX is low because of the smaller airgap than the CLLC-DCX. In short, the larger airgap causes more winding eddy loss in CLLC-DCX. Therefore, the loss is related to the heat, and Figure 25 shows the maximum temperature of DCX. The temperature is measured by FLIR E54 (OR-U.S.), which is a thermal imaging camera. The measurement points of temperature are the top of the core and the surface of the winding. Under conditions of high current density, the winding temperature increases, and with higher flux density, it can be observed that the core temperature tends to rise as well.

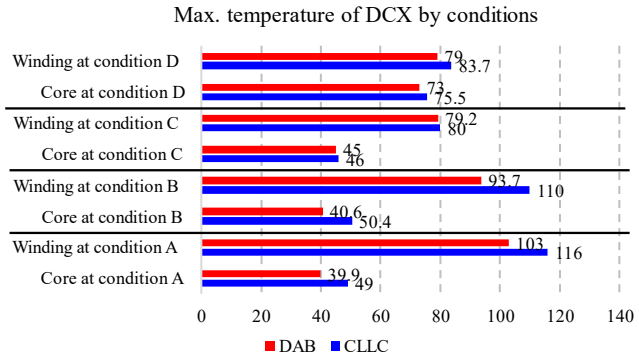


Figure 25. Maximum temperature of DCX under 100%.

5.3. Differences in Control and Comprehensive Analysis

The DAB has phase shift modulation, but the CLLC has frequency modulation and secondary side SR driving. SR driving is more complex than phase shift control. If an ideal and advanced SR driving method was applied, the secondary side switch losses would be nearly zero. However, as mentioned above in Section 2, since the most typical control for bi-directional topologies is used, the efficiency of the CLLC is lower at 100% load, when the output current is large. This raises the temperature of the secondary side switches in the CLLC. On the other hand, the efficiency of the CLLC at a light load is higher than that of the DAB because CLLC can achieve ZVS over a wide range of load conditions. The secondary side of the DAB does not achieve ZVS at light load.

As a result, the CLLC can theoretically achieve higher efficiency. However, the increase in switch losses due to SR driving or the eddy loss of the windings in the design of the DCX can decrease efficiency. In V2G, CLLC-DCX can equally act as a factor for the increase in losses. If there were no similar constraints, CLLC-DCX could be improved to increase the overall efficiency of CLLC. The DAB can achieve high efficiency with simple design and modulation. However, typical SPS methods cause low efficiency under light loads. If other modulation strategies are adopted, the efficiency of the light load conditions can be improved. Also, this is the same for the V2G of the DAB. In summary, selecting the design direction and modulation strategy is important, as system specifications such as input/output voltage and design parameters influence the performance. If more advanced modulation strategies or controls are considered, different results may be obtained.

6. Conclusions

This article compares high-efficiency, high-density DAB and CLLC for electric vehicles (EVs). Theoretical analyses of the two topologies are conducted to compare design variables, design complexity, soft-switching range, and modulation control methods. Design directions are proposed under the same design constraints, and design parameters are selected according to each topology's design direction. The DCX of each topology is designed using an FEA-based simulation tool. Through simulations, the airgap of CLLC results in higher eddy current loss in the wires compared to the DAB-DCX. The loss of each topology was analyzed according to the components of the converter in relation to heat. In addition, the difference between the design and the experiment was identified and it was identified. Analyzing the experimental results can contribute to the selection of topology, design direction, and transformer design. Both topologies meet the target efficiency of 97.5%. However, depending on constraints and design directions, the DAB can be more efficient than CLLC. Additionally, CLLC has a higher efficiency in light loads because the DAB cannot achieve ZVS using a typical modulation strategy. In short, the DAB and CLLC are designed under the same design constraints: a power density of 5.5 kW/L, a wide input/output range, and a high output of 10.9 kW. In conclusion, when a typical bidirectional topology is designed as an 11 kW/400 V system under the same constraints, the DAB shows excellent performance at 100% load, but the efficiency decreases due to non-ZVS under light load. On the other hand, CLLC is generally excellent in all conditions. Therefore, the DAB can increase efficiency under light loads by improving the modulation strategy. Meanwhile, CLLC can increase efficiency by performing additional research on SR driving. This article can contribute to the selection of a typical topology of the bidirectional OBC DC-DC stage. Future work will be on V2G-related analyses and experiments. In addition, this article adopts a 10.9 kW/400 V battery system. A similar specification (11 kW/400 V) applies to the Volkswagen ID.3 Pro S, Tesla Model 3, Kia EV6, etc. Therefore, this article will contribute to the development of various electric vehicles.

Author Contributions: Conceptualization, J.-B.L.; methodology, H.-S.O. and S.-Y.H.; software, H.-S.O. and S.-Y.H.; validation, H.-S.O. and S.-Y.H.; formal analysis, H.-S.O.; investigation, S.-Y.H.; writing—original draft preparation, H.-S.O.; writing—review and editing, J.-B.L.; visualization, H.-S.O. and J.L.; supervision, J.-B.L. and J.L.; project administration, J.-B.L.; funding acquisition, J.-B.L. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The datasets presented in this article are not readily available because the data are part of an ongoing study.

Conflicts of Interest: The authors declare no conflicts of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

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