

OPEN ACCESS

Surface-Tensile-Stress Induced Polishing-Voids Suppression via H_2O_2 Oxidizer Effect in Cross-Point Phase-Change-Memory-Cells

To cite this article: Soo-Bum Kim et al 2019 ECS J. Solid State Sci. Technol. 8 P667

View the article online for updates and enhancements.

You may also like

- <u>Study on the Mechanism of Nano-Flake</u> <u>Defect during Tungsten Contact Chemical</u> <u>Mechanical Polishing</u> Hong Jin Kim, Adam Lawyer, Bryan Egan et al.
- Impact of Wafer Geometry on CMP for Advanced Nodes Pradeep Vukkadala, Kevin T. Turner and Jaydeep K. Sinha
- Assessment of Change in Physicochemical Properties and Cellular Toxicity of Pre- and Post-CMP Silica Slurries

Slurries K. Kosaraju, S. Crawford, M. Tarannum et al.

Investigate your battery materials under defined force! The new PAT-Cell-Force, especially suitable for solid-state electrolytes!



 Battery test cell for force adjustment and measurement, 0 to 1500 Newton (0-5.9 MPa at 18mm electrode diameter)

· Additional monitoring of gas pressure and temperature

www.el-cell.com +49 (0) 40 79012 737 sales@el-cell.com





P667



Surface-Tensile-Stress Induced Polishing-Voids Suppression via H₂O₂ Oxidizer Effect in Cross-Point Phase-Change-Memory-Cells

Soo-Bum Kim,¹ Hao Cui,¹ Jong-Young Cho,¹ Eun-Bin Seo,¹ Sang-Su Yun,¹ Young-Hye Son,¹ Gi-Ppeum Jeong,¹ Jae-Young Bae,² Jin-Hyung Park,³ Sung-Goon Kang,⁴ and Jea-Gun Park ^D^{1,2}

¹Department of Electronics and Communications Engineering, Hanyang University, Seoul 133-791, Korea
²Department of Energy Engineering, Hanyang University, Seoul 133-791, Korea
³UB materials Inc, Gyeonggi-do 449-823, Korea
⁴Next-Generation Memory Academic-Industrial Collaboration Centers, Hanyang University, Seoul 133-791, Korea

The chemical-mechanical-planarization (CMP) of the Ge-doped SbTe (Ge-ST) film deposited by atomic layer deposition (ALD) is essentially necessary for 3-dimensional (3D) cross-point phase-change-memory (PCM) array, producing indispensably the surfacetensile-stress inducing polishing-voids due to the corrosion of the Ge-ST film and structural tensile stress in the confined memory-cells with \sim 20-nm-diameter. The oxidizer (i.e., H₂O₂) in a CMP slurry played an important role to suppress the generation of the polishing voids via strong chemical oxidation of Sb₂O₅ and TeO₂ of the Ge-ST film surface to avoid a corrosion process during CMP. The suppression efficiency of the polishing voids greatly depended on the H₂O₂ concentration in a ALD Ge-ST-film CMP of the confined memory-cell array; i.e., the polishing voids could disappear completely greater than a specific H₂O₂ concentration (i.e., 4wt%). © The Author(s) 2019. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0061911jss]

Manuscript submitted August 5, 2019; revised manuscript received October 15, 2019. Published October 23, 2019.

Recently, 3D cross-point memory fabricated with chalcogenidealloy based PCM-cells and chalcogenide based non-linear-selectors¹⁻⁴ has been proposed as a storage class memory having a nonvolatile memory characteristic, a fast operation speed (i.e., several hundred of ns),⁵ a good write/erase endurance cycle (i.e., $>1 \times 10^8$), and a high integration density (i.e., several Mega-bit).⁶⁻¹³ 3D cross-point memory-cells have been fabricated by using the structure of confined memory-cells to minimize reset current of PCM cells,^{7,8,11,14,15} where chalcogenide-alloy based PCM-material (i.e., Ge_xSb_yTe_z or Ge or N₂ doped SbTe etc.)^{5,16-18} is vertically stacked on chalcogenide based nonlinear-selector into confined memory-cells (i.e., holes on TiN bottom electrodes), as shown in Fig. 1a. A PCM material is filled by ALD in confined memory-cells and followed by CMP,^{19–23} as shown in Fig. 1b. We reported that the CMP of a GST material filled in confined memorycells produced surface-tensile-stress induced polishing-voids via the mechanism of the stress corrosion cracking, as shown in Figs. 1b and 1c.24 The surface-tensile-stress induced polishing-voids during the CMP of a PCM material deposited by ALD were mainly produced near the shoulder position of the confined memory-cell where a maximum tensile stress was generated because of the structure effect and the material difference between a chalcogenide-alloy and spacer (i.e., SiO₂). In particular, the reduction of the surface tensile stress at the shoulder position of the confined memory-cell, via the spacer material change from Si₃N₄ to SiO₂, suppressed the generation of polishing voids. Not only the structure of the confined memory-cell and the spacer material as well as the chemical properties of a CMP slurry are a key parameter to determine the generation of the surfacetensile-stress induced polishing-voids. In our study, we investigated the suppression effect of the H₂O₂ on the generation of the surfacetensile-stress induced polishing-voids during the CMP of the PCM material depsosited on confined memory-cells. Note the H₂O₂ as an oxidizer was added into the CMP slurry. We characterized the generation of the polishing voids as a function of the H₂O₂ concentration in a CMP slurry via the surface corrosion behavior, the surface chemical reaction by x-ray-photoelectron-spectroscopy (XPS), the chemical composition depth profile of the Ge-ST film-surface by auger-electronspectroscopy (AES), and the cross-sectional(x-) high-resolutiontransmission-electron-microscopy (x-HRTEM) image-observation at the acceleration voltage of 200KV. In particular, we observed the generation frequency and size dependency of the polishing voids on the polishing rate and the H₂O₂ concentration in a CMP slurry after the

CMP of the ALD Ge-ST film deposited on the confined memory-cell array.

Experimental

A 50-nm-thick Ge-ST films (Ge 5%, Sb 70%, and Te 25 at %) on the SiO₂-film or the confined memory-cell array (i.e., 8-inch patterned wafer) in Fig. 1a were deposited by ALD using a precursor of Ge(i- $C_4H_9)_4$, $Sb(i-C_3H_7)_3$, and $Te(i-C_3H_7)_2$ and the number of cycles of 100. In the confined memory-cell array, the diameter at the top of the SiO₂-film spacer and the shoulder of the confined memory-cell were \sim 65 nm and \sim 20 nm, respectively, and the height of the memory-cell was \sim 93 nm, as shown in Fig. 1a. The CMP slurry was made of the colloidal silica abrasives of 1 wt% (Fuso chemicals, 20 wt%) at pH 2.5, a titrant of HNO₃, a deionized water, and the H₂O₂ of 0, 1, 2, 3, 4, and 5 wt%. For analyzing the corrosion behavior at the Ge-ST film surface, the ALD Ge-ST films were dipped into the CMP slurries at 40°C for 3 min. Note that the CMP of the as-deposited Ge-ST film increases the temperature of the film surface up to $\sim 40^{\circ}$ C. The 8-inch patterned wafer fabricated with the confined memory-cell array was cut into 4×4 cm² piece wafers and were polished using a CMP polisher (Poli 300, G&P Tech. Inc.) with an industry standard CMP pad (IC 1000/ Suba IV, Dow Chemical, U.S.A). The polishing pressure was 2.5 psi and the rotation speed of the polishing head and table were 80 and 20 rpm/min, respectively.

Results and Discussion

We summarized our experiment result, as shown in Table I. First of all, the dependency of the Ge-ST-film surface corrosion on the H₂O₂ concentration was observed by the secondary-ion-microscopy (SEM) images at 5 KV after dipping the Ge-ST films into the CMP slurries at 40°C for 3 min. In the as-deposited Ge-ST-film, there was no corrosion pits at the Ge-ST film surface, resulting in the surface roughness of \sim 3.1 nm at 5 um \times 5 um scanning area using atomic-force-microscopy (AFM), as shown in Fig. 2a. However, although the Ge-ST film was just dipped in the CMP slurry without H₂O₂, a high number of the corrosion pits with a large size (i.1., $50 \sim 200$ nm) were produced on the Ge-ST film surface, inducing the surface roughness of ~ 10.4 nm, as shown in Fig. 2b. In addition, when the Ge-ST film was dipped at the CMP slurry with the H₂O₂ concentration of 3 wt%, the size of the corrosion pits was remarkably reduced, i.e., ~50 nm, decreasing the surface roughness up to \sim 6.7 nm, as shown in Fig. 2c. Furthermore, when the Ge-ST film was dipped at the CMP slurry with the H₂O₂ concentration



Figure 1. x-HRTEM image of the PCM-cell array after the ALD deposition of the Ge-ST film (a) before CMP, (b) after CMP using a slurry without an oxidizer, and (c) top-view SEM image of the PCM-cell array after the CMP using a slurry without an oxidizer.

of 5 wt%, the size of the corrosion pits was greatly reduced, i.e., less than \sim 50nm, decreasing the surface roughness further up to \sim 4.3 nm, as shown in Fig. 2d. These result indicates that the Ge-ST would be etched easily in the CMP slurry without H2O2 via corrosion and the addition of the H₂O₂ in the CMP slurry would passivate the Ge-ST film surface via chemical oxidation. To confirm the corrosion or chemical oxidation, x-HRTEM images were observed as a function of the H₂O₂ concentration. The thickness of the as-deposited Ge-ST film was \sim 55.5 nm and the film surface was almost flat, as shown in Fig. 3a. However, the thickness of the Ge-ST film dipped in the CMP slurry without H2O2 was ~24 nm, etching ~21.5-nm-thick Ge-ST film via a corrosion process and resulting in a higher etched surface and a higher number of the surface corrosion pits, as shown in Figs. 2b and 3b. Otherwise, the thickness of the Ge-ST film dipped in the CMP slurry with the H_2O_2 concentration of 3 wt% was ~52.0 nm, chemically oxidizing the film surface, slightly etching the 3.5-nm-thick Ge-ST film, and greatly reducing the corrosion-pits on the film surface, as shown in Figs. 2c and 3c. In addition, the Ge-ST film thickness dipped in with the H_2O_2 concentration of 5 wt% was ~55.3 nm, indicating that the film surface was completely oxidized with the chemically oxidized film-surface of ~6.3nm. This result prevented almost the film surface corrosion and reduced extremely the film surface roughness, as shown in Figs. 2d and 3d. The correlation between the film-surface SEM images and the film x-TEM images, depending on the H_2O_2 concentration, obviously demonstrated that a CMP slurry including the H₂O₂ during CMP could chemically oxidize the Ge-ST film surface and prevent the film surface corrosion via forming chemically the

Table I. Summary of experiment result.

oxidized surface-passivation-layer. As a result, during the CMP of the ALD Ge-ST-film deposited on the confined memory-cell array, the generation of the surface-tensile-stress induced polishing-voids would be completely disappeared.

To understand the oxidation effect of the H2O2 in the Ge-ST-film CMP slurry, the chemical composition of the surface and bulk Ge-ST film dipped into the CMP slurries including the H_2O_2 at ~40°C for 3 min were investigated by XPS and AES. In XPS, the signals of the Sb₂O₅ combined with Sb₃d^{5/2} and Sb₃d^{3/2} orbits were found at 530.7 and 539.8 eV while those of the Sb combined with $Sb_3d^{5/2}$ and $Sb_3d^{3/2}$ orbits were located at 528.5 and 538.0 eV, respectively, as shown in Fig. 4a. For the Ge-ST film dipped into the CMP slurry without H_2O_2 (i.e., the mixture of colloidal silica abrasives, HNO₃, and DI water), the signals of the Sb combined with $Sb_3d^{5/2}$ (i.e., relative intensity of ~1000) and Sb₃d^{3/2} (i.e., relative intensity of ~700) orbits were present. In addition, the signals of the Sb₂O₅ combined with Sb₃d^{5/2} (i.e., relative intensity of \sim 2402) and Sb₃d^{3/2} (i.e., relative intensity of \sim 1409) orbits were existent. This result means that the dipping of the Ge-ST film into the CMP slurry without H₂O₂ showed the signals of both the Sb₂O₅ and Sb, and thus the Ge-ST film surface was etched via corrosion. However, when the Ge-ST film was dipped into the CMP slurry including the H_2O_2 , the signals of the Sb_2O_5 combined with $Sb_3d^{5/2}$ (i.e., relative intensity of ~4202) and $Sb_3d^{3/2}$ (i.e., relative intensity of \sim 2110) were only exhibited and their signal intensities were considerably not depended on the H₂O₂ concentration, implying that the Ge-ST-film surface obviously was oxidized by the H₂O₂. In addition, the signals of the TeO₂ combined with $Te_3d^{5/2}$ and $Te_3d^{3/2}$ orbits

Experiment	Technique		Measurement	As-deposited Ge-ST film	H ₂ O ₂ concentration [wt%]			
					0	1	3	5
Fig. 2	AFM		RMS [nm]	3.1	10.4	9	6.7	4.3
Fig. 3	x-HRTEM		Ge-ST film thickness [nm]	55.5	24	-	52	55.3
Fig. 4	XPS	Intensity [a.u.]	Sb $(Sb_3d^{5/2})$ / Sb $(Sb_3d^{3/2})$	-	${\sim}1000/{\sim}700$		-	
			Sb ₂ O ₅ (Sb ₃ d ^{5/2}) / Sb ₂ O ₅ (Sb ₃ d ^{3/2})	-	~2402/~1409	~4202 / ~2110		2110
						(not depend on the		
						H_2O_2	concent	ration)
			Te $(Te_3d^{5/2}) / Te (Te_3d^{3/2})$	-	${\sim}2746$ / ${\sim}1820$		-	
			$TeO_2 (Te_3 d^{5/2}) / TeO_2 (Te_3 d^{3/2})$	-	-	\sim	988 / ~7	708
						(not depend on the H_2O_2 concentration)		on the
Fig. 5	AES		Ge-ST thickness [nm]	53		26	-	50
C			Etched Ge-ST thickness [nm]	-	31.5	18	-	-
			Chemically oxidized Ge-ST thickness [nm]	2.3	24	11	-	6.8
Fig. <mark>6</mark>	Ellipsometry		Polishing rate [nm/min]	-	53.6	25.7	19.4	20.6
-	x-HRTEM		Void size [nm]	-	43.1	20.8	0	0
			Void frequency [%]	-	100	33.3	0	0



Figure 2. SEM images of Ge-ST film surface deposited by ALD on a SiO₂-film/Si substrate. (a) as-deposited, dipped into the CMP slurry, (b) without H_2O_2 , (c) 3wt% H_2O_2 , and (d) 5wt% H_2O_2 , where rms is root-mean-square.

were found at 576.3 and 586.7 eV while the signals of the Te combined with Te₃d^{5/2} and Te₃d^{3/2} orbits were found 572.2 and 583.0 eV, respectively, as shown in Fig. 4b. For the Ge-ST film dipped into the CMP slurry without an H₂O₂, the etched Ge-ST-film surface found only the signals of the Te combined with Te₃d^{5/2} (i.e., the relative intensity of ~2746) and Te₃d^{3/2} (i.e., the relative intensity of ~1820). Otherwise, the dipping of the Ge-ST film into the CMP slurries with the H₂O₂ chemically oxidized Ge-ST-film surface, showing the signals of the TeO₂ combined with Te₃d^{5/2} (i.e., the relative intensity of ~988) and Te₃d^{3/2} (i.e., the relative intensity of ~708). This result means that the H₂O₂ in the CMP slurry chemically oxidized the Ge-ST film surface via forming TeO₂. Therefore, the XPS analysis summarizes that the dipping of the Ge-ST film into the CMP slurry without an oxidizer



Figure 3. x-HRTEM images of (a) as-deposited, dipped into the CMP slurry (b) without H_2O_2 , (c) $3wt\% H_2O_2$, and (d) $5wt\% H_2O_2$. The vertical structure of the samples was an aluminum layer, Ge-ST film, and SiO₂ film, particularly, the aluminum layer was deposited for protecting the Ge-ST-film surface during a TEM sample preparation.

demonstrated obviously a corrosion process via both etching of Sb & Te and chemical oxidation of Sb_2O_5 & TeO₂, while the dipping of the Ge-ST film into the CMP slurry with the H₂O₂ presented evidently a chemical passivation process to avoid corrosion via producing Sb_2O_5 and TeO₂. Next, the chemical-composition depth profiles of the Ge-ST films dipped in the CMP slurries were investigated by AES. For as-deposited Ge-ST film, there was almost no chemical oxidation of the Ge-ST film surface (i.e., the chemically oxidized surface thickness of ~2.3 nm) and the relative Ge, Sb, and Te composition profiles of the Ge-ST film bulk were 70, 25, and 5 at %, as shown in Fig. 5a. Note that the Ge-ST film thickness in Fig. 2a (i.e., ~55 nm)



Figure 4. XPS signals of (a) Sb 3d spectra and (b) Te 3d spectra. All Ge-ST films were dipped into the CMP slurries varied from 0, 1, 2, 3, 4, and 5 wt% at 40°C for 3 min, respectively.



Figure 5. AES profiles of (a) as-deposited Ge-ST film surface by ALD, Ge-ST films dipped into the CMP slurry (b) without an oxidizer, (c) $1wt\% H_2O_2$, and (d) $5wt\% H_2O_2$.

corresponded to the sputtering time of ~ 15 s. The Ge-ST film dipped into the slurry without an oxidizer etched ~31.5-nm-thick Ge-ST film and the remained Ge-ST film was completely chemically oxidized by forming Sb₂O₅ and TeO₂ (i.e., the chemically-oxidized surface thickness of \sim 24 nm), as shown in Fig. 5b. In addition, when the Ge-ST film was dipped into the CMP slurry including the 1 wt% H_2O_2 , the Ge-ST film surface was chemically oxidized where the oxidized Ge-ST-film thickness was ~11 nm and the remaining Ge-ST film bulk was \sim 26 nm, respectively. Thus, this result indicates that the CMP slurry etched ~18-nm-thick Ge-ST film and chemically oxidized the Ge-ST film surface by mainly producing Sb₂O₅, as shown in Fig. 5c. However, when the Ge-ST film was dipped into the CMP slurry including the H₂O₂ of 5 wt%, the Ge-ST-film surface was chemically oxidized only 6.8 nm without corrosion etching, implying that the H₂O₂ of 5 wt% well oxidized and passivated the Ge-ST film surface to avoid corrosion etching, as compared by Figs. 3d and 5d. Particularly, the oxidized Ge-ST-film-surface thickness decreased with increasing the H₂O₂ concentration in the CMP slurry; i.e., 24.0 nm for without an oxidizer, 11.0 nm for the 1 wt% H₂O₂, and 6.0 nm for the 5 wt% H₂O₂, demonstrating that a higher H₂O₂ concentration in the CMP slurry could chemically passivate well the Ge-ST film surface via producing Sb₂O₅ and TeO₂ and thus prevent the corrosion etching of the Ge-ST film surface. In addition, this AES analysis indicates that a higher H₂O₂ concentration in the CMP slurry leads to a dense chemical oxidation layer (i.e., Sb₂O₅ and TeO₂) on the Ge-ST film surface

so that the polishing rate would decrease with increasing the $\rm H_2O_2$ concentration in the CMP slurry.

To test the effect of the H_2O_2 in the CMP slurry on the suppression efficiency of the surface-tensile-stress induced polishing-voids during the CMP of the ALD Ge-ST film deposited on the confined memorycells in Fig. 1a, we investigated the CMP polishing rate, the surface film roughness, and the polishing void size & polishing void frequency, as a function of the H₂O₂ concentration in the CMP slurry. The polishing rate of the Ge-ST film using the slurry without a H₂O₂ was quite high (i.e., ~54 nm/min) because of corrosion etching and mechanical polishing. Then, it rapidly reduced to ~ 26 nm/min, and then it slightly decreased and saturated to ~20 nm/min, when the H2O2 concentration increased from 1 to 5 wt%, as shown in Fig. 6a. The decrease trend of the polishing rate along increasing the H_2O_2 concentration could be understood from the XPS analysis in Fig. 5, since a higher H_2O_2 concentration produced a dense chemical oxide layer (i.e., Sb₂O₅ and TeO_2) on the Ge-ST film surface. Note that this polishing mechanism of the Ge-ST film would be different from that of the GST film deposited by physical vapor deposition (PVD).²⁵⁻²⁷ Otherwise, after the CMP, the surface roughness of the Ge-ST-film surface considerably decreased with increasing the H2O2 concentration, since the passivation degree of the chemical oxidation layer on the Ge-ST film surface increased with the H2O2 concentration. Finally, after the CMP, the frequency and size of the surface-tensile-stress induced polishing-voids in the confined memory-cell array was remarkably decreased from 50



Figure 6. CMP performance and suppression efficiency of the surface-tensile-stress induced polishing voids depending on the H_2O_2 concentration. Dependency of (a) polishing rate and surface roughness and (b) void forming frequency and void size on the H_2O_2 concentration.

to 0% and from 43 nm to 0, respectively, when the H_2O_2 concentration increased 0 to 5 wt%. In particular, from observing surface roughness and polishing void frequency in Fig. 6b, the H_2O_2 concentration of more than 4 wt% could achieve completely free of the surface-tensilestress induced polishing-voids in the confined memory-cells after the CMP of the ALD Ge-ST-film, which was confirmed by x-HRTEM images in Fig. 7.

Conclusions

In a 3D cross-point PCM-cell array, the fabrication of the confined memory-cells filled with a phase change material would be essentially necessary to achieve minimum reset current of the PCM cells. Thus, the Ge-ST film is deposited on the confined memory-cell array by ALD and is followed by CMP. A high number of the surface-tensile-stress



Figure 7. Suppression efficiency of the surface-tensile-stress induced polishing voids depending on the H_2O_2 concentration. x-HRTEM images of the confined memory-cell array after the CMP using the slurry (a) without H_2O_2 , (b) 1wt% H_2O_2 , (c) 3wt% H_2O_2 , and (d) 5wt% H_2O_2 .

induced polishing-voids in the confined memory-cells are produced during the CMP using the slurry without an oxidizer via corrosion cracking memcahnism.²⁴ The addition of an oxidizer such as H₂O₂ in the CMP slurry can prevent the generation of the surface-tensile-stress induced polishing-voids after the CMP of the ALD Ge-ST film, since the H_2O_2 in the CMP slurry chemically well oxidized and passivated the Ge-ST-film surface via producing Sb₂O₅ and TeO₂. In particular, the design of a proper oxidizer and its concentration in a CMP slurry would be a key research to determine suppress the generation of the surface-tensile-stress induced polishing-voids in the confined memory-cells after the CMP of the ALD Ge-ST-film, strongly depending on the H₂O₂ concentration. In addition, a scaling-down of the confined PCM cells less than 10 nm to reduce reset current and to achieve a higher memory density should redesign the confined memory-cell structure, spacer material, and the CMP slurry composition such as oxidizer and corrosion inhibitor.

Acknowledgments

This work was supported by the MOTIE (Ministry of Trade, Industry & Energy) (10085643) and KSRC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor devices, Republic of Korea and the Brain-Korea 21 PLUS Program and by the National Research Foundation grant funded by MSIP (2013R1A1A2008697).

ORCID

Jea-Gun Park D https://orcid.org/0000-0002-5831-2854

References

- D. Kau, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K. W. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, and G. Spadini, *IEDM Tech. Dig.*, 617 (2019).
- N. Xu, J. Wang, Y. Deng, Y. Lu, B. Fu, W. Choi, U. Monga, J. Jeon, J. Kim, K. H. Lee, and E. S. Jung, *IEDM Tech. Dig.*, 192 (2016).
- https://www.intel.com/content/www/us/en/products/docs/memory-storage/ optane-technology/what-is-optane-technology-brief.html.
- S. Kim, M. Ishii, S. Lewis, T. Perri, M. Brightsky, W. Kim, R. Jordan, G. W. Burr, N. Sosa, A. Ray, J. P. Han, C. Miller, K. Hosokawa, and C. Lam, *IEDM Tech. Dig.*, 443 (2015).
- S. Lee, J. Jeong, Z. Wu, Y.-W. Park, W. M. Kim, and B. Cheong, *J. Electrochem. Soc.*, 156, H612 (2009).
- 6. P. Cappelletti, IEDM Tech. Dig., 241 (2015).
- S. J. Ahn, Y. J. Song, C. W. Jeong, J. M. Shin, Y. Fai, Y. N. Hwang, S. H. Lee, K. C. Ryoo, S. Y. Lee, J. H. Park, H. Horii, Y. H. Ha, J. H. Yi, B. J. Kuh, G. H. Koh, G. T. Jeong, H. S. Jeong, Kinam Kim, and B. I. Ryu, *IEDM Tech. Dig.*, 907 (2004).

- S. L. Cho, J. H. Yi, Y. H. Ha, B. J. Kuh, C. M. Lee, J. H. Park, S. D. Nam, H. Horii, B. O. Cho, K. C. Ryoo, S. O. Park, H. S. Kim, U-In. Chung, J. T. Moon, and B. I. Ryu, *Symp. VLSI Tech. Dig.*, 96 (2005).
- S. J. Ahn, Y. N. Hwang, Y. J. Song, S. H. Lee, S. Y. Lee, J. H. Park, C. W. Jeong, K. C. Ryoo, J. M. Shin, J. H. Park, Y. Fai, J. H. Oh, G. H. Koh, G. T. Jeong, S. H. Joo, S. H. Choi, Y. H. Son, J. C. Shin, Y. T. Kim, H. S. Jeong, and Kinam Kim, *Symp. VLSI Tech. Dig.*, 98 (2005).
- Y. J. Song, K. C. Ryoo, Y. N. Hwang, C. W. Jeong, D. W. Lim, S. S. Park, J. I. Kim, J. H. Kim, S. Y. Lee, J. H. Kong, S. J. Ahn, S. H. Lee, J. H. Park, J. H. Oh, Y. T. Oh, J. S. Kim, J. M. Shin, J. H. Park, Y. Fai, G. H. Koh, G. T. Jeong, R. H. Kim, H. S. Lim, I. S. Park, H. S. Jeong, and Kinam Kim, *Symp. VLSI Tech. Dig.*, 118 (2006).
- 11. S. Lai and T. Lowrey, IEDM Tech. Dig., 36.5.1 (2001).
- J. I. Lee, H. Park, S. L. Cho, Y. L. Park, B. J. Bae, J. H. Park, J. S. Park, H. G. An, J. S. Bae, D. H. Ahn, Y. T. Kim, H. Horii, S. A. Song, J. C. Shin, S. O. Park, H. S. Kim, U. I. Chung, J. T. Moon, and B. I. Ryu, *Symp. VLSI Technol. Dig. Tech. Pap.*, 102 (2007).
- I. S. Kim, S. L. Cho, D. H. Im, E. H. Cho, D. H. Kim, G. H. Oh, D. H. Ahn, S. O. Park, S. W. Nam, J. T. Moon, and C. H. Chung, *Dig. Tech. Pap. - Symp. VLSI Technol.*, 203 (2010).
- 14. M. Gill, T. Lowrey, and J. Park, Int. Solid-State Circuits Conf., 202 (2002).
- L. Van Pieterson, M. H. R. Lankhorst, M. Van Schijndel, A. E. T. Kuiper, and J. H. J. Roosen, J. Appl. Phys., 97, 083520 (2005).

- 16. J. H. Park, S. W. Kim, J. H. Kim, Z. Wu, S. L. Cho, D. Ahn, D. H. Ahn, J. M. Lee, S. U. Nam, and D. H. Ko, *J. Appl. Phys.*, **117**, 115703 (2015).
- Y. Chen, C. Rettner, Y. C. Chen, S. Raoux, and G. Burr, *Electron Devices.*, 777 (2007).
- S. Lee, J. Jeong, Z. Liu, S. Feng, and B. Chen, *J. Electrochem. Soc.*, 155, H929 (2008).
- L. Wang, B. Liu, Z. Song, S. Feng, Y. Xiang, and F. Zhang, *J. Electrochem. Soc.*, 156, H699 (2009).
- J.-Y. Cho, H. Cui, J.-H. Park, S.-H. Yi, and J.-G. Park, *Electrochem. Solid-State Lett.*, 13, H155 (2010).
- H. Cui, J.-Y. Cho, H.-S. Hwang, J.-H. Lim, J.-H. Park, H. S. Park, K. Hong, and J.-G. Park, J. Electrochem. Soc., 157, H1036 (2010).
- H. Cui, J.-Y. Cho, J.-H. Park, H. S. Park, and J.-G. Park, J. Electrochem. Soc., 158, H666 (2011).
- L. Wang, Z. Song, M. Zhong, W. Liu, W. Yan, F. Qin, A. He, and B. Liu, *Appl. Surf. Sci.*, 258, 5185 (2012).
- 24. S. B. Kim, H. Cui, J. Y. Cho, E. B. Seo, S. S. Yoon, Y. H. Son, G. P. Jeong, J. Y. Bae, J. H. Park, and J. G. Park, *Semicond. Sci. Technol.*, **34**, 065002 (2019).
- 25. Z. Song, W. Liu, and L. Wang, Procedia Engineering, 102, 582 (2015).
- 26. S. H. Yi, J. Y. Cho, and J. G. Park, J. Electrochem. Soc., 159, C546 (2012).
- A. He, L. Wang, Z. Song, B. Liu, M. Zhong, W. Yan, J. Li, and S. Feng, ECS Journal of Solid State Science and Technology, 1, P179 (2012).