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ABSTRACT

Oxide semiconductors have recently emerged as promising back-end-of-line compatible channel materials for monolithic 3D integration, addressing limitations such as scalability and thermal constraints in conventional semiconductors. However, increasing the carrier concentration in oxide semiconductors to enhance mobility often leads to conductive behavior, hindering gate control. Here, a transistor structure was demonstrated that enabled a degenerate indium oxide (In_2O_3) channel thin-film transistor to operate in enhancement mode. By forming a p–n junction between a degenerate In_2O_3 and a heavily doped p-type Si (p^{++}-Si) substrate, the local carrier concentration in the In_2O_3 was suppressed, lowering the Fermi level relative to the conduction band edge and establishing a homojunction potential barrier in the channel. This maintained the off-state at equilibrium and allowed enhancement-mode operation. With a 6-nm-thick degenerate In_2O_3 channel, the transistor achieved a field-effect mobility (μ_{FE}) of 52.7 $cm^2/V\,s$ and a threshold voltage (V_{th}) of +3.6 V. These findings demonstrated that local carrier suppression via electrostatic modulation was an effective strategy for achieving enhancement-mode transistors in high-mobility degenerate conductive metal oxides.

Conductive oxides (COs), such as In_2O_3, SnO_2, and In–Sn–O, have been extensively studied as channel materials for thin-film transistors (TFTs) owing to their high conductivity and process compatibility.[1,2] However, their intrinsically high carrier concentrations limit gate controllability. In bulk In_2O_3, the charge-neutral level (CNL) lies above the conduction-band minimum (E_C),[3] pinning the Fermi level (E_F) and leading to degenerate conduction and increased off-state leakage. To address this limitation, cation substitution approaches, such as In–Ga–Zn–O, have been widely used to reduce carrier concentration while maintaining mobility in oxide TFTs.[4–6] To enhance mobility for high-frequency and back-end-of-line (BEOL)-compatible applications,[7,8] cation composition modification[9] and heterojunction channel designs[10,11] were explored but often caused negative V_{th} shifts and depletion-mode operation. Channel-thickness scaling of In_2O_3 enables enhancement-mode operation via bandgap widening but typically sacrifices carrier concentration and mobility.[12–14]

In this study, we propose an approach that introduces a local potential barrier along the conduction path of a degenerate CO channel in a thin-film transistor, which enables enhancement-mode operation while maintaining higher mobility characteristics. The barrier was realized by placing a local carrier-suppressed (CS) region along the channel, which created a homojunction potential barrier. Specifically, when a p^{++}-Si made contact with the n-type In_2O_3, forming a p–n junction, it suppressed the local carrier concentration in the adjoining In_2O_3 channel. A potential barrier then formed at the boundary between this CS region and the neighboring degenerate In_2O_3, blocking current flow until a positive gate bias was applied, similar to the off-state barrier in a conventional MOSFET. We refer to this architecture as a carrier-suppressed semiconductor field-effect transistor (CSFET). The design suppresses leakage currents and achieves enhancement-mode operation while still using a degenerate CO channel, offering a pathway to optimize device performance. Experimental

results showed that a 6-nm-thick degenerate In_2O_3 channel TFT with a V_{th} of −3.8 V operated in enhancement mode with a positive V_{th} of 3.6 V and a ΔV_{th} of +7.4 V when the CSFET structure was applied, while maintaining a high μ_{FE} of 52.7 $cm^2/V\,s$. This was achieved not by any compositional variation or physical treatment to the metal oxide channel. The results demonstrate the significant potential of the proposed CSFET structure to address enhancement-mode operation challenges of high mobility COs, paving the way for its application in future advanced electronic devices. To investigate the carrier suppression characteristics at the In_2O_3/p^{++}-Si junction and identify the ranges of In_2O_3 film thickness (t_{InO}) and n-type carrier concentration (n_e) that enable enhancement-mode operation, we theoretically evaluated the junction profile with both TCAD simulations and an approximate one-dimensional electrostatic junction model. The required In_2O_3 band structure parameters were extracted from ultraviolet photoelectron spectroscopy and a Tauc plot (see Fig. S1). In_2O_3 exhibited an electron affinity (χ_{InO}) of 4.38 eV, a bandgap of 2.9 eV, and the E_F was positioned 0.04 eV above the E_C. Assuming an electron effective mass of $0.3m_e$ at 300 K,[15–17] the degenerate In_2O_3 channel yielded an estimated carrier concentration of $\sim 1 \times 10^{19}\ cm^{-3}$. The offset between the CNL and E_F was attributed to oxygen vacancies formed during post-deposition annealing.[18]

For p-type Si with χ_{Si} of 4.05 eV and a doping concentration of $5 \times 10^{19}\ cm^{-3}$, the E_F was located near the valence-band maximum [see Fig. 1(a)]. Density functional theory calculations indicated that enhancement-mode operation in In_2O_3 required an $E_C - E_F$ of ~0.37 eV, corresponding to a suppressed carrier concentration of $\sim 2.5 \times 10^{12}\ cm^{-3}$. Applying this criterion to the CS region established a homojunction along the conduction path, enabling enhancement-mode operation, as illustrated in Fig. 1(b). Applying the previously extracted parameters to the n-type In_2O_3/p^{++}-Si junction, simulations showed that t_{InO} that satisfied the threshold condition of $E_C - E_F \geq 0.37$ eV was approximately 6.6 nm. For $t_{InO} = 6$ nm, $E_C - E_F$ was calculated to be 0.80 eV at the junction interface and 0.46 eV at a distance of 6 nm, yielding an n_e of $1.5 \times 10^5\ cm^{-3}$ at the junction and $7.7 \times 10^{10}\ cm^{-3}$ at 6 nm away [see Fig. 1(c)]. Carrier suppression increased with decreasing t_{InO} and p_h/n_e, while thicker channels relaxed toward bulk-like behavior, as shown in Fig. 1(d).

In a one-dimensional electrostatic junction model, the maximum $E_C - E_F$ at the In_2O_3 interface was limited to ~0.87 eV by the work-function difference between p^{++}-Si and In_2O_3. For a 6-nm-thick In_2O_3 layer, quantum confinement increased E_C by only ~0.02 eV and had a negligible impact on carrier concentration (see Fig. S2). The parameters used in all simulations and junction models are provided in Table S1. In the CSFET, the In_2O_3 channel was defined across a dry-etched window formed in a 50-nm-thick SiO_2 layer on a p^{++}-Si substrate. Within this window, the In_2O_3 film directly contacted the p^{++}-Si, forming an In_2O_3/p^{++}-Si junction that served as the CS region. The overall fabrication steps are described in supplementary material Text S1, where the CSFET-specific dry-etched window formation was discussed. The In_2O_3 channel layer was subjected to post-deposition annealing at 400 °C in air, resulting in a nanocrystalline In_2O_3 phase (see supplementary material Fig. S3 and Text S2).

To assess whether the dry-etched SiO_2 window introduced geometry-related issues in the CS region, the window geometry and surface characteristics were examined by cross-sectional SEM and AFM analyses. As illustrated in Fig. 2(a), the SiO_2 dry-etching process defined a localized window exposing the p^{++}-Si surface. Cross-sectional SEM images obtained immediately after SiO_2 reactive-ion etching, prior to photoresist removal [Fig. 2(b)], revealed the initial

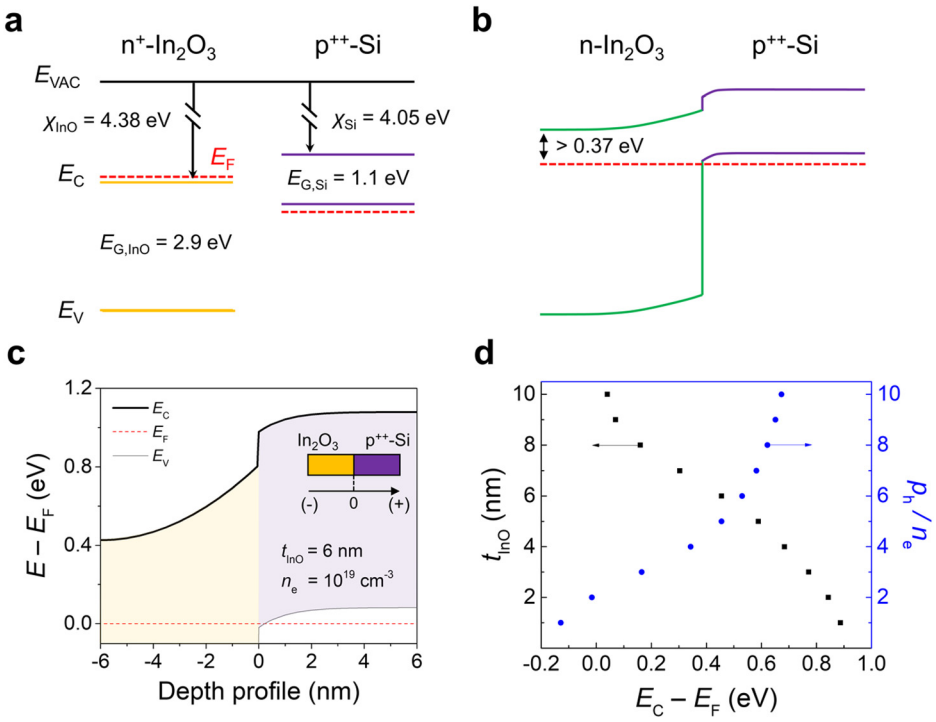

FIG. 1. Band alignment and carrier-suppression simulation of the In_2O_3/p^{++}-Si junction. (a) Isolated energy bands of In_2O_3 and p^{++}-Si. (b) Equilibrium band diagram showing the enhancement-mode criterion of $E_C - E_F \geq 0.37$ eV in In_2O_3. (c) Calculated $E_C - E_F$ profile for a 6-nm-thick In_2O_3 layer ($n_e = 1 \times 10^{19}\ cm^{-3}$). (d) $E_C - E_F$ at the point farthest from the junction as a function of In_2O_3 thickness and p_h/n_e ratio.

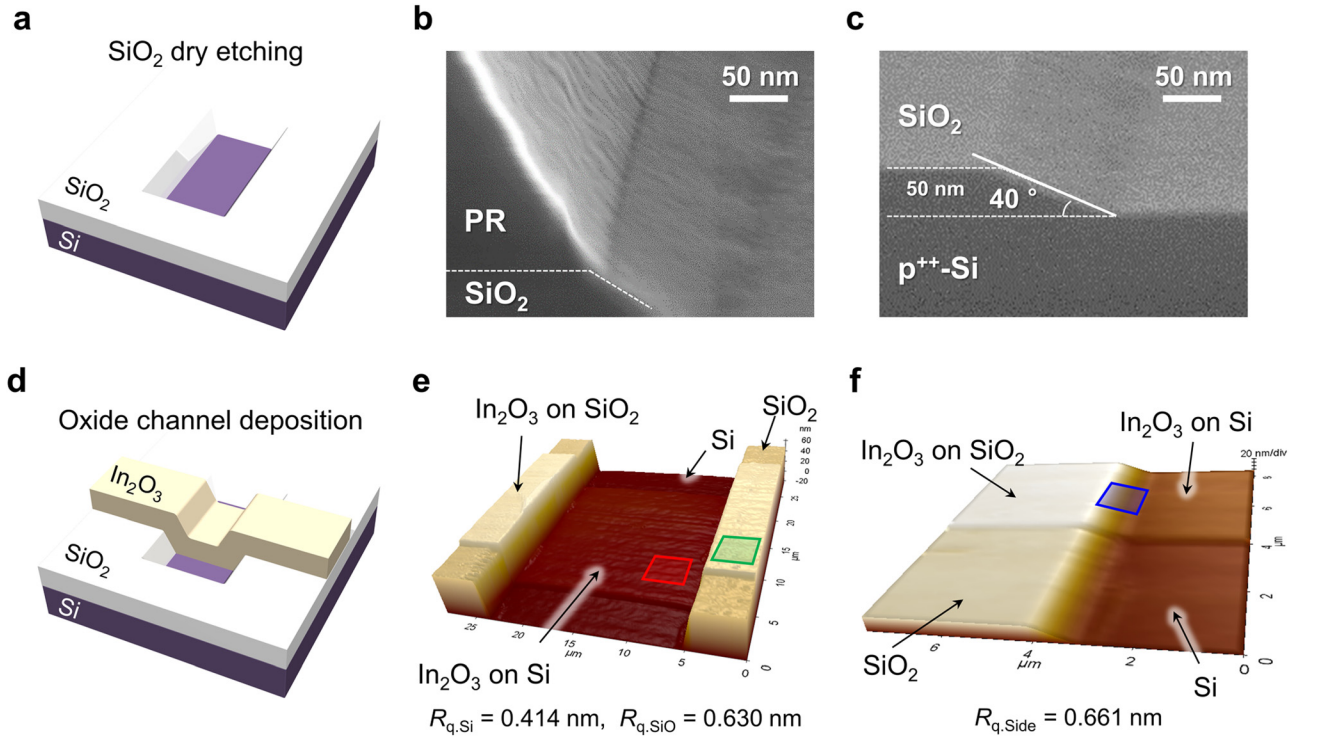

FIG. 2. Fabrication and structural characterization of the In_2O_3/p^{++}-Si junction. (a) Schematic of the SiO_2 dry-etched window exposing the p^{++}-Si surface. Cross-sectional SEM images obtained (b) before and (c) after photoresist removal, showing a SiO_2 sidewall angle of ~40°. (d) Schematic of the In_2O_3/p^{++}-Si junction after In_2O_3 deposition. AFM topography images of the post-deposition surface (e) on Si and planar SiO_2 and (f) along the SiO_2 sidewall.

sidewall profile. After photoresist removal, a SiO_2 sidewall with an angle of approximately 40° relative to the substrate surface was observed, indicating the absence of an abrupt geometrical discontinuity at the window edge and suggesting that continuous oxide deposition along the sidewall was feasible without step-coverage concerns. Following oxide channel deposition, the resulting In_2O_3/p^{++}-Si junction configuration is schematically shown in Fig. 2(d). AFM analysis of the surfaces [Figs. 2(e) and 2(f)] showed that the root mean square surface roughness (R_q) of In_2O_3 deposited on the SiO_2 sidewall (0.661 nm) was comparable to that on planar SiO_2 (0.630 nm) and Si (0.414 nm) regions, indicating relatively uniform surface morphology without pronounced roughness variation or localized geometrical irregularities near the CS boundary. Taken together, the SEM and AFM observations indicated that the etched-window geometry was unlikely to introduce step-coverage issues or geometry-induced electric-field crowding.

The cross-sectional illustration and the optical microscope image of the fabricated In_2O_3/p^{++}-Si junction, prior to Al_2O_3 gate dielectric layer deposition, are shown in Fig. 3(a). The current–voltage (I–V) characteristics revealed a typical rectifying behavior indicating the formation of a p–n junction, as shown in Fig. 3(b). The capacitance–voltage (C–V) measurements were carried out to determine the height of the In_2O_3 homojunction energy barrier created by the local carrier suppression, as shown in Fig. 3(c). The energy barrier height (ϕ_{Bi}) was derived using the relationship $1/C^2 = 2(\phi_{Bi} + V_r)/(q \cdot \varepsilon_S \cdot N_C \cdot A^2)$, where V_r, q, ε_S, and A are the applied reverse bias voltage, elementary charge, permittivity of the semiconductor, and junction area, respectively. This relationship describes the dependence of the capacitance on ϕ_{Bi} and V_r. The results indicate an x-intercept of approximately 0.48 eV, which we interpret as the highest possible energy barrier height along the equilibrium p–n junction pathway in In_2O_3.[19] Candidate barriers included the homojunction barrier, the Schottky barrier at the metal–semiconductor junction, and the conduction band offset at the In_2O_3/p^{++}-Si junction. The capacitance at the homojunction was $\sim 10^4$ times lower than that of the p–n junction, so it dominated the series capacitance, and the p–n junction barrier contribution could be neglected. Band alignment calculations also confirmed this conclusion. Based on the work function of W (4.55 eV)[20] and χ_{InO} (4.38 eV), the theoretical maximum Schottky barrier was calculated to be 0.17 eV. The conduction band offset between In_2O_3 and bulk Si, derived from their electron affinities (with Si at 4.05 eV), was 0.33 eV. Since both the 0.17 and 0.33 eV values were lower than the measured 0.48 eV, this strongly suggested that the observed energy barrier corresponded specifically to the homojunction barrier. Carrier suppression then reduced the n_e in In_2O_3 from the initial 1×10^{19} to 3.6×10^{10} cm^{-3}, representing a nearly 9 orders of magnitude reduction. The derived n_e was similar, within an order of magnitude, to the previously calculated value of 7.7×10^{10} cm^{-3}. At equilibrium [point D in Figs. 3(b) and 3(d)], an n-type In_2O_3 that underwent carrier suppression separates the degenerate In_2O_3 and p^{++}-Si, forming a p–n junction. Under reverse bias [$V_p = -1$ V, V_n = GND; point E in Figs. 3(b) and 3(e)], a reverse current that saturated at around 10 nA was observed. It seemed unlikely

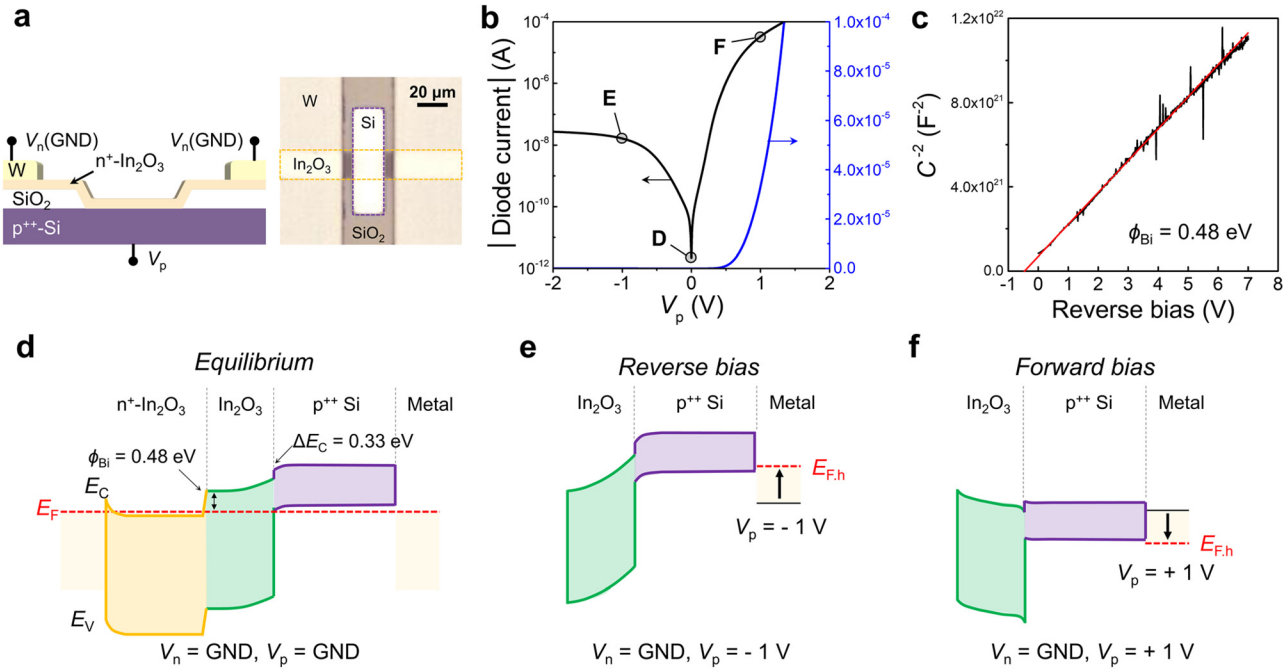

FIG. 3. Characteristics of the In_2O_3/p⁺⁺-Si junction. (a) Schematic cross section and optical micrograph. (b) *I–V* characteristics measured at $V_n = 0$ V with V_p swept from −2 to +2 V (log scale: black; linear scale: blue). (c) *C–V* characteristics measured under reverse bias ($V_p < 0$, $V_n = 0$ V). Band diagrams showing (d) equilibrium ($V_n = V_p = 0$ V), (e) reverse bias ($V_n = 0$ V, $V_p = -1$ V), and (f) forward bias ($V_n = 0$ V, $V_p = +1$ V). Here, V_n and V_p denote the cathode and anode biases.

that this was electron drift current from Si to In_2O_3 since the bulk p⁺⁺-Si had an extremely low electron concentration. Similarly, hole drift current from In_2O_3 to bulk p⁺⁺-Si was also improbable due to the extremely low concentration of holes in the oxide semiconductor, where the valence band is composed of localized 2p orbitals.[21] Thus, band-to-band tunneling of electrons below the valence band of p⁺⁺-Si to the conduction band of In_2O_3 was a plausible explanation for the saturated reverse bias current.[22] If carrier suppression was not present, we can expect a much higher reverse bias current since the empty conduction band states in the In_2O_3 would have been accessible to the holes from the p⁺⁺-Si without additional energy.[23] Under forward bias [$V_p = +1$ V, V_n = GND; F in Figs. 3(b) and 3(f)], a significant energy barrier of over 2 eV would prevent holes from p⁺⁺-Si to be injected into In_2O_3. Thus, the forward bias current was due to electron diffusion from In_2O_3 to bulk p⁺⁺-Si, overcoming the homojunction barrier via high electric field and thermal energy assistance.[24] However, this mode of bias will not be present during CSFET operation and should not contribute to the device current.

The simplified circuit diagram, schematic cross section, and optical micrograph of the fully fabricated In_2O_3 CSFET device are presented in Fig. 4(a). The circuit highlights the CS region by assigning an auxiliary node V_{CS} to that part of the channel. This notation distinguishes the CSFET from a conventional top-gate TFT, whose channel lacks a CS region. In the optical microscope image, the degenerate In_2O_3 layer on SiO_2 and the $20 \times 20\ \mu m^2$ area that contacts p⁺⁺-Si and defines the CS region could be seen. The effect of regional carrier suppression on V_{th} shift was clearly demonstrated in the transfer characteristics shown in Fig. 4(b). Current saturation was observed in the output characteristics shown in the inset of Fig. 4(b) as V_D increased, indicating channel pinch off and suggesting that carrier suppression had induced semiconducting behavior in the CO channel. The conventional reference top-gate In_2O_3 TFT exhibited a V_{th} of −3.8 V, operating in depletion mode, with a μ_{FE} of 31.7 cm^2/V s. In contrast, the CSFET demonstrated a significant positive shift in V_{th}, transitioning to 3.6 V. This shift enabled the CSFET to function in enhancement mode without having any compositional change or additional treatment to the channel material. At $V_G = 0$ V and $V_D = 3.1$ V, the reference TFT did not switch off, whereas the CSFET remained on the off-state. From the transfer characteristics, it can be seen that the transconductance (g_m) of the In_2O_3 CSFET was increased by 52.5% to 60.1 μS, compared to that of the reference device (at $V_D = 3.1$ V) and the μ_{FE} increased by 66.2% to 52.7 cm^2/V s (at $V_D = 0.1$ V) [Fig. 4(c)]. The μ_{FE} was calculated using the relation $\mu_{FE} = g_m \cdot L/(W \cdot C_{ox} \cdot V_D)$, where L and W denote the effective channel length and channel width, and C_{ox} denotes the oxide capacitance.[25] The observed enhancement in μ_{FE} was associated with changes in g_m under gate bias. Although the equilibrium carrier concentration in the CS region was strongly reduced by p–n junction-induced band bending, this suppression did not originate from impurity doping. Under positive gate bias, the homojunction barrier in the CS region was reduced, allowing carrier accumulation to be restored along the conduction path [see Figs. 4(d)–4(f)]. As a result, μ_{FE} could be maintained at a level comparable to that of the reference device. In addition, local carrier suppression may have contributed to enhanced gate modulation by partially alleviating charge screening. Furthermore, the smoother In_2O_3/p⁺⁺-Si interface compared to In_2O_3/SiO_2 [Figs. 2(e) and 2(f)] was expected to reduce

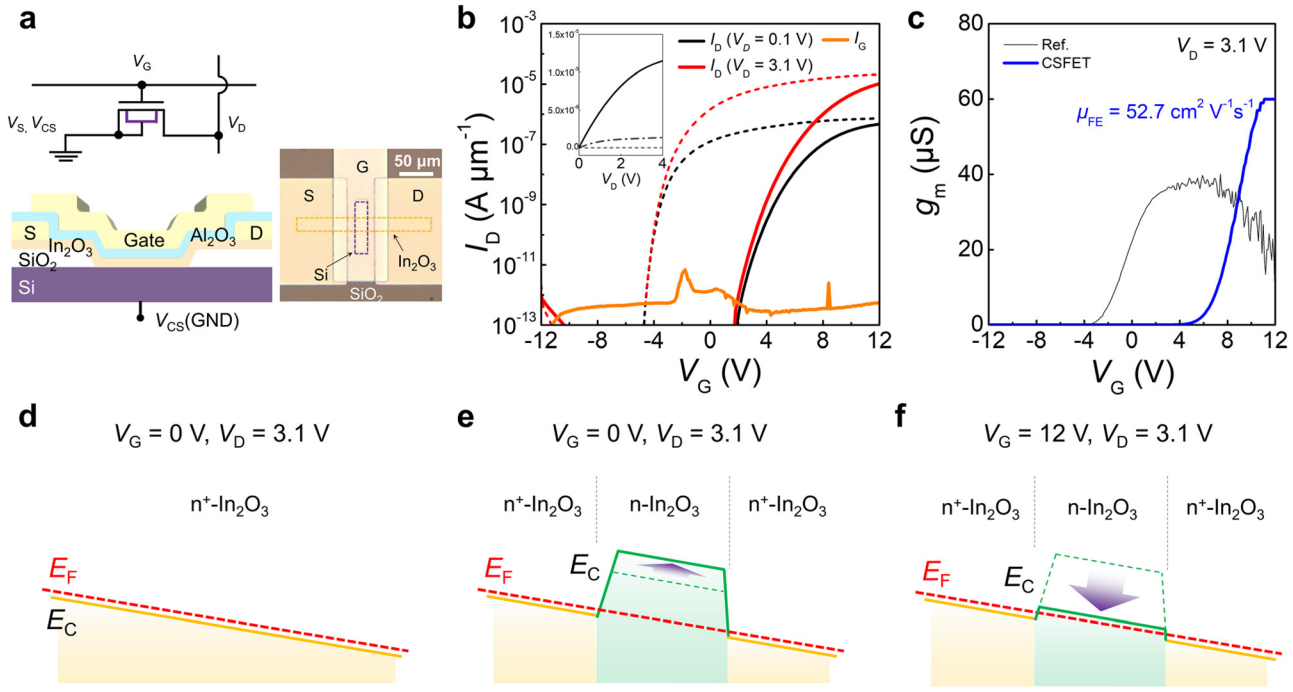

FIG. 4. Operating characteristics of the In_2O_3 CSFET. (a) Schematic cross section, optical micrograph, and simplified circuit diagram. (b) Transfer characteristics measured at $V_S = V_{CS} = 0$ V for the CSFET shown as a solid line and the reference top-gate In_2O_3 TFT shown as a dashed line. Inset output characteristics measured at $V_G = +4$ V (dashed), +8 V (dashed-dotted), and +12 V (solid). (c) g_m of the reference TFT shown in black and the CSFET shown in blue. The extracted μ_{FE} corresponds to the CSFET. Band diagrams of (d) the reference TFT at $V_G = 0$ V and $V_D = 3.1$ V, (e) the CSFET at $V_G = 0$ V and $V_D = 3.1$ V, and (f) the CSFET at $V_G = 12$ V and $V_D = 3.1$ V.

interface-related scattering, contributing to the higher μ_{FE} observed in the CSFET. To clarify the origin of the drain current, the possible involvement of p–n junction leakage under on-state CSFET operating conditions was examined, as detailed in supplementary material Text S3 and Fig. S4. In addition, to verify the presence of carrier suppression in the proposed device, In_2O_3 thickness-dependent transport behaviors were examined in supplementary material Text S4 and Fig. S5, where we can observe a higher degree of V_{th} shift as the channel becomes thinner, which follows the results obtained by simulations shown in Fig. 1(d). The CSFET exhibited a larger subthreshold swing (*SS*) of 197 mV/dec compared with 130 mV/dec for the reference device, despite the identical gate dielectric. This increase was attributed to an increased effective capacitance associated with the CS region, due to ionized dopants in the p^{++}-Si substrate, which may have weakened gate-to-barrier coupling in the subthreshold regime. Meanwhile, the contact regions in both devices remained unchanged, consisting of a degenerate In_2O_3/W junction, resulting in similar contact resistance values of approximately 56 kΩ μm. The CSFET structure yields low contact resistance because while the metal–semiconductor work-function difference fixes the Schottky barrier height, the degenerately doped In_2O_3 beneath the contacts supplies a high n_e that narrows the Schottky barrier width (W_{SB}) given by $W_{SB} = \{2\varepsilon_n V_{bi}/(qn_e)\}^{1/2}$, where V_{bi} is the built-in potential at the In_2O_3/W junction.[19] The resulting narrower W_{SB} enhances carrier tunneling through the barrier and thus keeps the contact resistance at a minimal state. A summary of the key electrical characteristics (I_{on}, I_{on}/I_{off}, V_{th}, and *SS*) for the CSFET is provided in Table S2.

To understand the conduction process, the energy band structure was examined. In reference to the In_2O_3 top-gate TFT, the channel region remained in a degenerate state with $E_F - E_C \approx 0.02$ eV, and only Schottky barriers of approximately 0.17 eV were formed at the source and drain, which were insufficient to suppress current leakage [Fig. 4(d)]. In contrast, the proposed device exhibited a pronounced homojunction barrier of ~0.72 eV in the CS region, corresponding to an approximately 10^{12}-fold reduction in electron concentration [Fig. 4(e)]. When a positive gate bias was applied, this homojunction barrier was significantly reduced, allowing carrier accumulation to be restored and enabling the CS region to function as the effective transport channel [Fig. 4(f)], consistent with the recovery of current and μ_{FE} to levels comparable to those of the reference device.

Other techniques for local modulation of n_e have been reported, including oxygen and fluorine plasma treatments that realized enhancement-mode operation.[26–28] However, plasma-based approaches often degraded mobility through defect formation[21,29,30] and suffered from limited depth control. In contrast, the CSFET enables conduction-band modulation without any chemical modification, relying solely on junction-mediated electrostatic control. Comparable junction-based effects have been observed in other material systems[24,31–34] and similar approaches to achieve enhancement mode operation, such as incorporating a localized metal oxide heterojunction or capping layer,[35–39] supporting the validity of this method as a reliable strategy. However, the key structural concept of the CSFET of local carrier suppression by introducing a reverse biased p–n junction may be applied to other conductive metal oxide and semiconductor channels, unlike the

above-mentioned methods, and may enable enhancement-mode operation with high μ_{FE}. Furthermore, it may be possible to create similar carrier suppression effects with deposited p-type semiconductors, such as polysilicon, enabling 3D integration, in which case the level of carrier suppression and thereby V_{th} shift may be fine-tuned by controlling the p-type doping concentration. Therefore, the CSFET concept for high μ_{FE} metal oxide TFT operating in enhancement mode would be highly applicable to multifunctional BEOL integration with current semiconductor technology.

See the supplementary material for UPS and bandgap analysis, TCAD parameters, fabrication details, and supporting electrical data.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jiyoung Bang and Seungjae Lee contributed equally to this work.

Jiyoung Bang: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Software (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead). **Seungjae Lee:** Data curation (lead); Formal analysis (equal); Investigation (lead); Methodology (equal); Validation (lead); Visualization (equal); Writing – review & editing (lead). **Kyubin Hwang:** Data curation (equal); Formal analysis (equal); Investigation (lead). **Hyeonjeong Sun:** Conceptualization (supporting); Funding acquisition (equal); Methodology (equal). **Seungmin Choi:** Data curation (supporting); Formal analysis (supporting); Investigation (equal). **Youngsoo Noh:** Data curation (supporting); Formal analysis (supporting); Investigation (equal). **Hyowon Kim:** Investigation (supporting); Methodology (supporting); Validation (lead). **Yeoeun Yun:** Investigation (supporting); Methodology (supporting); Validation (equal). **Eunsuk Choi:** Conceptualization (equal); Funding acquisition (equal). **Jae Kyeong Jeong:** Resources (supporting); Supervision (supporting). **Seung-Beck Lee:** Conceptualization (equal); Funding acquisition (lead); Project administration (lead); Resources (lead); Supervision (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]H. A. Klasens and H. Koelmans, Solid State Electron. **7**, 701 (1964).
[2]K. Ellmer, Nat. Photonics **6**, 809 (2012).
[3]A. Charnas, Z. Zhang, Z. Lin, D. Zheng, J. Zhang, M. Si, and P. D. Ye, Adv. Mater. **36**, 2304044 (2024).
[4]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**, 488 (2004).
[5]J. Lee, D. Kim, D. Yang, S. Hong, K. Yoon, P. Hong, C. Jeong, H. Park, S. Y. Kim, S. K. Lim, S. S. Kim, K. Son, T. Kim, J. Kwon, and S. Lee, SID Symp. Dig. Tech. Pap. **39**, 625 (2008).
[6]S. Kang, B. Kim, G.-B. Kim, and J. K. Jeong, ACS Appl. Mater. Interfaces **17**, 47230 (2025).
[7]Y.-S. Shiah, K. Sim, Y. Shi, K. Abe, S. Ueda, M. Sasase, J. Kim, and H. Hosono, Nat. Electron. **4**, 800 (2021).
[8]S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, IEEE Micro **39**, 8–15 (2019).
[9]M. H. Cho, C. H. Choi, H. J. Seul, H. C. Cho, and J. K. Jeong, ACS Appl. Mater. Interfaces **13**, 16628 (2021).
[10]H. Faber, S. Das, Y.-H. Lin, N. Pliatsikas, K. Zhao, T. Kehagias, G. Dimitrakopulos, A. Amassian, P. A. Patsalas, and T. D. Anthopoulos, Sci. Adv. **3**, e1602640 (2017).
[11]M. Lee, J. Jo, Y. Kim, S. Choi, S. M. Kwon, S. P. Jeon, A. Facchetti, Y. Kim, and S. K. Park, Adv. Mater. **30**, 1804120 (2018).
[12]S. Li, M. Tian, Q. Gao, M. Wang, T. Li, Q. Hu, X. Li, and Y. Wu, Nat. Mater. **18**, 1091 (2019).
[13]M. Si, Y. Hu, Z. Lin, X. Sun, A. Charnas, D. Zheng, X. Lyu, H. Wang, K. Cho, and P. D. Ye, Nano Lett. **21**, 500 (2021).
[14]M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, Nat. Electron. **5**, 164 (2022).
[15]H. K. Müller, Phys. Status Solidi B **27**, 733 (1968).
[16]H. Fujiwara and M. Kondo, Phys. Rev. B **71**, 075109 (2005).
[17]N. Preissler, O. Bierwagen, A. T. Ramu, and J. S. Speck, Phys. Rev. B **88**, 085305 (2013).
[18]J.-Y. Lin, Z. Zhang, Z. Lin, Y. Zhang, Y. Zhang, T. Kim, H. Jang, C. Sung, M. Hong, S. M. Lee, T. Lee, M. H. Cho, D. Ha, C. Jeong, H. Wang, M. A. Alam, and P. D. Ye, IEEE Electron Device Lett. **45**, 1851 (2024).
[19]C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, 1st ed. (Pearson, 2010).
[20]H. B. Michaelson, J. Appl. Phys. **48**, 4729 (1977).
[21]O. Bierwagen, J. S. Speck, T. Nagata, T. Chikyow, Y. Yamashita, H. Yoshikawa, and K. Kobayashi, Appl. Phys. Lett. **98**, 172101 (2011).
[22]O. Sul, Y. Lee, S. Kim, M. Kwon, H. Sun, J. Bang, H. Ju, E. Choi, and S.-B. Lee, Nanotechnology **34**, 035201 (2023).
[23]D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, Nature **526**, 91 (2015).
[24]O. Sul, H. Seo, E. Choi, S. Kim, J. Gong, J. Bang, H. Ju, S. Oh, Y. Lee, H. Sun, M. Kwon, K. Kang, J. Hong, E. Yang, Y. Chung, and S.-B. Lee, Small **18**, 2202153 (2022).
[25]A. Yan, C. Wang, J. Yan, Z. Wang, E. Zhang, Y. Dong, Z.-Y. Yan, T. Lu, T. Cui, D. Li, P. Shen, Y. Jin, H. Liu, Y. Yang, and T.-L. Ren, Adv. Funct. Mater. **34**, 2304409 (2024).
[26]R. Hu, Y. Pei, Z. Chen, J. Yang, Y. Li, J. Lin, Y. Zhao, C. Wang, J. Liang, B. Fan, and G. Wang, IEEE Electron Device Lett. **36**, 1163 (2015).
[27]A. Charnas, M. Si, Z. Lin, and P. D. Ye, Appl. Phys. Lett. **118**, 052107 (2021).
[28]Y.-C. Chang, S.-T. Wang, Y.-T. Lee, C.-S. Huang, C.-H. Hsu, T. Ting. Weng, C.-C. Huang, C.-W. Chen, T.-T. Chou, C.-Y. Chang, W.-Y. Woon, C.-L. Lin, J. Y.-C. Sun, and D.-H. Lien, Adv. Mater. **37**, 2413212 (2025).
[29]P. Ágoston, P. Erhart, A. Klein, and K. Albe, J. Phys.: Condens. Matter **21**, 455801 (2009).
[30]L. Liu, C.-C. He, J. Zeng, Y.-H. Peng, W.-Y. Chen, Y.-J. Zhao, and X.-B. Yang, J. Phys. Chem. C **125**, 7077 (2021).
[31]B. Rajasekharan, C. Salm, R. J. E. Hueting, T. Hoang, and J. Schmitz, in 9th International Conference on Ultimate Integration of Silicon, 2008.
[32]R. J. E. Hueting, B. Rajasekharan, C. Salm, and J. Schmitz, IEEE Electron Device Lett. **29**, 1367 (2008).
[33]M. J. Kumar and S. Janardhanan, IEEE Trans. Electron Devices **60**, 3285 (2013).
[34]C. C. Sahu and J. Singh, IEEE Electron Device Lett. **35**, 411 (2014).
[35]Y. Shin, S. T. Kim, K. Kim, M. Y. Kim, S. Oh, and J. K. Jeong, Sci. Rep. **7**, 10885 (2017).
[36]X. Wang, S. Yan, W. Mu, Z. Jia, J. Zhang, Q. Xin, and A. Song, IEEE Electron Device Lett. **43**, 44–47 (2022).
[37]H. Sun, J. Bang, H. Ju, S. Choi, Y. Lee, S. Kim, Y. Noh, E. Choi, J. K. Jeong, and S.-B. Lee, Nanotechnology **35**, 355202 (2024).
[38]J. H. Han, D. Y. Shin, C. Sung, S. H. Cho, K.-B. Chung, and S. Nam, ACS Appl. Mater. Interfaces **16**, 31254 (2024).
[39]Y. Zhang, S. Siram, and K. Nomura, IEEE Electron Device Lett. **46**, 294 (2025).