

A novel three-dimensional NAND flash structure for improving the erase performance

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Abstract: In this paper, the Indium Gallium Zinc Oxide (IGZO)-Oxide-P-filler (IOP) structure is proposed to improve the poor erase performance of three-dimensional (3D) NAND flash structures using IGZO channel. First, the erase performance of the polysilicon channel and the IGZO channel of the 3D NAND flash structure were compared. During this simulation, the IGZO channel displayed a low 0.06 V erase performance. To solve this problem, the proposed IOP structure was able to produce a memory window of 5.29 V. Based on these results, we confirmed that the IOP structure can greatly improve erase performance, which is the largest obstacle in using the IGZO channel.

Keywords: flash memory, 3D NAND, indium gallium zinc oxide (IGZO)

Classification: Electron devices, circuits and modules

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1 Introduction

To meet market demands and overcome integration limits, the NAND flash architecture has evolved from the existing 2D structure to a 3D structure [1, 2, 3], and recently, a structure having more than 100 vertical word lines is being developed [4]. However, the vertical channel material currently in use is polysilicon. Polysilicon presents numerous issues, including operating current decrease, leakage current increase, and increase in threshold voltage (V_{th}) scattering due to the presence of grain boundaries [5, 6]. To resolve the issues with polysilicon, numerous replacement channel materials have been studied. In recent years, IGZO has been suggested as a possible candidate, as its wide bandgap produces a desirable low leakage current [7, 8, 9].

As described above, IGZO has desirable leakage current, operating current, and V_{th} distribution characteristics. However, conversely, the IGZO has a very low hole concentration and a very large band gap. Therefore, hole erasing (the only erase method used in a vertical channel NAND flash structure) cannot be used. To overcome this drawback, we proposed an IOP structure which utilizes a field erase method, as opposed to a hole erase method. The proposed structure was verified and analyzed through device simulation.

2 IOP structure

Fig. 1a and b show the general V-NAND-TCAT [2] structure and the proposed IOP structure. In addition to the TCAT structure, the proposed IOP structure adds a p-type filler (P-filler) to the center of the hole (blue). This filler is connected to the P-Sub area at the bottom of the structure. Here, the filler assists the high voltage applied to the P-sub region to be quickly transferred to the entire channel during the erase operation. When high voltage is supplied to the channel by the filler, the field erase is possible by the potential difference between the high voltage of the IGZO channel and the ground voltage of each WL.

The operation of the proposed structure is the same as the existing TCAT structure. However, given that the high voltage due to the added p-type filler is uniformly distributed throughout the channel, the erase operation proceeds across all WLs.

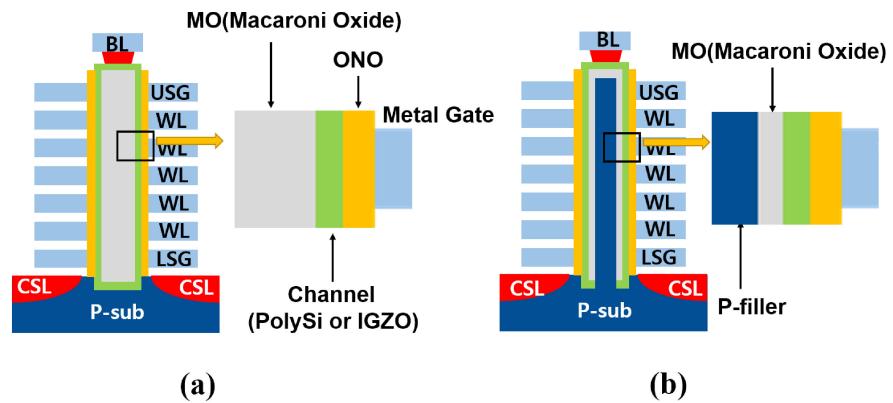


Fig. 1. Comparison between 3D NAND flash and IOP structure. (a) is Single string of TCAT and (b) is Single string of IOP

3 Simulation results and analysis

In this paper, Sentaurus TCAD [10] from Synopsys was used for simulation verification of the proposed structure. Table I and Fig. 2 show the structure and parameters used in device simulation. In addition to the parameters shown in the table, material parameters other than IGZO are referenced from [10] and material parameters of IGZO are referenced from [11]. The simulation structure in Fig. 2a uses a cylindrical command in the Sentaurus simulation tool to rotate one half of a vertical string section 360 degrees to create a complete cylindrical structure. Doping dependence, high field saturation, Shockley-Read-Hall, Auger, and band-to-band recombination models were used in the device simulations. In addition, Poole-Frenkel and nonlocal tunneling models [10] were also used to simulate tunneling phenomenon in the memory operation.

Table I. The physical parameters used in the device simulation.

Parameter	Value
Total height (a-Blue) (μm)	11.92 (96 WL)
Hole radius (a-Red) (nm)	62
WL height (nm)	40
WL–WL height (nm)	40
O/N/O Thickness (nm)	4/7/11
MO Thickness in IOP (nm)	10 – 2
P-filler thickness in IOP (nm)	10 – 18
Sub doping (cm^3)	5×10^{18}
BL, CSL doping (cm^3)	1×10^{20}
Electron trap density in channel (cm^3)	1×10^{21} (polysilicon), 1.55×10^{20} (IGZO)
Hole trap density in channel (cm^3)	1×10^{21} (polysilicon), 1.55×10^{20} (IGZO)

Figs. 3a and b show the results of program and erase, respectively, for polysilicon and IGZO channel materials.

Initially, the program operates normally regardless of the channel material. However, during the erase operation, as expected, the erase operation has limited progression in the case of the IGZO channel, reaching only 0.06 V at 0.1 ms.

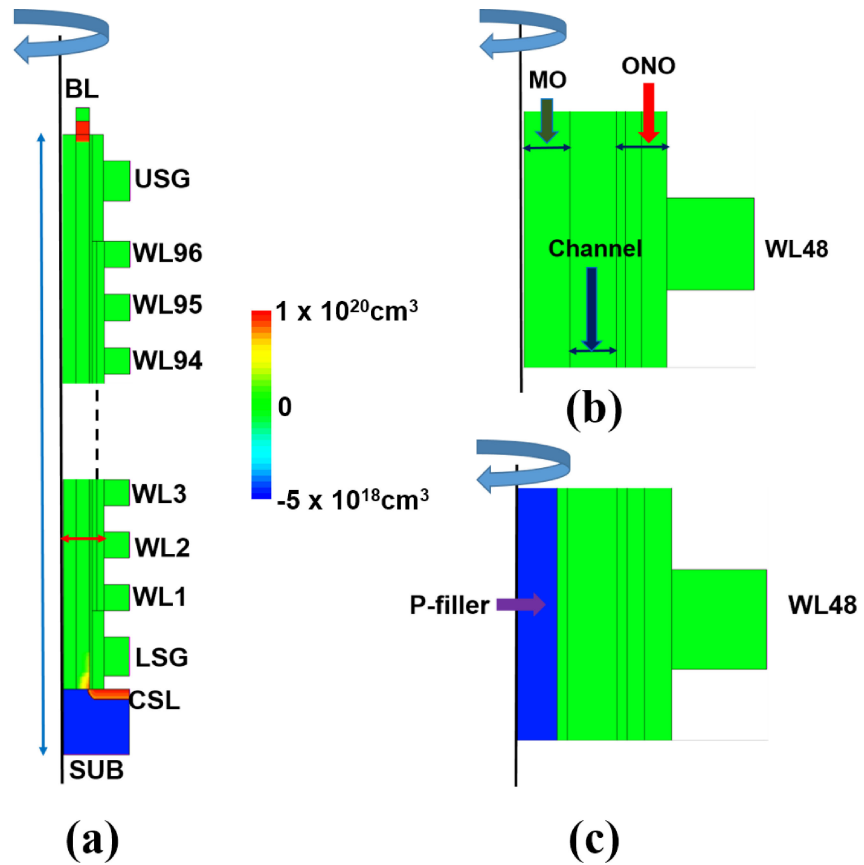


Fig. 2. Details of structure and doping concentration used in device simulation. (a) is Overall structure details, (b) is Structure details at the WL48 in TCAT and (c) is Structure details at the WL48 in IOP

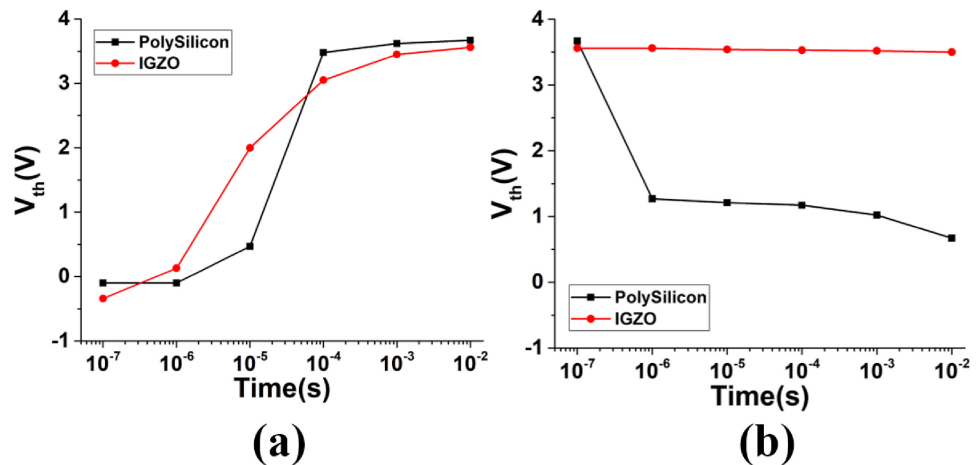


Fig. 3. Memory operation results. (a) is Programming operation results, (b) is erasing operation results.

These results can be explained by a and b in Fig. 4. As can be seen in c, the hole density of IGZO during the erase operation is 1019 times smaller than that of the polysilicon channel, rendering it virtually nonexistent. In addition, IGZO's high bandgap (E_{g1}) produces a very high barrier ($E_{g1}/2$), limiting the movement of the hole in the P + sub to the channel.

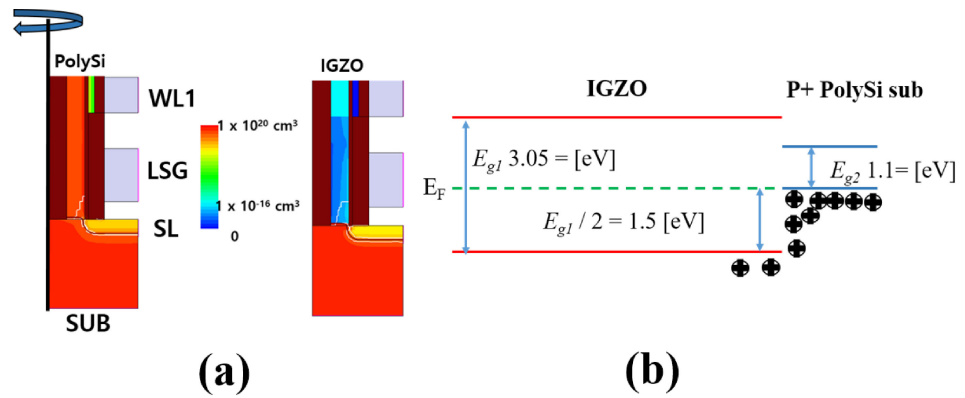


Fig. 4. Analysis in the polysilicon channel and IGZO channel structure. (a) is Hole density in each channel during the erase and (b) is explanation of energy band gap and hole movement in IGZO and P-sub in the erase operation.

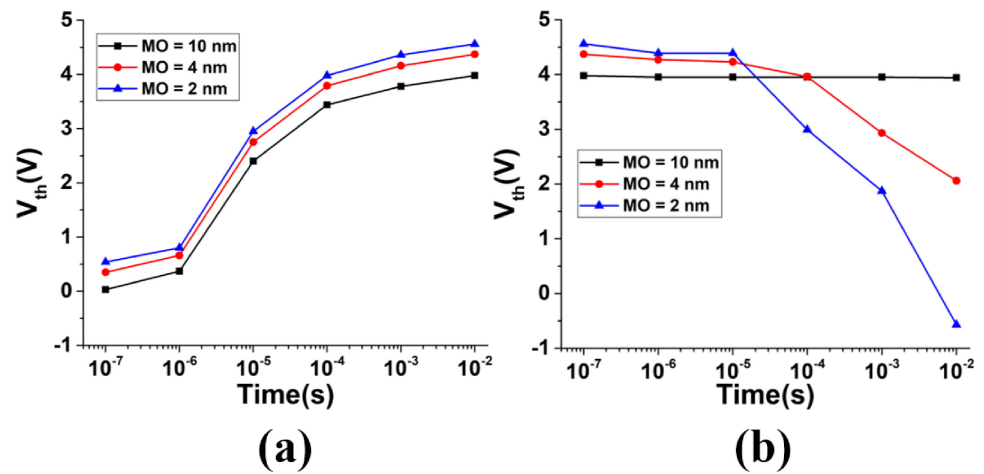


Fig. 5. Improvement in the erase operation performance due to the decreased thickness of MO. (a) is Programming operation results, (b) is Erasing operation results.

Next, a and b in Fig. 5 show memory operation results according to the thickness of MO in the proposed IOP structure (IGZO channel). Initially, as shown in a, the program operation characteristics are similar regardless of the MO thickness. However, during the erase operation (shown in b), the operating characteristic increases to 5.29 V as a function of the decreased MO thickness. These results indicate that normal memory operation is possible in the IGZO channel when the proposed structure is applied.

The improvement in erase performance with MO thickness reduction in the IOP structure can be explained in Fig. 6a and b. In the erase operation, the high voltage generated in the p-type filler experiences stronger transmission to the IGZO channel as the thickness of the MO decreases, thus creating a potential at the channel/tunnel oxide boundary and ultimately determining the erase performance. Simulation results show that the erase performance increases sharply when the potential at the channel/tunnel oxide boundary exceeds 8 V. Therefore, the potential at the channel/tunnel oxide interface can be raised even if the thickness of both the channel and the MO are reduced.

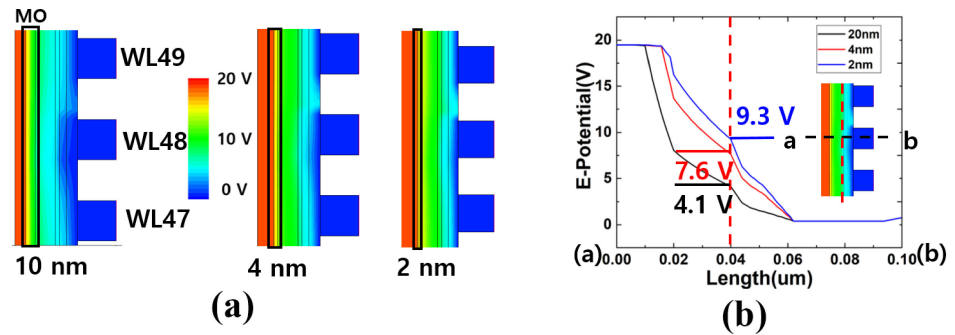


Fig. 6. (a) Indication of electrical potential increase in IGZO channel/tunnel oxide due to decrease in MO thickness and (b) is cross section of electrical potential.

4 Conclusion

In this paper, we proposed an IOP structure to improve erase performance in vertical channel NAND flash architecture by utilizing an IGZO channel. The IOP structure was verified and analyzed through device simulation. Simulation results show that erase performance is greatly improved by the thickness of MO when the proposed structure is applied. This result indicates that it is possible for IGZO to overcome poor erase performance (due to poor hole concentration) while still maintaining the desirable characteristics of IGZO.

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