Appl. Sci. Converg. Technol. 29(6): 183-185 (2020)
https://doi.org/10.5757/ASCT.2020.29.6.183
eISSN : 2288-6559

Research Paper Check for updates

Memory Characteristics of Capacitors with Poly-GaP Floating Gates

Received September 23, 2020; revised November 20, 2020; accepted November 20, 2020

Sang Hoon Shin[a], Young Taek Oh[a], Jin Dong Song[b], and Yun Heub Song[a,*]

[a]Department of Electronics Engineering, Hanyang University, Seoul 04763, Republic of Korea
[b]Center of Opto-Electronic Materials and Devices, Korea Institute of Science and Technology, Seoul 02792, Republic of Korea

*Corresponding author E-mail: yhsong2008@hanyang.ac.kr

ABSTRACT

We fabricated a capacitor with polycrystalline gallium phosphide (Poly-GaP), which has high thermal immunity for better CMOS compactness, as a floating gate. Using a phosphide beam flux, in a molecular beam epitaxy chamber, 0.5 μm of Poly-GaP film was successfully grown on silicon at 250 ℃. Its device characteristics were compared with capacitors that instead used Poly-GaAs and Poly-Si. It is revealed that the memory window for the capacitor with the Poly-GaP floating film is comparable to the Poly-GaAs one, and still shows approximately twice the value of the Poly-Si. Based on these results, we conclude that flash memory with a Poly-GaP floating material can provide not only a wider memory window due to significant traps in III-V compounds, but also thermal immunity of the GaP material, which can be applied for 2D scaled flash memory.

Keywords: III-V floating gate, III-V memory, Memory window, Molecular beam epitaxy, Polycrytalline gallium phosphide

1. Introduction

In recent years, two-dimensional NAND flash memory innovation has transcended 20-nm technology. Nevertheless, there remain several challenges to scaling it down. The most critical issue arises when a small memory window of a tiny cell for multi-bit operation expands. The memory window width determines the charge trap density based on the floating gate material, coupling ratio, cell-to-cell interference, etc. [1–6]. Considerable effort has been devoted toward developing a structural approach for solving these issues to realize scaled NAND flash memory. Poly-Si has long been used as a floating gate in NAND flash memory owing to its favorable characteristics [7,8]. To enhance the property of a floating memory cell, we attempted to change the floating cell from Poly-Si to Poly-GaAs and reported our findings in a previous article [9]. GaAs is an attractive material owing to its electron speed, high charge trap density, and temperature immunity. However, its drawbacks are the dispersion phenomenon of arsenic at 600 ℃ and the large strain from the silicon substrate. Hence, we require an advanced material having a temperature endurance of greater than 700 ℃ and low silicon defect density. Gallium phosphide (GaP) has special properties such as a charge trap density of 10^{14}–10^{16} cm^{-3} measured using a current transient spectroscopy system [10], temperature immunity of greater than 750 ℃, and a mismatch density that is much lower than that of GaAs for the silicon-based material.

In this study, we evaluated a new material, namely polycrystalline gallium phosphide (Poly-GaP), at a low temperature. It is known that GaP provides excellent thermal endurability of greater than 750 ℃ and is highly compatible with CMOS. In addition, via C–V measurement, we discovered through intensive examination that Poly-GaP has a significant charge trap density that is equal to or greater than that of Poly-GaAs. With the expectation of higher trap densities in the vicinity of the interface between Poly-GaP and SiO_2 on a silicon substrate, the memory window of the III–V capacitor with a GaP floating gate was compared with that of a Poly-GaAs and Poly-Si floating gate [9] using C–V measurement. Thus, we confirmed the possibility of a candidate material for microscopic NAND flash memory.

2. Experimental details

To obtain a high-quality Poly-GaP layer, the main chamber was kept in an ultra-high vacuum at 3×10^{-10} Torr. The sample was loaded into the main chamber and a 0.5-μm-thick floating layer was grown at 1.82 Å/s, below 300 ℃, with an operation vacuum level of 3×10^{-8} Torr and a 1×10^{-5} Torr III–V (phosphorus or arsenic) beam source. SiO_2, as a block oxide, was deposited using a low-pressure chemical vapor deposition system. For the gate material, titanium (50 nm), as a barrier layer, and platinum (100 nm) were deposited by electron beam evaporation. For reference, three types of samples, namely Poly-GaAs, Poly-GaP, and Poly-Si, were planned and fabricated under the same geometric conditions to compare the characteristics of their memory window as a capacitor.

3. Results and discussion

3.1. Device Characteristics

To confirm the polycrystallinity of GaP, the fast Fourier transformation (FFT) analytic technique was adopted with a high-resolution transmission electron microscopy (TEM) image at a scale bar of 50 nm. The GaP material a columnar structure [10].

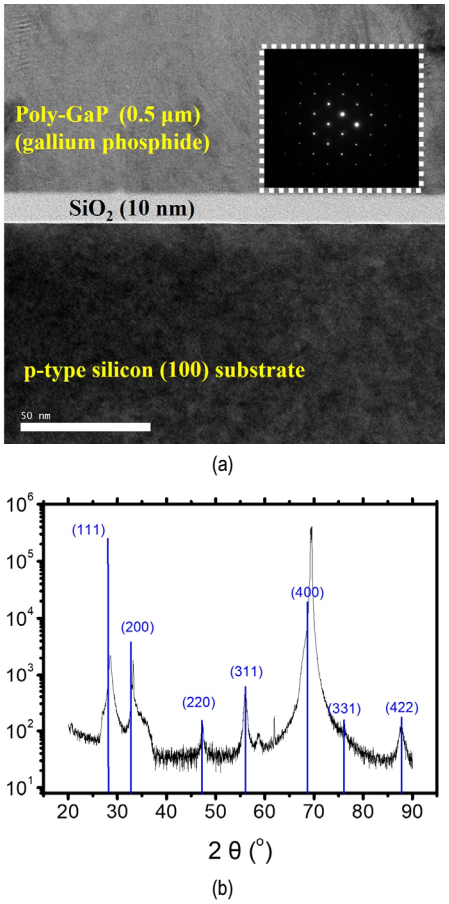

Figure 1. Cross-sectional TEM image of fabricated Poly-GaP device. (a) A P-type Si (100) wafer was prepared by pre-cleaning; then, thermal dry oxidation with a 10 nm thickness was performed at 900 ℃. A Poly-GaP layer was grown on SiO_2/p-type Si using a Riber Compact 21E solid source molecular beam epitaxy system. (b) The XRD pattern of the polycrystalline GaP layer is shown.

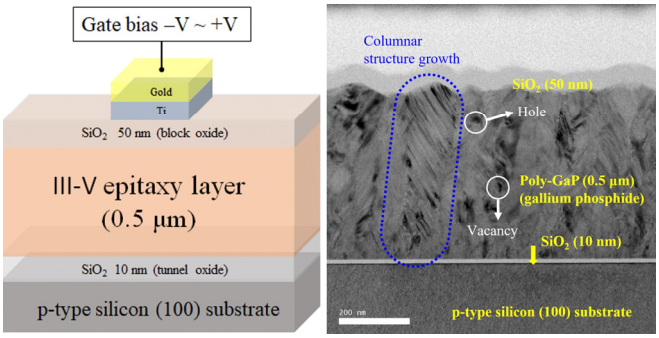

Figure 2. III-V memory structure using a Poly-GaP floating gate. Cross-sectional TEM image shows fabricated device. This structure consists of a metal gate, block oxide (50 nm), floating gate of Poly-GaP material (0.5 μm), and tunnel oxide (10 nm) on silicon substrate and the Poly-GaP layer has a columnar shape.

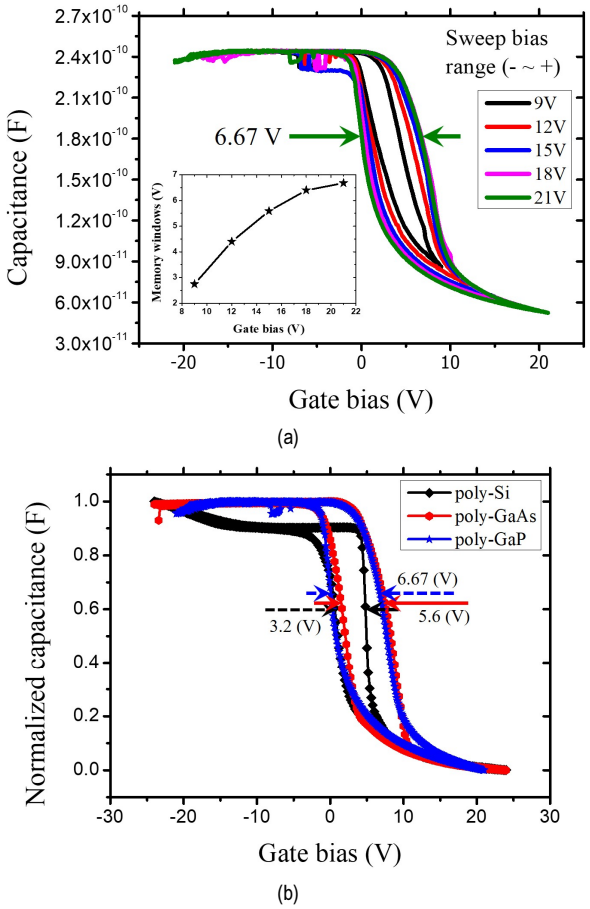

Figure 3. C-V characteristics of Poly-GaP, Poly-GaAs, and Poly-Si flash cells. (a) Average value of the memory window with 20 cell samples. (b) Shift of the flat band voltage (V_{fb}) with an applied sweep voltage from -24 to 24 V.

Figure 1(a) shows an FFT pattern of Poly-GaP on the grown SiO_2/Si substrate. A device with a Poly-GaP floating gate with a grain boundary was presented and compared with the Poly-GaAs and a Poly-Si floating gates [7]. Further, as shown in Fig. 1(b), all the peaks of GaP were assigned to the zinc blend phase of GaP (JCPDS data: 01-071-5973). Analysis of the FFT pattern and X-ray diffraction (XRD) data suggested polycrystalline growth on SiO_2 [11–13]. From these results, we confirmed that Poly-GaP was grown successfully.

Figure 2 shows a cross-sectional TEM image of the capacitor with floating Poly-GaP. As seen in this figure, large distortions were found, such as vacancies or holes in Poly-GaP. These defects can capture charges and act as charge storage sources. We concluded that electrons are stored in the interface of both the materials [14,15]. Figure 3 shows the C–V characteristics of those cells whose III–V floating gates consist of a polycrystalline state. The C–V measurement was conducted using an Agilent/HP 8110A pulse generator

Figure 3(a) shows various C–V hysteresis curves of the Poly-GaP samples. The sweep bias range is ±21 V. The hysteresis of the larger memory window increases with the sweep gate bias. As shown in the inset, the memory window may become saturated. The memory window is approximately 6.67 V at a gate bias of ±21 V. In the case of Fig. 3(b), we show the most stable memory window; while Poly-Si is saturated to 3.2 V at a sweep bias of ±14 V, Poly-GaAs shows 5.6 V at a bias of ±22 V and Poly-GaP shows 6.67 V at a bias of ±21 V.

From these results, we confirmed that the window margin of the Poly-GaP material is 2.1 times larger than that of Poly-Si and 1.2 times larger than that of Poly-GaAs. We used the average value of the memory window of 20 cell samples with a sweep voltage ranging from -24 to 24 V. Thus, we confirmed that more than 70% of the measured

cells have Poly-GaP at 6.67 V. Our structure is essential for the consideration of the block oxide (50 nm) because gate coupling is dependent on it. Further investigation is required for a capacitor using a III–V floating gate with a coupling ratio larger than 0.5 by applying a thinner block oxide (<10 nm).

4. Conclusions

In this paper, for the first time, we investigated how the memory window is related to the types of materials such as Poly-Si and Poly-GaAs in capacitors with Poly-GaP floating gates. Additionally, the memory window widths of III-Vs and Poly-Si are compared as a capacitor. The proposed Poly-GaP memory cells show a large memory window width of 6.67 V for the capacitor with a GaP floating gate, which is two times larger than that with a poly silicon floating gate. It has been confirmed that the window of the charge trap memory made using gallium phosphide exhibited better material characteristics, which led to significant improvement of the memory window. The proposed GaP growing method on silicon substrate is a very effective approach that results in better cell characteristics. A Poly-GaP is a good candidate material in nanoscale NAND flash memory due to the fact that it has resistant to high temperature and wider memory window.

Moreover, it is a more useful Nano technology because it is compatible with CMOS processes.

Acknowledgements

This research was supported by the Ministry of Trade, Industry & Energy (MOTIE (project number 20003808)) and Korea Semiconductor Research Consortium (KSRC) support program for the development of the future semiconductor device.

The author from KIST acknowledges partial support from the KIST institutional program.

References

[1] A. Goda and K. Parat, IEEE International Electron Devices Meeting (San Francisco, CA, USA, December 2012) pp. 2.1.1–2.1.4.
[2] K. Kim, VLSI-TSA (April 2008) pp. 5–9.
[3] Y. S. Kim, D. J. Lee, C. K. Lee, H. K. Choi, S. S. Kim, J. H. Song, D. H. Song, J. H. Choi, K. D. Suh, and C. Chung, IEEE International Reliability Physics Symposium (IRPS 2010) pp. 599–603.
[4] S. Seo, H. Kim, S. Park, S. Lee, S. Aritome, and S. Hong, IEEE International Reliability Physics Symposium (IRPS, Monterey, CA, USA, April 2011) pp. 6B.2.1–6B.2.4.
[5] S. Lee, IEEE International Memory Workshop (Milan, May 2012) pp. 1–4.
[6] R. Bez, E. Camerlenchi, A. Modelli, and A. Visconti, Proceedings of the IEEE (April 2003) pp. 489–502.
[7] T. K. Kim, S. Chang, and J. H. Choi, Solid-State Electron. 53, 792 (2009).
[8] T. Kamigaichi, F. Arai, H. Nitsuta, M. Endo, K. Nishihara, T. Murata, H. Takekida, T. Izumi, K. Uchida, T. Maruyama, L. Kawabata, Y. Suyama, A. Sato, K. Ueno, H. Takeshita, Y. Joko, S. Watanabe, Y. Liu, H. Meguro, A. Kajita, Y. Ozawa, T. Watanabe, S. Sato, H. Tomiie, Y. Kanamaru, R. Shoji, C. H. Lai, M. Nakamichi, K. Oowada, T. Ishigaki, G. Hemink, D. Dutta, Y. Dong, C. Chen, G. Liang, M. Higashitani, and J. Lutze, IEEE Electron Devices Meeting (San Francisco, CA, USA, December 2008), pp. 1–4.
[9] I. P. Roh, N. S. Kang, S. H. Shin, Y. T. Oh, K. B. Kim, J. D. Song, and Y. H. Song, Electron. Lett. 26, 963 (2016).
[10] H. Lee, S. H. Park, Y. K. Park, S. J. Kim, B. H. Kim, J. Lee, and S. C. Jung, Int. J. Photoenergy 2014, 7 (2014).
[11] B. P. Wang, Z. C. Zhang, and N. Zhang, Solid State Sci. 12, 1188 (2010).
[12] K. Park, J. A. Lee, H. S. Im, C. S. Jung, H. S. Kim, J. Park, and C. L. Lee, Nano Lett. 14, 5912 (2014).
[13] C. R. Helms and B. E. Deal, The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface 2 (Plenum Press, New York, 1993) 235–256.
[14] S. Das, S. K. Chaudhuri, and K. C. Mandal, ECS J. Solid State Sci. Technol. 5, 3059 (2016).
[15] D. S. McGregor, R. A. Rojeski, G. F. Knoll, F. L. Terry Jr, J. East, and Y. Eisen, J. Appl. Phys. 75, 7910 (1994).