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Shift of switching threshold in low-dimensional semiconductor-based complementary inverters via inkjet printing

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Abstract

MoS_2 crystals grown by chemical vapor deposition are suited for realization of practical 2D semiconductor-based electronics. In order to construct complementary circuits with n-type MoS_2, another p-type semiconductor, whose performance can be adjusted corresponding to that of MoS_2 in the limited chip area, has to be sought. Herein, we present a method for tuning switching threshold voltages of complementary inverters simply via inkjet printing without changing their channel dimensions. Random networks of inkjet printed single-walled carbon nanotubes are formed as p-channels beside MoS_2, and their density and thickness are controlled by varying the number of printed layers. As a result, p-type transistor characteristics as well as inverter characteristics are facilely tuned only by varying the number of printed layers.

Supplementary material for this article is available online

Keywords: printed electronics, tunable switching threshold, molybdenum disulfide (MoS_2), carbon nanotube (CNT)

(Some figures may appear in colour only in the online journal)

1. Introduction

A monolayer MoS_2 has been considered to be one of the most promising and representative two-dimensional (2D) semiconductors due to its superior mechanical, optical and electrical properties [1, 2]. High quality MoS_2 crystals with relatively large grain sizes can be synthesized by a chemical vapor deposition (CVD) method [3, 4] that is widely employed for deposition of various functional materials in real industrial applications. In order to implement integrated complementary circuits (the most dominant technology for constructing integrated circuits due to its low power consumption and high noise immunity) by employing CVD grown MoS_2, p-type semiconducting channels have to be formed selectively right next to the n-type MoS_2 channels [5]. In addition, performances of n- and p-type field-effect transistors (FETs) based on those channels have to be comparable for balanced circuit operations.

When n- and p-channel materials with different performances are selected to construct complementary circuits, FET characteristics are typically tuned by enlarging the channel width of the weaker side to compensate the difference in FET characteristics while the channel lengths are fixed [6]. However, it is quite challenging to form semiconducting channels next to each other with desired dimensions especially when randomly distributed CVD grown large crystals such as MoS_2

[5] These authors contributed equally to this work.

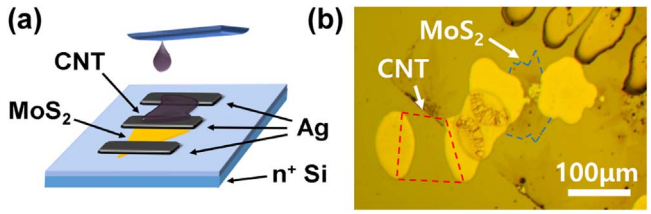

Figure 1. (a) Schematic of a complementary inverter based on CVD grown MoS_2 and inkjet printed SWCNTs. (b) Optical image of the complementary inverter.

are packed without leaving enough space. Therefore, it is necessary to find an area-effective method for tuning circuit characteristics under such space limitations.

In this work, we demonstrated a method for tuning switching threshold voltages (V_M) of complementary inverters via inkjet printing without changing channel length and width. The controllable V_M in inverter circuits have been previously reported by using rather complex methods such as a gate dielectric of mixed self-assembled monolayer [7], a laser annealing [8], and additional floating gates [9]. We employed single-walled carbon nanotubes (SWCNTs) as a p-type counter part of n-type MoS_2 and formed p-channels only in the desired area next to the MoS_2 FET by using a facile and scalable inkjet printing method. SWCNTs are suitable p-channel materials not only due to their wide use in printed electronics, [10–13] but also due to their tuning capability in FET characteristics depending on their network density and thickness [14, 15]. By simply varying the number of printed SWCNT layers (which is defined by the number of printing 'passes'), p-FET characteristics were modulated accordingly, leading to the modifications in inverter characteristics.

2. Device fabrication and characterizations

Figure 1(a) shows a schematic of the complementary inverter consisting of a MoS_2 n-FET and a SWCNT p-FET. Heavily doped Si served as a common gate electrode for both FETs. A gate dielectric layer of HfO_2 was deposited by atomic layer deposition (Nano-ALD2000, IPS) without removing a native oxide layer on the Si substrate. A MoS_2 monolayer was synthesized on another SiO_2/Si substrate by CVD, then transferred onto the HfO_2/Si substrate as described in previously reported work [5]. Top and bottom contact structures were employed for MoS_2 and SWCNT FETs, respectively. Ag nanoparticle-based ink (Sigma-Aldrich) was inkjet printed (DMP-2850, Fujifilm) as source/drain (S/D) electrodes for both MoS_2 and SWCNT FETs, followed by annealing at 150 °C for 10 min on a hotplate. Then, the surface of the substrate was treated with UV/O_3 (PSDP-UV4, Novascan) for 5.5 min to promote wetting of SWCNT ink. SWCNTs (semiconducting purity > 99%, Nanointegris) dispersed in 1-cyclohexyl-2-pyrrolidone (Sigma-Aldrich) at a concentration of 0.1 mg ml^{-1} were inkjet printed to form p-channel areas between preformed S/D electrodes. The diameter of SWCNTs is in the range of 1.2—1.7 nm (from the

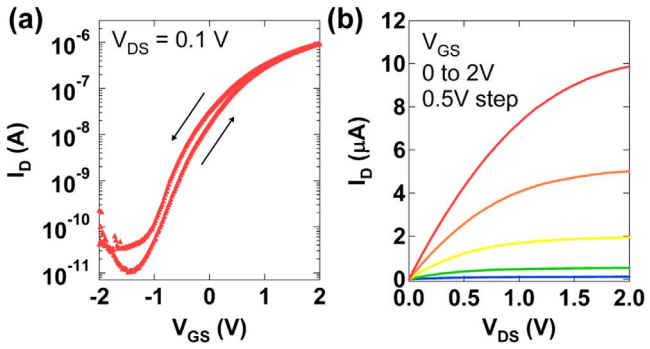

Figure 2. (a) Transfer characteristics (I_D–V_{GS}) and (b) output characteristics (I_D–V_{DS}) of the MoS_2 FET.

information provided by the manufacturer). The substrate was baked on a hot plate at 200 °C for 30 min to remove residual solvents. SWCNT printing and baking steps were repeated after measurement of device characteristics at each SWCNT layer number. Figure 1(b) shows an optical image of the complementary inverter.

The cartridges employed in Ag and SWCNT printing were designed for 10 pL drop volume. The drop spacing was chosen to be 40 μm for both Ag and SWCNT printing. The thickness of the gate dielectric layer was measured using ellipsometry (FS-XY150, Film Sense). Atomic force microscope (AFM) scans were acquired using a scanning probe microscope (XE7, Park Systems) with a silicon cantilever (PPP-NCHR, Nanosensors) of spring constant 42 N m^{-1} and tip radius $r < 10$ nm in tapping mode. The capacitance value of the gate dielectric layer was measured using a semiconductor device analyzer (B1500A, Keysight Technologies). FET and inverter characteristics were measured using a semiconductor parameter analyzer (Agilent 4155C) under ambient conditions.

3. Results and discussion

2D crystalline MoS_2 monolayers form electron current pathways for n-FET, while random networks composed of one-dimensional SWCNTs form hole current pathways for p-FET in this work. Individual FET characteristics of n- and p-FETs were analyzed before measuring inverter characteristics. A capacitor consisting of Ag/HfO_2/native oxide/n^+ Si was fabricated and characterized along with the devices to know characteristics of the gate dielectric layer. The thicknesses of the native oxide and HfO_2 were measured to be 1.9 nm and 19.6 nm, respectively. The areal capacitance of the gate dielectric layer was measured to be 308 nF cm^{-2}. The leakage current densities of the capacitor are shown in figure S1 (available online at stacks.iop.org/NANO/33/305203/mmedia) (supplementary information).

Figures 2(a) and (b) show transfer (I_D–V_{GS}) and output (I_D–V_{DS}) characteristics of the MoS_2 n-FET, respectively. The MoS_2 FET exhibits linear field-effect mobility (μ) of 9.2 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} of 9.1 × 10^4, subthreshold slop (SS) of 257 mV/dec, and threshold voltage (V_{Th}) of 0.83 V at V_{DS} = 0.1

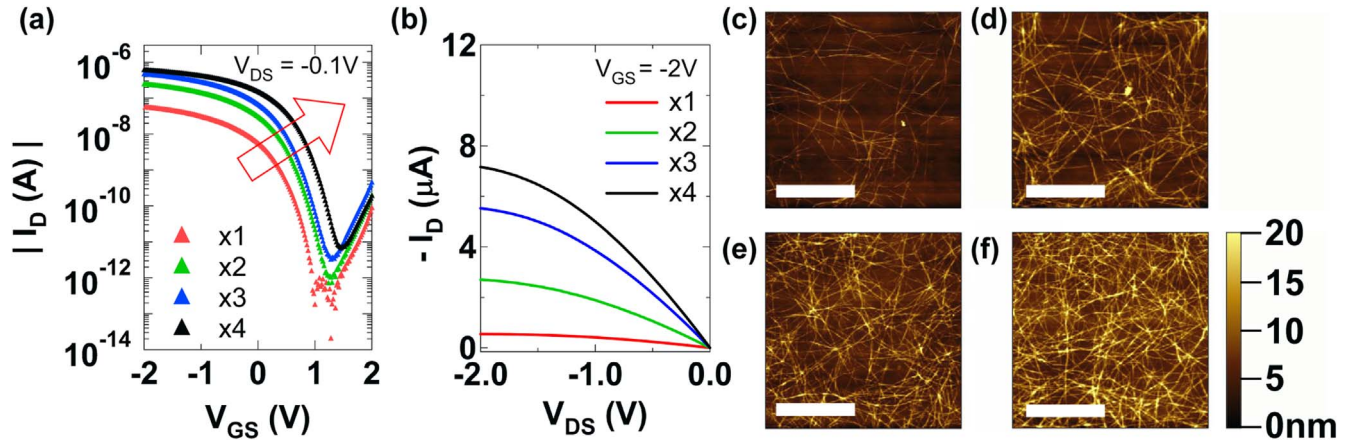

Figure 3. (a) Transfer characteristics (I_D–V_{GS}) and (b) output characteristics (I_D–V_{DS} at $V_{GS} = -2$ V) of the SWCNT FET with different numbers of printed layers. AFM images in channel areas of the SWCNT FETs when the printed layer numbers were (c) one, (d) two, (e) three, and (f) four. The scale bars are 2 μm. The color scale bar in (f) applies to all AFM images.

V. V_{Th} was extracted by using the linear extrapolation method at the maximum transconductance.

For SWCNT FETs, currents flow through percolating SWCNT random networks. Therefore, larger hole currents flow above the percolation threshold as the SWCNT networks become denser and thicker due to the formation of more current pathways in the case of SWCNT FETs [16, 17]. Density and thickness of SWCNT channels can be facilely adjusted by varying the number of printed SWCNT layers in the same channel area. As a result, current levels of the SWCNT p-FET can be tuned by varying the number of printed SWCNT layers without changing channel dimensions. Figure 3(a) shows transfer characteristics of the SWCNT FET at different numbers of printed layers. The curves shift toward the upper right direction as the number of printed layers increases as indicated by an arrow in figure 3(a). The hysteresis characteristics of the same SWCNT FET are shown in figure S2 (supplementary information). Device parameters (μ, I_{on}/I_{off}, SS, V_{Th}) at $V_{DS} = -0.1$ V for each SWCNT layer number were listed in table 1. In particular, μ increases and V_{Th} shifts to the more positive direction as the number of printed layers increases. Consistent trends were clearly observed in the independently conducted experiment where 16 p-FETs per each printing number were fabricated on the same substrate and characterized (Figure S3 and table S1 in supplementary information). As a result, p-FET $|I_D|$, which is a function of both V_{Th} and μ, increases as the number of printed layers increases. Figure 3(b) compares the magnitude of I_D at the fixed V_{GS} of -2 V with different numbers of printed SWCNT layers, and shows an obvious increase in the magnitude of I_D as the number of printed layers increases. Output characteristics of the same SWCNT FET at other V_{GS} values are displayed in figure S4 (supplementary information).

Figures 3(c)–(f) show AFM images of the p-FET channel areas at different numbers of printed layers. It is clearly observed that the density and thickness of SWCNT random networks increase as the number of printed SWCNT layers increases. Magnified AFM images (1 μm by 1 μm) and their line profiles are presented in Figures S5. The average linear densities of SWCNTs were measured to be 8.1, 12.8, 15.4, and 21.4 tubes/μm at the printed layer number of 1, 2, 3, and 4, respectively (from figure S5 in supplementary information). The root mean square roughness values were measured to be 1.7, 2.4, 2.7, and 3.5 nm at the printed layer number of 1, 2, 3, and 4, respectively (from figure S5 in supplementary information).

Table 1. Device parameters of the SWCNT FET with different numbers of printed layers.

# of printed layers	mobility ($cm^2\ V^{-1}\ s^{-1}$)	I_{on}/I_{off}	SS (mV/dec)	V_{Th} (V)
1	0.6	3.9×10^5	96.3	−0.20
2	2.2	3.5×10^5	133.3	0.08
3	3.9	1.4×10^5	162.6	0.21
4	4.8	9.1×10^4	165.7	0.52

Characteristics of a complementary inverter, which consists of one n-FET and one p-FET with shared drain electrodes, can be tuned by adjusting individual n- and p-FET characteristics. In order to demonstrate tunable inverter characteristics by varying the number of SWCNT layers via inkjet printing, drain electrodes of n- and p-FETs were connected together as a V_{OUT} terminal to construct a complementary inverter as shown in figure 1 and figure 4(a). Source electrodes of n- and p-FETs were connected to GND and V_{DD}, respectively. V_{IN} was applied to the common bottom gate. Figure 4(b) shows voltage transfer characteristics (VTC) of the inverter with different numbers of printed SWCNT layers. The inverter exhibits a rail-to-rail swing at a low operating voltage of 2 V. VTC shifts toward the positive voltage direction as the number of printed SWCNT layers increases. Therefore, V_M, which is defined as the voltage where $V_{IN} = V_{OUT}$, increases as the number of printed SWCNT layers increases as shown in figure 4(c). In consequence, we managed to place V_M (of the imbalanced inverter) near $V_{DD}/2$ by simply varying the number of SWCNT layers without sacrificing areas.

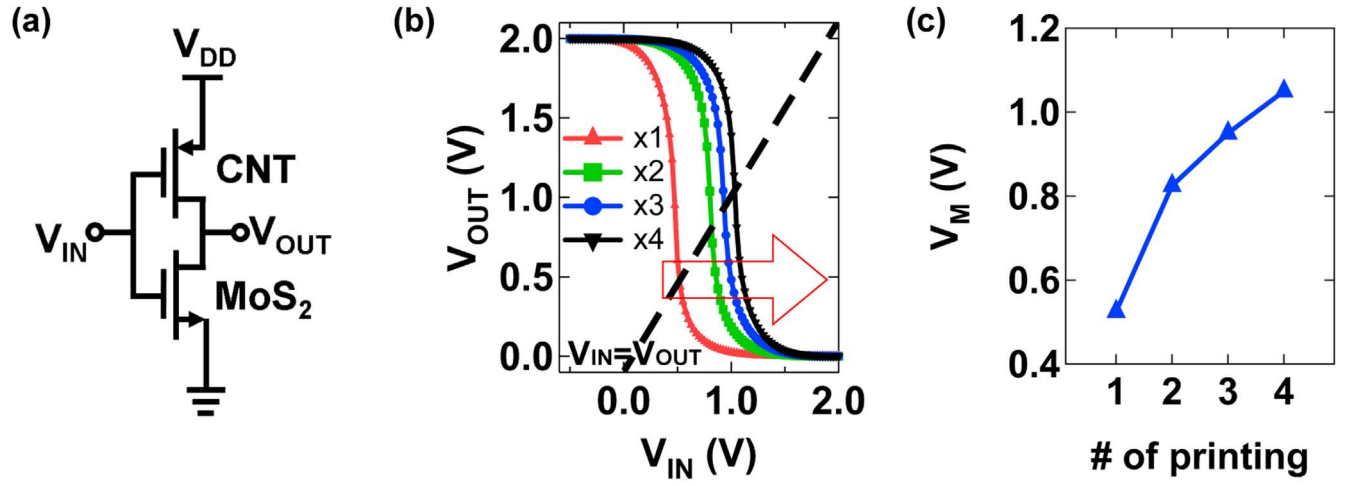

Figure 4. (a) A circuit diagram of the complementary inverter. (b) Voltage transfer characteristics with different numbers of printed SWCNT layers at $V_{DD} = 2$ V. (c) Switching threshold voltages (V_M) of the inverter as a function of the number of printed SWCNT layers.

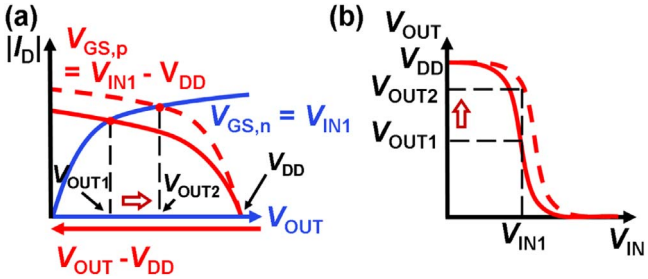

Figure 5. Schematic illustrations showing (a) where operating voltages of the inverter are determined when p-FET current changes from the red solid line to the red dashed line while n-FET current (blue solid line) remains the same, and (b) corresponding V_{OUT} positions in VTC.

In order to demonstrate the reproducibility of V_M tuning in inverter characteristics, three additional complementary inverters were fabricated on the same substrate and characterized (Figure S6, supplementary information).

Figure 5(a) graphically illustrates where operating voltages of the inverter are determined by using the load-line analysis. The position of V_{OUT} is determined where the superimposed output characteristics of n- and p-FETs at a fixed V_{IN} ($V_{GS,n} = V_{IN1}$ for n-FET and $V_{GS,p} = V_{IN1} - V_{DD}$ for p-FET) intersect. The transition of V_{OUT} between HIGH and LOW occurs in the middle range of V_{IN} where both n- and p-FETs are turned on. In such V_{IN} range, $|I_D|$ of p-FET at the same V_{IN} increases as the number of printed SWCNT layers increases (from the red solid curve to the red dashed curve in figure 5(a)), whereas n-FET I_D at the same V_{IN} remains the same (the blue solid curve in figure 5(a)) since no changes were made to the n-FET. Therefore, the intersection point of n- and p-FET curves shifts toward higher V_{OUT}. In the other V_{IN} ranges where one of the FETs is turned off, the intersection point is located near V_{DD} or 0 (whether the number of printed SWCNT layers increase or not), showing HIGH and LOW V_{OUT}, respectively. Corresponding VTCs for the increased number of SWCNT layers are shown in figure 5(b). VTC shifts toward the positive voltage direction as the number of printed SWCNT layers increases (from the red solid curve to the red dashed curve in figure 5(b)) because V_{OUT} becomes higher at the same V_{IN} as shown in figure 5(a). The direction of VTC shift would be opposite if the current of the n-FET was tuned to be larger while the current of the p-FET remains the same.

4. Conclusion

The tunability of the position of V_M in the complementary inverter was demonstrated via inkjet printing. Current levels of the SWCNT p-FET increased only by increasing the number of printed SWCNT layers without sacrificing limited areas between CVD grown MoS_2 flakes rather than enlarging the channel width. As a result of varying only p-FET characteristics via inkjet printing, VTC of the complementary inverter, which consisted of the CVD grown MoS_2 n-FET and the inkjet printed SWCNT p-FET, was shifted toward the positive voltage direction as the number of printed SWCNT layers increased. This result suggests that inkjet printing could be an effective method for tuning characteristics of complementary circuits based on low-dimensional semiconductors where the performance matching between n- and p-FETs is desired for balanced operations.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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