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Effect of P+ Source Pattern in 4H-SiC Trench-Gate MOSFETs on Low Specific On-Resistance

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Abstract: Novel 1.7-kV 4H-SiC trench-gate MOSFETs (TMOSFETs) with a grid pattern and a smaller specific on-resistance are proposed and demonstrated via numerical simulations. The proposed TMOSFETs provide a reduced cell pitch compared with TMOSFETs with square and stripe patterns. Although TMOSFETs with a grid pattern reduce the channel area by approximately 10%, the cell density is increased by approximately 35%. Consequently, the specific on-resistance of the grid pattern is less than that of the square and stripe patterns. The forward blocking characteristics of the grid pattern are increased by the reduced impact ionization rate at the P/N junction. As a result, the figure-of-merit (FOM) of the grid pattern is increased by approximately 33%.

Keywords: silicon carbide; 4H-SiC; trench-gate MOSFETs; 3D-simulation; design consideration; specific on-resistance; forward blocking; figure-of-merit

1. Introduction

Compared with silicon, the high critical electric field of silicon carbide (SiC) allows a low on-resistance to fabricate a thin epitaxial layer with a high doping concentration for a specified breakdown voltage. SiC MOSFETs with low on-resistance are useful in high-power and high-switching-speed applications such as DC-to-DC converters, motor drives, and electric vehicles. Researchers have attempted to minimize specific on-resistance ($R_{on,sp}$). With regard to device structure, trench-gate MOSFETs (TMOSFETs) have great potential for low on-resistance due to the absence of a JFET region and a small cell-pitch compared with planar gate MOSFETs [1–4]. Advanced process technologies including post-oxidation annealing in nitric oxide (NO) [5–8], self-aligned ohmic contact with two-step rapid thermal annealing (RTA) [8–11], and ion implantation at high temperatures [12,13] provide high-quality SiO_2/4H-SiC interfaces with low contact resistance. A prevalent channel self-alignment method increases current density [14–16]. However, in existing photolithography areas, critical limitations of smaller cell pitches result from critical dimension control [17,18]. The pattern mask for the P+ source diode uses square and stripe patterns. The square pattern formed by etching all edge directions must be enlarged more than the stripe pattern to prevent a distorted pattern [19]. As the specific on-resistance is proportional to the cell pitch, a P+ source with a square pattern produces a high on-resistance.

In this study, a novel device architecture with a grid pattern is proposed to minimize the cell pitch. Unlike a conventional P+ source with stripe and square patterns, the proposed P+ source pattern architecture was fabricated beside the trench gate. Although the reduced channel area increases on-resistance, the proposed device provides a small cell pitch. Thus, the P+ source grid TMOSFETs provide lower on-resistance than both prevalent devices. In addition, this structure can increase the breakdown voltage about 11% more than the conventional structures due to a reduced 3-D effect at the P+/N+ junction and enhance the third-quadrant characteristics by increasing the P+ source areas.

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2. Device Modeling and Simulation Methodology

Figure 1a–c show the 3-D structures of 1.7-kV conventional SiC TMOSFETs with a P+ source with square and stripe patterns and the proposed TMOSFETs with a P+ source with a grid pattern, respectively. The top view of TMOSFETs with a square-pattern P+ source is shown in Figure 1d. The square-type P+ source is placed intermittently around the N+ source. The square pattern size was set to 2 μm × 2 μm to consider alignment tolerance; thus, the half-cell pitch width was set to 2.3 μm. Figure 1e shows the top view of TMOSFETs with a stripe pattern P+ source and a half-cell pitch width of 2.0 μm. The stripe pattern is easily formed for two-direction patterning, allowing a smaller cell pitch than with a square pattern. The half-cell pitch width of TMOSFETs with a grid-pattern P+ source was set to 1.5 μm, with a trench width (W_{TRN}) of 1.0 μm, N+ source width (W_{NP}) of 1.0 μm, and P+ source width (W_{PP}) of 1.0 μm, as shown in Figure 1f. A P+ source with a grid pattern was placed next to the trench gate. Although the channel width was reduced, this pattern enabled a reduced cell-pitch. To analyze the effect of the grid pattern on electrical characteristics, a P+ source length (L_{PP}) was divided into five cases from 0.5 μm to 2.5 μm in the half-cell pitch in the y-direction.

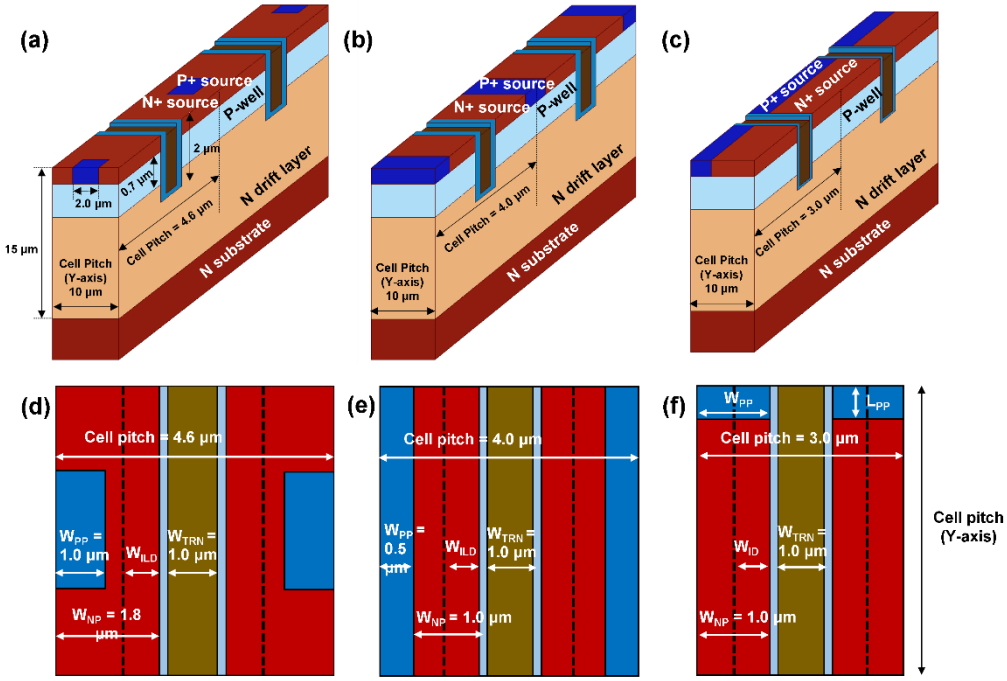

Figure 1. (**a**) Conventional trench-gate MOSFETs with P+ source with square pattern, (**b**) stripe pattern, and (**c**) grid pattern. Top view of TMOSFETs with P+ source with (**d**) square pattern, (**e**) stripe pattern, and (**f**) grid pattern.

For TMOSFETs with a 1.7-kV voltage rating, an N-type doping concentration of 6×10^{15} cm^{-3} with a drift thickness of 15 μm was designed using Sentaurus TCAD process tools. The detailed structural parameters presented in Table 1. TMOSFETs structural parameters were considered by experimental reference data [20,21]. Grid-pattern TMOSFETs of the P-well, N+ source, P+ source, and trench gate were designed using the fabrication sequence shown in Figure 2. The fabrication processes of the proposed TMOSFETs with P+ source grid pattern is the same as those of the conventional TMOSFETs with P+ source square and stripe patterns except photo-patterning of P+ source. The electrical characteristics of TMOSFETs with P+ source patterns were compared using the Sentaurus device. All simulations of electrical characteristics used the Lombardi model for carrier–carrier scattering by acoustic surface phonons and surface roughness. Shockley–Read–Hall (SRH) and an Auger were used in the generation-recombination process [22]. For the breakdown simula-

tion, the van Overstraeten model was used for the avalanche generation model [22,23]. The breakdown voltage was determined when the current reached 1 μA.

Table 1. Device structural parameters.

Parameter	Value	Unit
Thickness of drift layer	15	μm
Doping concentration of drift layer	6×10^{15}	cm^{-3}
Trench depth and width	2, 1	μm
Doping concentration of P base	2×10^{17}	cm^{-3}
Channel length	0.7	μm
Gate oxide thickness	50	nm
Width of inter layer dielectric (ILD)	0.5	μm
Half-width of cell pitch (y-axis)	5	μm
Half P+ source size (square pattern)	1×2	μm
Half P+ source size (stripe pattern)	0.5×5	μm
Half-width of cell pitch (square pattern)	2.3	μm
Half-width of cell pitch (stripe pattern)	2.0	μm
Half-width of cell pitch (grid pattern)	1.5	μm
Half-width of P+ source (grid pattern)	1.5	μm
Half-length of P+ source (grid pattern)	0.5–2.5 (+0.5)	μm

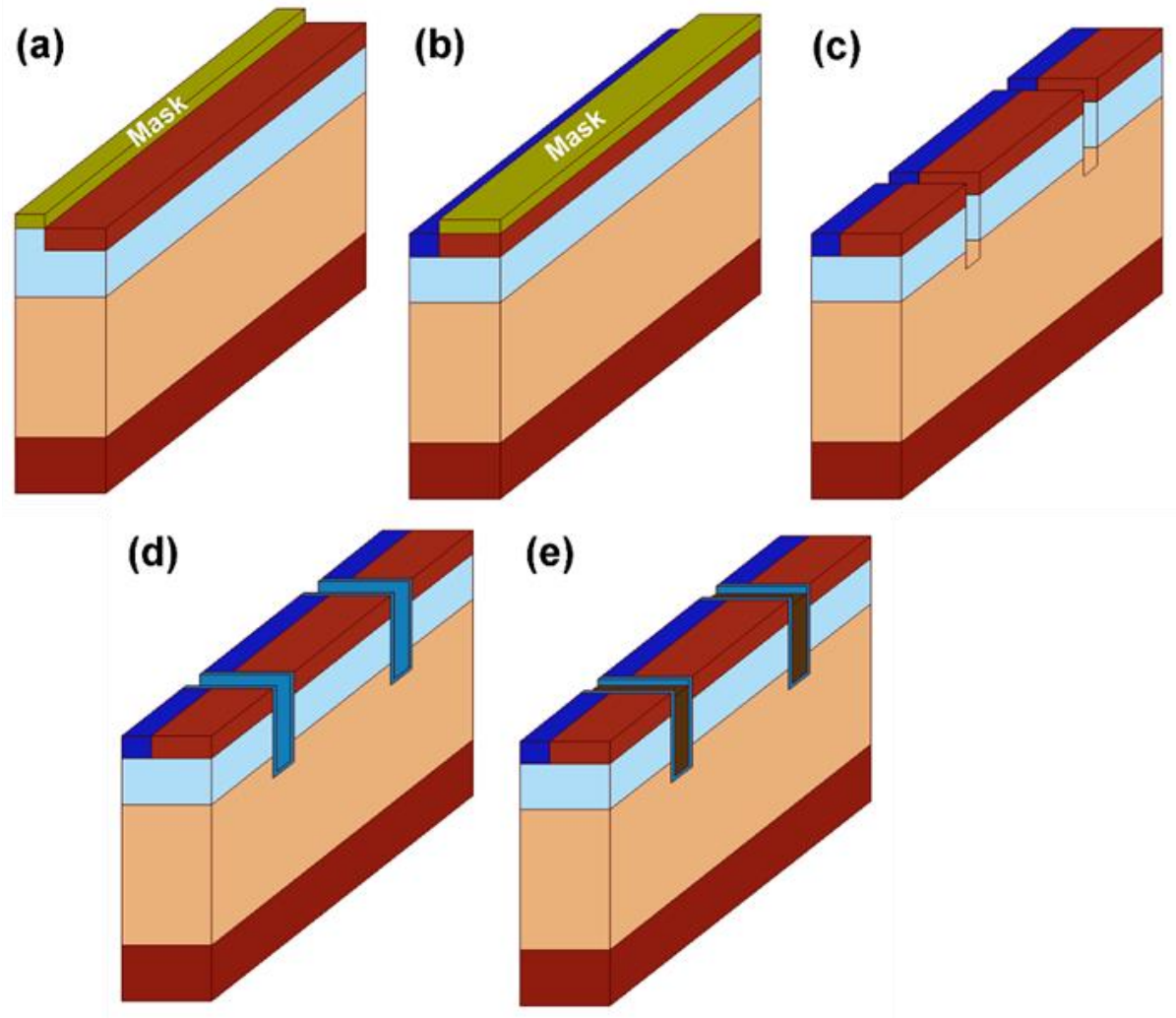

Figure 2. Outline of grid P+ source TMOSFET fabrication sequence: (**a**) implant N+ source; (**b**) implant P+ source; (**c**) etch trenches; (**d**) gate oxidation; (**e**) deposit polysilicon gates.

3. Results and Discussion

The output characteristics of conventional TMOSFETs with square and stripe patterns are compared with those with a grid P+ source at V_{gs} = 9 and 20 V and V_{ds} = 10 V in Figure 3. A grid pattern with a half-cell pitch of 1.5 µm provides a larger current than a square pattern with a half-cell pitch of 2.3 µm and a stripe pattern with a half-cell pitch of 2.0 µm. The difference in $R_{on,sp}$ originates from the cell pitch. Thus, the $R_{on,sp}$ of a grid pattern with a P+ source length (L_{PP}) of 0.5 µm is less than the $R_{on,sp}$ with a square pattern or stripe pattern, approximately 4.5% and 2.4% less, respectively.

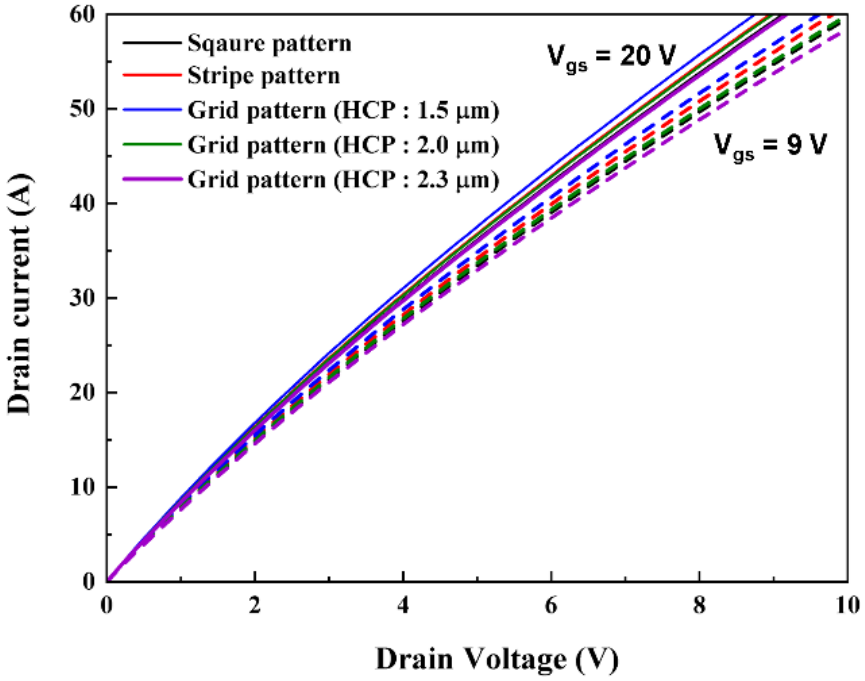

Figure 3. Output characteristics of TMOSFETs with square, stripe, and grid pattern.

Figure 4a shows the output characteristics of grid P+ source TMOSFETs with different L_{PP} at V_{gs} = 9 and 20 V and V_{ds} = 10 V. Maintaining a cell-pitch of 3.0 µm including the trench width, the N+ source width, P+ source width, and L_{pp} values of 0.5 to 2.5 µm with 0.5 µm steps, respectively, were used to examine the impact of L_{pp} on the specific on-resistance ($R_{on,sp}$). As L_{PP} increased, the reduction in channel area produced an increase in $R_{on,sp}$. Figure 4b shows the measured $R_{on,sp}$ with different half-cell pitches for the grid pattern and different P+ source lengths. As expected, a smaller cell pitch resulted in a lower $R_{on,sp}$. With a cell pitch of 3.0 µm, TMOSFETs with a grid pattern produce a lower $R_{on,sp}$ than a square pattern for all L_{pp} values. A grid pattern with L_{pp} = 2.5 µm reduced the channel area approximately 50%; with a cell pitch of 3.0 µm, the channel area was reduced approximately 35%. Although the percentage decrease in the channel area was larger than the percentage decrease in cell pitch, $R_{on,sp}$ for the grid pattern was less than that for the square pattern because the effect of the cell pitch was dominant. Compared with a stripe pattern, TMOSFETs with a grid pattern have a lower $R_{on,sp}$ except with an L_{pp} of 2.5 µm. Thus, cell pitch is critical for determining the specific on-resistance. The grid pattern TMOSFEFs with the cell-pitch of 4.0 µm and 4.6 µm were fabricated to investigate the influence of the reduced channel areas. Maintaining the cell-pitch of 4.0 µm or 4.6 µm, the $R_{on,sp}$ of grid pattern TMOSFETs compared to the $R_{on,sp}$ of stripe pattern TMOSFETs or the $R_{on,sp}$ of square pattern TMOSFETs, respectively. As a results, the stripe pattern or the square pattern have a lower $R_{on,sp}$ than the grid pattern in the same cell-pitch because of the effect of the reduced channel areas in Figure 4b.

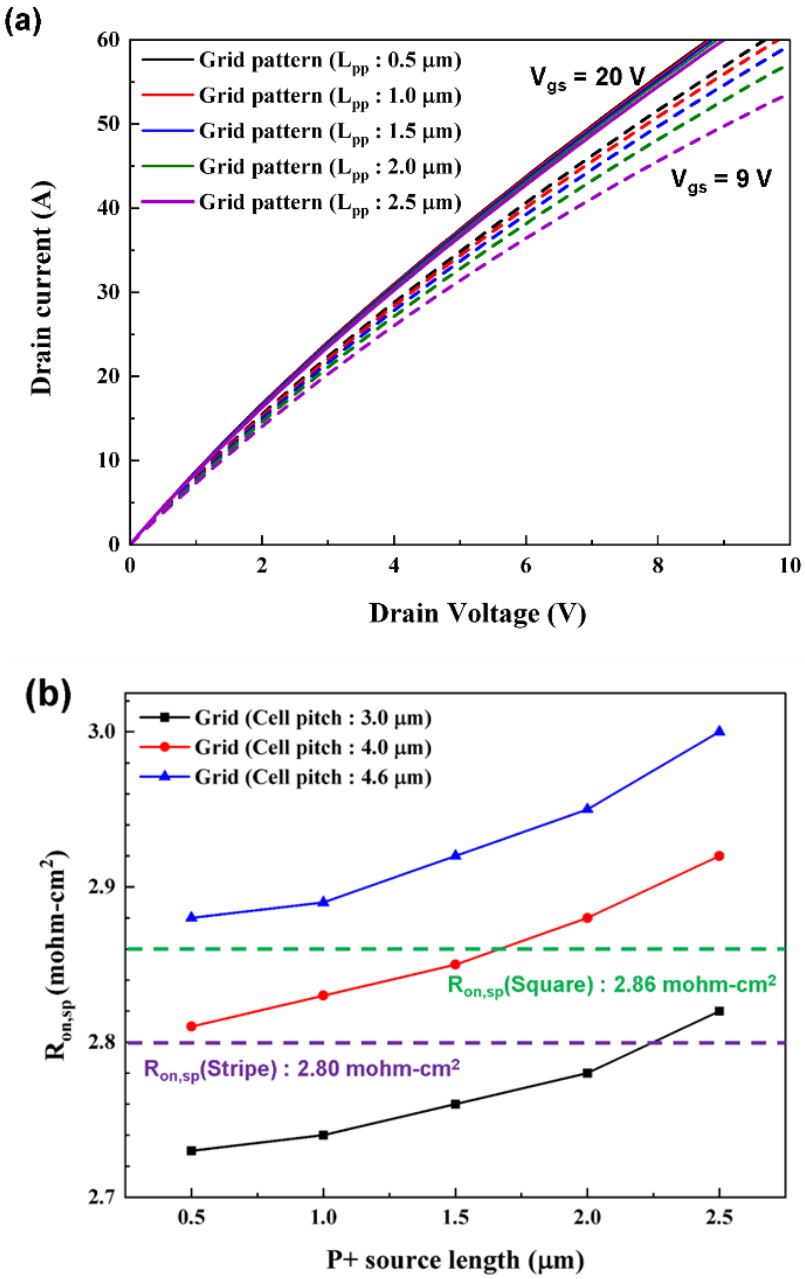

Figure 4. (**a**) Output characteristics of grid pattern with L_{pp} of 0.5 to 2.5 μm with 0.5 μm steps; (**b**) specific on-resistance with square, stripe, and grid patterns with cell pitches of 3.0 μm, 4.0 μm, and 4.6 μm.

Figure 5a shows the forward blocking behaviors of all simulated TMOSFETs with stripe, square, and grid patterns with different cell pitches and L_{PP} = 0.5 μm. The grid and stripe patterns produced a higher forward blocking voltage than the square pattern. In the TMOSFETs with a square pattern, a high impact ionization rate was observed at the P+/N+ junction at all edges of the square, and each point in the square pattern produced an increase in the electric-field stress, leading to a reduced breakdown voltage. To examine the impact of L_{PP} on forward blocking characteristics, L_{PP} of 0.5 μm, 1.0 μm, 1.5 μm, 2.0 μm, and 2.5 μm were designed to maintain the cell pitch. The role of the P+ source is to restrain a punch-through across the junction formed between the P-well and the N-drift region in forward blocking conditions [4]. This is not critical in deciding the blocking voltage in avalanche breakdown conditions; thus, high breakdown voltages remained regardless of the L_{PP}, as shown in Figure 5b.

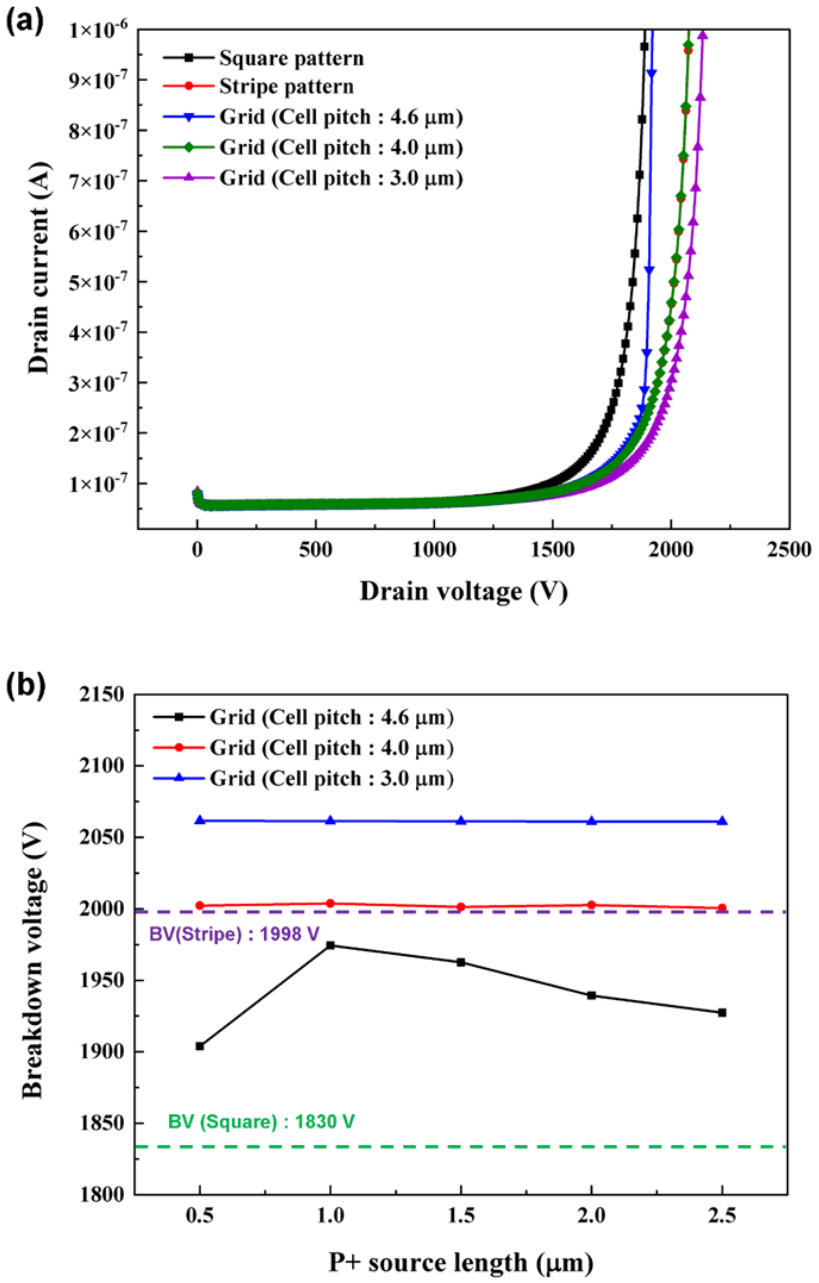

Figure 5. (**a**) Forward blocking behaviors of square, stripe, and grid patterns with cell pitches of 3.0 μm, 4.0 μm, and 4.6 μm; (**b**) breakdown voltage of grid pattern with cell pitches of 3.0 μm, 4.0 μm, and 4.6 μm, and L_{pp} of 0.5~2.5 μm.

The equivalent circuit for the TMOSFETs with an integral p-body diode is shown in Figure 6a. To examine the impact of P+ source areas on the third-quadrant characteristics, the grid P+ source TMOSFETs with different L_{PP} are compared in Figure 6b. As expected, an increase in L_{PP} produces an increase in current density through the body diode in the third quadrant. Figure 6c shows the third-quadrant behaviors of TMOSFETs with square, stripe, and grid patterns and L_{pp} of 0.5 μm, 1.5 μm, and 2.5 μm. A shorter L_{PP} (0.5 μm) in the grid TMOSFETs produces smaller quadrant behaviors than with conventional square and stripe TMOSFETs due to the small P+ source areas. However, a longer L_{PP} (1.5 μm) in the grid TMOSFETs produces a larger current density than in the square p-body TMOSFETs due to the larger p-body area. In addition, all L_{pp} values produce smaller quadrant current than with the stripe p-body TMOSFETs.

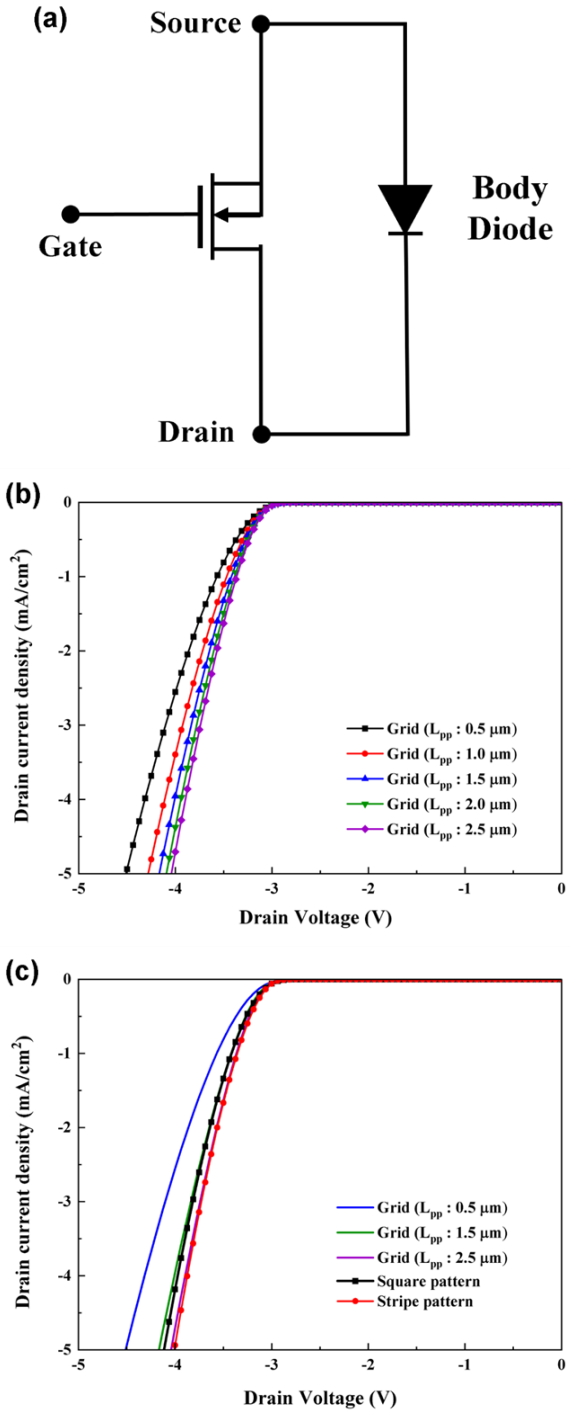

Figure 6. (**a**) Equivalent circuit for MOSFETs with body diode; (**b**) third-quadrant behaviors for grid pattern with L_{pp} of 0.5~2.5 μm; (**c**) third-quadrant behaviors of square, stripe, and grid pattern with L_{pp} of 0.5 μm, 1.5 μm, and 2.5 μm.

The static characteristics of TMOSFETs with square, stripe, and grid patterns and all simulated results for $R_{on,sp}$, forward blocking behavior (BV), and figure-of-merit (FOM, $BV^2/R_{on,sp}$) are compared in Table 2. Cell pitch (CP) is the most critical factor affecting $R_{on,sp}$. The smaller cell pitch of the TMOSFETs with a grid pattern produces a lower $R_{on,sp}$. For the same cell pitch, the channel area has a greater influence on $R_{on,sp}$. The P+ source for the stripe and grid patterns is influenced by greater forward blocking characteristics than the P+ source for the square pattern.

Table 2. Summary of device structures and static characteristics.

Device Structure	Simulation Results		
	Specific On-Resistance ($R_{on,sp}$) [mOhm-cm^2]	**Forward Blocking (BV) [V]**	**Figure-of-Merit (FOM) [MW/cm^2]**
Square pattern (CP = 4.6 μm)	2.86	1830	1172
Stripe pattern (CP = 4.0 μm)	2.80	1998	1426
Grid pattern (CP = 3.0 μm, L_{pp} = 0.5 μm)	2.73	2061	1556
Grid pattern (CP = 3.0 μm, L_{pp} = 1.0 μm)	2.74	2061	1549
Grid pattern (CP = 3.0 μm, L_{pp} = 1.5 μm)	2.76	2061	1539
Grid pattern (CP = 3.0 μm, L_{pp} = 2.0 μm)	2.78	2061	1526
Grid pattern (CP = 3.0 μm, L_{pp} = 2.5 μm)	2.82	2061	1508
Grid pattern (CP = 4.0 μm, L_{pp} = 0.5 μm)	2.81	2002	1426
Grid pattern (CP = 4.0 μm, L_{pp} = 1.0 μm)	2.83	2003	1420
Grid pattern (CP = 4.0 μm, Lpp = 1.5 μm)	2.85	2001	1406
Grid pattern (CP = 4.0 μm, L_{pp} = 2.0 μm)	2.88	2002	1393
Grid pattern (CP = 4.0 μm, L_{pp} = 2.5 μm)	2.92	2000	1370
Grid pattern (CP = 4.6 μm, L_{pp} = 0.5 μm)	2.88	1903	1260
Grid pattern (CP = 4.6 μm, L_{pp} = 1.0 μm)	2.89	1974	1347
Grid pattern (CP = 4.6 μm, L_{pp} = 1.5 μm)	2.92	1962	1320
Grid pattern (CP = 4.6 μm, L_{pp} = 2.0 μm)	2.95	1939	1274
Grid pattern (CP = 4.6 μm, L_{pp} = 2.5 μm)	3.00	1927	1238

4. Conclusions

In this paper, 1.7-kV 4H-SiC trench-gate MOSFETs with a P+ source pattern are investigated in terms of P+ source dimension (length and width) on static characteristics, such as output characteristic and forward blocking voltage by 3-D numerical device simulation. It is demonstrated that P+ source pattern is the important factor in TMOSFETs due to cell-pitch and P+/N+ junction curve effect. The proposed TMOSFETs with P+ source with grid pattern reduced the cell-pitch approximately 35% and decreased the p-n junction effect. As a result, the grid P+ source TMOSFETs has a low specific on-resistance of 2.73 mOhm-cm^2 and a high breakdown voltage of 2061 V. Compared with the conventional P+ source pattern TMOSFET structures, simulation results show that the Figure-Of-Merit (FOM, $BV^2/R_{on,sp}$) of the proposed grid pattern TMOSFET is improved by approximately 33%.

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