

Article



Designs of Charge-Balanced Edge Termination Structures for 3.3 kV SiC Power Devices Using PN Multi-Epitaxial Layers

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Abstract: We demonstrated 3.3 kV silicon carbide (SiC) PiN diodes using a trenched ringassisted junction termination extension (TRA-JTE) with PN multi-epitaxial layers. Multiple P⁺ rings and width-modulated multiple trenches were utilized to alleviate electric-field crowding at the edges of the junction to quantitively control the effective charge (Q_{eff}) in the termination structures. The TRA-JTE forms with the identical P-type epitaxial layer, which enables high-efficiency hole injection and conductivity modulation. The effects of major design parameters for the TRA-JTE, such as the number of trenches (N_{trench}) and depth of trenches (D_{trench}), were analyzed to obtain reliable blocking capabilities. Furthermore, the single-zone-JTE (SZ-JTE), ring-assisted-JTE (RA-JTE), and trenched-JTE (T-JTE) were also evaluated for comparative analysis. Our results show that the TRA-JTE exhibited the highest breakdown voltage (BV), exceeding 4.2 kV, and the strongest tolerance against variance in doping concentration for the JTE (N_{JTE}) compared to both the RA-JTE and T-JTE due to the charge-balanced edge termination by multiple P⁺ rings and trench structures.

Keywords: silicon carbide (SiC); edge termination; junction termination extension (JTE); P-type epitaxial growth; trenched ring-assisted-JTE (TRA-JTE); PiN diode

1. Introduction

Silicon carbide (SiC) has a wide energy bandgap and high critical electric field, so it offers significant advantages as a semiconductor material for power devices in highvoltage applications, such as high-voltage direct-current transmission systems and electric transportation [1–3]. SiC-based high-voltage power devices exhibit lower on-state static and switching power losses compared to the conventional Si-based thyristor due to its thinner drift layer [4].

Bipolar devices are suitable for high-voltage applications due to the availability of conductivity modulation, provided that sufficient hole injection occurs from the anode to the drift layer [5–7]. However, the Al implantation process, typically employed for the formation of P-type anodes, is known to introduce various lifetime degrading defects, including $Z_{1/2}$ and basal plane dislocation (BPD) [8–15]. These defects can lead to bipolar degradation, significantly affecting both the performance and long-term reliability of bipolar devices [10,11].

Appropriate edge termination designs are required to mitigate electric-field crowding at the edges of the PN junction. Field-limiting rings (FLRs) and a junction termination extension (JTE) are commonly used structures for SiC power devices [16–30]. In the case of FLRs, multiple P⁺ rings are formed simultaneously with the main junction. However, FLRs require a large chip area to sustain high voltage. On the other hand, a JTE can be



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Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/ licenses/by/4.0/). implemented with a smaller chip area than FLRs by achieving charge balance between the JTE and drift layers. A JTE is required to ensure high breakdown voltage (BV) over a wide range of JTE concentration (N_{ITE}) and fixed oxide charge (Q_F).

Several research groups have reported high-voltage SiC PiN diodes incorporating PN multi-epitaxial layers to enhance conductivity modulation and prevent the devices from degradation-related problems [31–37]. Nevertheless, in the reported studies, the SiC PiN devices employing PN multi-epitaxial layers typically utilized mesa etching to form conventional edge termination structures on the drift layers, such as FLRs and JTEs, using Al implantation [16–30]. The use of mesa etching in P-type epitaxial layers to form edge termination structures dimension reduction and induces relatively complex processes compared to the planar-type structures [31–37].

In this paper, we propose 3.3 kV SiC PiN diodes featuring a trenched ring-assisted junction termination extension (TRA-JTE) using PN multi-epitaxial layers. The TRA-JTE design benefits from the planar nature of P-type epitaxial growth, which facilitates easier design and is expected to enhance hole injection. We evaluated the BVs and electric field distributions of the TRA-JTE structure and compared them with those of the single-zone-JTE (SZ-JTE), ring-assisted-JTE (RA-JTE), and trenched-JTE (T-JTE). The TRA-JTE structure incorporates multiple P⁺ rings and trench-etched regions to effectively control the effective charge (Q_{eff}). We successfully demonstrated the edge termination structure using PN multi-epitaxial layers for high-voltage mesa-shaped devices.

2. Designs and Structures

Process simulation to design various edge termination structures with PN multiepitaxial layers and analyze their electrical characteristics was carried out using Sentaurus TCAD (T-2022.03). Figure 1 shows the cross-sectional views of 3.3 kV SiC PiN diodes with (a) SZ-JTE, (b) RA-JTE, (c) T-JTE, and (d) TRA-JTE. The sequence for process simulation of devices was followed. Initially, a 30 μ m thick N-type drift layer with a doping concentration of 3 \times 10¹⁵ cm⁻³ was epitaxially grown on an N⁺ substrate, followed by the growth of a 2 μ m thick P-type epitaxial layer on the N-type drift layer for use of both hole-injection active regions and JTE structures in edge termination regions. After that, P⁺ regions formed high-dose Al implantation, simultaneously constructing multiple P⁺ rings with a width of 3 μ m for both RA-JTE and TRA-JTE.

The parameter S₁, defined as the spacing between the edge of the main junction and the first P⁺ ring, was optimized to 3 μ m, while the increment in spacing between subsequent P⁺ rings, denoted S_i, was set to 0.5 μ m. The width of the JTE (W_{JTE}) was determined by the mesa etching process and fixed at 135 μ m. For the SZ-JTE and RA-JTE structures, a 2.1 μ m deep etching of the SiC was performed, completely removing the P-type epitaxial layers in the outer JTE regions, accounting for a 5% over-etching margin. In case of T-JTE and TRA-JTE, a 1.5 μ m deep trench etching was carried out prior to the subsequent 0.6 μ m deep mesa etching, as illustrated in Figure 2. The optimized design parameters for each structure are summarized in Table 1.

Structures	W _{JTE} [μm]	D _{mesa} [µm]	D _{trench} [µm]	W _{ring} [µm]	S ₁ [μm]	S _i [µm]
SZ-JTE	135	2.1	-	-	-	-
RA-JTE	135	2.1	-	3	3	0.5
T-JTE	$W_{JTE1} = 70$ $W_{JTE2} = 65$	0.6	1.5	-	-	-
TRA-JTE	$W_{JTE1} = 70$ $W_{JTE2} = 65$	0.6	1.5	3	3	0.5

Table 1. Optimized design parameters of each structure.

(a)	Anode		Field Oxide		
	P ⁺			Dmar	
	P-epi			- mes	4 ·
	N-drift	•	WJTE		-+
	N ⁺ substra Cathode	ite			
(b)					
(~)	Anode	D+ D+ D+ D+	Field Oxide		
	P-epi			D _{me}	sa I
	N-drift		WJTE		
	N ⁺ substra Cathode	ite			
(c)					
(-)	Anode		Field Oxide	to	
	P-epi			↓ D _{trench}	*
		•	+		sa 🖡
	N-drift	WJTE1		W _{JTE2}	
	N ⁺ substra Cathode	ite			
(d)					
(~)	Anode		Field Oxide		
	P ⁺	P. P. P. P.	PT PT	[D _{trench}	
	P-epi			D _{me}	sat
	N-drift	W _{JTE1}	+ +	 W _{JTE2}	
	N ⁺ substra Cathode	ite			

Figure 1. Cross-sectional views of (a) SZ-JTE, (b) RA-JTE, (c) T-JTE, and (d) TRA-JTE.



Figure 2. Widths and spaces between double trenches of TRA-JTE.

3. Results and Discussion

The BVs of the SZ-JTE and RA-JTE structures as a function of N_{JTE} are compared in Figure 3. The RA-JTE exhibits greater tolerance to variations in N_{JTE} compared to the SZ-JTE. While the SZ-JTE has the benefit of being simply formed through a single mesa etching process, it exhibits high sensitivity to N_{JTE}. As a result, the BVs of the SZ-JTE structure remain below 3.3 kV, except when the N_{JTE} value is optimized to 5×10^{16} cm⁻³. In the RA-JTE structure, the presence of multiple P⁺ rings enhances the electric field distribution near the main junction, particularly at low N_{JTE} values.



Figure 3. BVs according to N_{JTE} for SZ-JTE and RA-JTE. N_{JTE} values are increased by 1×10^{16} cm⁻³ from 2×10^{16} cm⁻³ to 6×10^{16} cm⁻³.

Figure 4 shows the electric field distributions of the SZ-JTE and RA-JTE at a reverse bias of 3.0 kV for the N_{JTE} value of 4×10^{16} cm⁻³. The SZ-JTE shows a high electric field value at the main junction, whereas the P⁺ rings of the RA-JTE effectively suppress the electric-field crowding at the main junction.



Figure 4. Electric field distributions of SZ-JTE and RA-JTE at reverse bias of 3.0 kV for N_{JTE} value of $4\times10^{16}~cm^{-3}.$

At a high N_{JTE} exceeding 5×10^{16} cm⁻³, both the SZ-JTE and RA-JTE exhibit sharp reductions in BV due to the significant electric-field crowding at the mesa sidewall, as illustrated in Figure 5. When the electric field concentrates at the mesa edge, avalanche breakdown may occur at undesirably low voltage or irreversible physical damage to the field oxide layer. In the proposed TRA-JTE structure, multiple trenches were additionally employed to optimize the electric field distribution, specifically mitigating crowding at the mesa sidewall to ensure stable blocking performance.



Figure 5. Electric field distributions of (a) SZ-JTE and (b) RA-JTE at reverse bias of 1.2 kV of N_{JTE} value of 6 \times 10¹⁶ cm⁻³.

Figure 6 shows the BVs of the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE according to N_{JTE}. Both the T-JTE and TRA-JTE have high BVs exceeding the rated 3.3 kV up to an N_{JTE} of 1.7×10^{17} cm⁻³, attributed to the effective charge balancing achieved by the trench structure in the P-type epitaxial layers. Our simulation results exhibit that the electric field is effectively distributed among three distinct peaks located at the P⁺ rings, double trenches, and mesa sidewall.



Figure 6. BVs according to N_{JTE} for SZ-JTE, RA-JTE, T-JTE, and TRA-JTE.

Effective charge density ($Q_{eff} = N_{JTE} \times T_{P-epi}$) was used to analyze the charge balance in the edge termination structures, including the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE. We classified the specific regions within the edge termination structures based on the Q_{eff} as illustrated in Figure 7.



Figure 7. Cross-sectional views of Q_{eff} including electrons and holes per unit area for (**a**) SZ-JTE, (**b**) RA-JTE, (**c**) T-JTE, and (**d**) TRA-JTE.

The SZ-JTE exhibits a single region of medium Q_{eff} with a uniform charge distribution, resulting in highly sensitive breakdown characteristics to variation in N_{JTE}. The RA-JTE and TRA-JTE have high Q_{eff} regions attributed to the presence of P⁺ rings so that the potential of the main junction is effectively delivered outward through the termination structure, resulting in stable blocking characteristics even at low N_{JTE}. The T-JTE and TRA-JTE have low Q_{eff} regions due to the locally thinned P-type epitaxial layer. The trenched regions create multiple electric field peaks to support blocking voltage and a gradual increase in potential. In the case of the TRA-JTE, the presence of all the types of Q_{eff} regions offers advantages for achieving charge balance and brings about robust blocking characteristics against variations in N_{JTE}.

Figure 8a illustrates the electric field distributions for the TRA-JTE at a reverse bias of 3.3 kV with various values of N_{JTE}. Regions 1, 2, and 3 include the main junction/multiple P⁺ rings, double trenches/the first mesa, and second mesa, respectively. The multiple P⁺ rings effectively suppress the electric-field crowding near the main junction in the case of an N_{JTE} of 5×10^{16} cm⁻³. For higher N_{JTE} conditions than of 5×10^{16} cm⁻³, the double trenches significantly alleviate the electric field at the mesa sidewall through the charge-balanced P-type epitaxial layer. Figure 8b–e illustrate the locations of the maximum electric field observed in each region of the TRA-JTE structure under various N_{JTE} conditions with the reverse bias of 3.3 kV. As N_{JTE} increases from 5×10^{16} to 1.7×10^{17} cm⁻³, the maximum

electric field in region 1 decreases from 2.10 to 1.90 MV/cm, while that corresponding value in region 3 increases from 0.58 MV/cm to 2.53 MV/cm. It is noted that the TRA-JTE structures demonstrate reliable blocking capability under relatively high N_{JTE} conditions by controlling the charge balance in region 2 through the double trenches so that the electric field peak values are almost evenly distributed across the entire edge termination structure under a higher N_{JTE} of 5×10^{16} cm⁻³.



Figure 8. (a) Electric field distributions for TRA-JTE at reverse bias of 3.3 kV with various N_{JTE} and peak electric field of TRA-JTE per divided region for N_{JTE} values of (b) 5×10^{16} cm⁻³, (c) 8×10^{16} cm⁻³, (d) 1.4×10^{17} cm⁻³, and (e) 1.7×10^{17} cm⁻³.

Figure 9 shows the electric field distributions of the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE at breakdown for the N_{JTE} value of 5 \times 10¹⁶ cm⁻³ with BVs above 3.3 kV for all the

structures. In the case of the SZ-JTE and RA-JTE, the electric field is concentrated at the mesa sidewall. In contrast, for the T-JTE and TRA-JTE, the electric field at the mesa is effectively suppressed because the JTE region is fully depleted prior to the occurrence of avalanche breakdown. As a result, the T-JTE and TRA-JTE exhibit peak values of electric field of less than 2 MV/cm, lower than those of the SZ-JTE and RA-JTE. Notably, the TRA-JTE has the widest N_{JTE} tolerance, surpassing the T-JTE by 8.33%, attributed to the high Q_{eff} at the multiple P⁺ rings.



Figure 9. Electric field distributions of SZ-JTE, RA-JTE, T-JTE, and TRA-JTE at breakdown for N_{JTE} value of 5 \times 10¹⁶ cm⁻³.

Figure 10 shows the forward J–V characteristics of the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE for the N_{JTE} value of 5×10^{16} cm⁻³. Since the main junction is identical for all the structures, the forward voltage drops at a current density of 100 A/cm² are 3.3 V for all the structures. These results demonstrate that the TRA-JTE exhibits the most outstanding reverse characteristics without sacrificing forward characteristics.



Figure 10. J–V characteristics of the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE for the N_{JTE} value of 5×10^{16} cm⁻³.

 Q_F is formed in field oxide during thermal oxidation and post-oxidation annealing [38–40]. It affects the Q_{eff} , potentially causing a change in the BVs of SiC devices [41–43]. Figure 11 shows the simulation results for the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE structures considering several Q_F values in the field oxide. Positive Q_F values attract electrons to the surface, reducing Q_{eff} and decreasing the depletion curvature at the outer edge of the JTE. The incorporation of multiple P⁺ rings in the RA-JTE and TRA-JTE structures effectively compensates for the reduced Q_{eff} . As a result, in the presence of positive Q_F , the BVs of the RA-JTE and TRA-JTE are reduced by only 0.30 kV and 0.66 kV, respectively, whereas the BVs of the SZ-JTE and T-JTE are reduced by 1.07 kV and 1.01 kV, respectively.



Figure 11. BVs according to Q_F of $\pm 2\times 10^{12}$ cm $^{-2}$ for SZ-JTE, RA-JTE, T-JTE, and TRA-JTE at N_{JTE} value of 5 \times 10¹⁶ cm $^{-3}$.

A negative Q_F value increases the Q_{eff} , causing the depletion regions to extend towards the end of the JTE. Consequently, the BVs of the SZ-JTE and RA-JTE are sharply reduced under the condition of a negative Q_F . However, the T-JTE and TRA-JTE exhibit reduced sensitivity to negative Q_F due to their thinner T_{P-epi} by the formation of trenches, which maintain a lower Q_{eff} compared to other structures. It can be observed that the BV of the T-JTE is increased from 4.1 kV to 4.3 kV. Also, the stability of the TRA-JTE was validated, demonstrating relatively less sensitivity to both positive and negative Q_F .

Subsequently, we simulated the TRA-JTE under various design parameters, including the number of trenches (N_{trench}) and depth of trenches (D_{trench}). Figure 12 illustrates the BVs of the TRA-JTE according to N_{JTE} and N_{trench} with identical D_{trench} of 1.5 μ m with a comparison of the results from the RA-JTE. The BVs of the RA-JTE structure are sharply reduced at N_{JTE} of 6 \times 10¹⁶ cm⁻³ because the electric field is crowded at the mesa sidewall, as shown in Figure 5. In the case of the TRA-JTE with a single trench of 3 μ m wide width, the BVs are slightly higher compared to the RA-JTE. However, the TRA-JTE with a single trench is insufficient to effectively distribute the electric field for various N_{JTE} conditions. Our simulation results indicate that the TRA-JTE with double trenches demonstrates the widest N_{JTE} tolerance range even though the structure with triple trenches exhibits slightly higher BV values at N_{JTE} below 1.6 \times 10¹⁷ cm⁻³.



Figure 12. BVs according to N_{JTE} and N_{trench} for RA-JTE and TRA-JTE with identical D_{trench} of 1.5 μ m.

Figure 13 shows the BVs as a function of N_{JTE} for the TRA-JTE with D_{trench} values of 0.5 µm, 1.0 µm, 1.5 µm, and 2.0 µm. In all the cases, the double trenches are employed. The device with D_{trench} of 0.5 µm has slightly higher BVs at low N_{JTE}, attributed to the relatively high Q_{eff} in the trenched region compared to the other D_{trench} conditions. However, the BVs are steeply decreased when N_{JTE} is higher than 7×10^{16} cm⁻³. In the N_{JTE} range between 8×10^{16} cm⁻³ and 1.0×10^{17} cm⁻³, the TRA-JTE with D_{trench} of 1.0 µm shows the highest BVs and N_{JTE} range between 1.1×10^{16} cm⁻³ and 1.7×10^{17} cm⁻³, and the TRA-JTE with D_{trench} of 1.5 µm shows the highest BVs. The larger D_{trench} enhances the spreading depletion in a full JTE region, including a mesa sidewall. However, at D_{trench} of 2.0 µm, too much potential is delivered from the etched region as the P-type epitaxial layer is almost removed.



Figure 13. BVs according to N_{JTE} and D_{trench} for TRA-JTE with double trenches.

Figure 14 shows the electric field distributions of the TRA-JTE with D_{trench} values of (a) 0.5 µm, (b) 1.0 µm, (c) 1.5 µm, and (d) 2.0 µm at the N_{JTE} value of 7×10^{16} cm⁻³. As D_{trench} increases from 0.5 µm to 2.0 µm, the peak electric field points shift from the second mesa to the first trench. Notably, the PiN diode with D_{trench} of 1.5 µm exhibits the widest N_{JTE} tolerance. These results indicate that D_{trench} is a critical design parameter for achieving the charge balance of the TRA-JTE. Figure 13 shows the electric field distributions of the TRA-JTE with D_{trench} values of (a) 0.5 µm, (b) 1.0 µm, (c) 1.5 µm, and (d) 2.0 µm at the N_{JTE} value of 7×10^{16} cm⁻³. As D_{trench} increases from 0.5 µm to 2.0 µm, the peak electric field points shift from the second mesa to the first trench. Notably, the PiN diode with D_{trench} of 1.5 µm exhibits the widest N_{JTE} tolerance. These results increases from 0.5 µm to 2.0 µm, the peak electric field points shift from the second mesa to the first trench. Notably, the PiN diode with D_{trench} of 1.5 µm exhibits the widest N_{JTE} tolerance. Those results indicate that D_{trench} is a critical design parameter for achieving the charge balance of the TRA-JTE.



Figure 14. Electric field distributions of TRA-JTE with D_{trench} values of (a) 0.5 μ m, (b) 1.0 μ m, (c) 1.5 μ m, and (d) 2.0 μ m at N_{TTE} value of 7 \times 10¹⁶ cm⁻³.

4. Conclusions

We designed the SZ-JTE, RA-JTE, T-JTE, and TRA-JTE using PN multi-epitaxial layers as JTEs for 3.3 kV SiC PiN diodes. The RA-JTE and TRA-JTE exhibited high BVs at low N_{JTE} due to the multiple P⁺ rings enhancing the Q_{eff} near the main junction. Additional trench structures for the T-JTE and TRA-JTE effectively sustained high BVs at high N_{JTE} and are less sensitive to Q_F variation without increasing the forward voltage drop. By optimizing the parameters of the TRA-JTE, including N_{trench} and D_{trench}, we demonstrated that the TRA-JTE with double trenches and D_{trench} of 1.5 µm is a suitable edge termination structure for high-voltage SiC devices.

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References

- Spazia, L.; Lu, L. Silicon, GaN and SiC: There's room for all: An application space overview of device considerations. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 8–11. [CrossRef]
- Millán, J.; Godignon, P.; Perpiñà, X.; Pérez-Tomás, A.; Rebollo, J. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Trans. Power Electron.* 2014, 29, 2155–2163. [CrossRef]
- Kimoto, T.; Cooper, J.A. Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications; John Wiley & Sons: Hoboken, NJ, USA, 2014. Available online: https://onlinelibrary.wiley.com/doi/book/10.1002/9781118313534 (accessed on 5 October 2021).
- 4. Kimoto, T. Ultrahigh-voltage SiC devices for future power infrastructure. In Proceedings of the European Solid-State Device Research Conference (ESSDERC), Bucharest, Romania, 16–20 September 2013; pp. 22–29. [CrossRef]
- Jacobs, K.; Heinig, S.; Johannesson, D.; Norrga, S.; Nee, H.-P. Comparative evaluation of voltage source converters with silicon carbide semiconductor devices for high-voltage direct current transmission. *IEEE Trans. Power Electron.* 2021, 36, 8887–8906. [CrossRef]
- 6. Niwa, H.; Suda, J.; Kimoto, T. Ultrahigh-voltage SiC MPS diodes with hybrid unipolar/bipolar operation. *IEEE Trans. Electron Devices* **2017**, *65*, 874–881. [CrossRef]
- Kimoto, T.; Suda, J.; Yonezawa, Y.; Asano, K.; Fukuda, K.; Okumura, H. Progress in ultrahigh-voltage SiC devices for future power infrastructure. In Proceedings of the 2014 IEEE Int. Electron Devices Metting (IEDM), San Francisco, CA, USA, 15–17 December 2014; pp. 2.5.1–2.5.4. [CrossRef]
- 8. Tsunenobu, K.; Watanabe, H. Defect engineering in SiC technology for high-voltage power devices. *Appl. Phys. Exp.* **2020**, 13, 120101. [CrossRef]
- 9. Kawahara, K.; Alfieri, G.; Kimoto, T. Detection and depth analyses of deep levels generated by ion implantation in n- and p-type 4H-SiC. *J. Appl. Phys.* **2009**, *106*, 013719. [CrossRef]
- Mancini, S.A.; Jang, S.Y.; Kim, D.; Sung, W. Static Performance and Reliability of 4H-SiC Diodes with P+ Regions Formed by Various Profiles and Temperatures. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 27–31 March 2022; pp. P62-1–P62-6. [CrossRef]
- 11. Bu, Y.; Yoshimoto, H.; Watanabe, N.; Shima, A. Fabrication of 4H-SiC PiN diodes without bipolar degradation by improved device processes. *J. Appl. Phys.* **2017**, *122*, 244504. [CrossRef]
- 12. Kimoto, T.; Yamada, K.; Niwa, H.; Suda, J. Promise and challenges of high-voltage SiC bipolar power devices. *Energies* **2016**, *9*, 908. [CrossRef]
- 13. Fukaya, S.; Yonezawa, Y.; Kato, T.; Kato, M. Depth Distribution of Defects in SiC PiN Diodes Formed Using Ion Implantation or Epitaxial Growth. *Phys. Status Solidi B* **2022**, 259, 2100419. [CrossRef]
- 14. Peters, D.; Bartsch, W.; Thomas, B.; Sommer, R. 6.5 kV SiC PiN diodes with improved forward characteristics. *Mater. Sci. Forum* **2010**, 645–648, 901–904. [CrossRef]
- 15. Erlekampf, J.; Kallinger, B.; Weiße, J.; Sommer, M.; Berwian, P.; Friedrich, J.; Erlbaxher, T. Deeper insight into lifetime-engineering in 4H-SiC by ion implantation. *J. Appl. Phys.* **2019**, *126*, 045701. [CrossRef]
- 16. Huang, C.-F.; Hsu, H.-C.; Chu, K.-W.; Lee, L.-H.; Tsai, M.-J.; Lee, K.-Y.; Zhao, F. Counter-Doped JTE, an edge termination for HV SiC devices with increased tolerance to the surface charge. *IEEE Trans. Electron Devices* **2015**, *62*, 354–358. [CrossRef]
- 17. Zhou, C.-N.; Wang, Y.; Yue, R.-F.; Dai, G.; Li, J.-T. Step JTE, an edge termination for UHV SiC power devices with increased tolerances to JTE dose and surface charges. *IEEE Trans. Electron Devices* **2017**, *64*, 1193–1196. [CrossRef]
- Pérez, R.; Mestres, N.; Blanqué, S.; Tournier, D.; Jorda, X.; Godignon, P.; Nipoti, R. A highly effective edge termination design for SiC planar high power devices. *Mater. Sci. Forum* 2004, 457–460, 1253–1256. [CrossRef]
- 19. Sung, W.; Van Brunt, E.; Baliga, B.J.; Huang, A.Q. A new edge termination technique for high-voltage devices in 4H-SiC multiple-floating-zone junction termination extension. *IEEE Electron Device Lett.* **2011**, *32*, 880–882. [CrossRef]
- 20. Sung, W.; Baliga, B.J. A Near Ideal Edge Termination Technique for 4500 V 4H-SiC Devices: The Hybrid Junction Termination Extension. *IEEE Electron Device Lett.* 2016, *37*, 1609–1612. [CrossRef]
- Dai, T.; Zhang, L.; Vavasour, O.; Renz, A.B.; Cao, Q.; Shah, V.A.; Mawby, P.A.; Antoniou, M.; Gammon, P.M. A Compact and Cost-efficient Edge Termination Design for High Voltage 4H-SiC Devices. In Proceedings of the 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Nagoya, Japan, 30 May–3 June 2021; pp. 251–254. [CrossRef]

- 22. Van Brunt, E.; Cheng, L.; O'Loughlin, M.J.; Richmond, J.; Pala, V.; Palmour, J.W.; Tipton, C.W.; Scozzie, C. 27 kV, 20 A 4H-SiC n-IGBTs. *Mater. Sci. Forum* 2015, *821*, 847–850. [CrossRef]
- Wen, Y.; Xu, X.; Zhu, H.; Li, X.; Deng, X.; Yang, F.; Li, J.; Zhang, B. Design and characteristics of an etching field limiting ring for 10kV SiC power device. In Proceeding of the 2019 16th China International Forum on Solid State Lighting & 2019 International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS), Shenzhen, China, 25–27 November 2019; pp. 37–41. [CrossRef]
- 24. Hirao, T.; Onose, H.; Yasui, K.; Mori, M. Edge termination with enhanced field-limiting rings insensitive to surface charge for high-voltage SiC power devices. *IEEE Trans. Electron Devices* **2020**, *67*, 2850–2853. [CrossRef]
- 25. Kao, Y.C.; Wolley, E.D. High-voltage planar p-n junctions. Proc. IEEE 1967, 55, 1409–1414. [CrossRef]
- Temple, V.A.K.; Tantraporn, W. Junction termination extension for near-ideal breakdown voltage in p-n junctions. *IEEE Trans. Electron Devices* 1986, ED-33, 1601–1608. [CrossRef]
- Li, S.; Liu, H.; Huang, R.; Tao, Y.; Liu, Q.; Li, Y.; Bai, S. Simulation, fabrication and characterization of 6500V 4H-SiC power DMOSFETs. In Proceedings of the 2014 14th China International Forum on Solid State Lighting & 2019 International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS), Beijing, China, 1–3 November 2017; pp. 144–147. [CrossRef]
- Tan, B.; Tian, X.-L.; Lu, J.; Bai, Y.; Deng, X.-C.; Li, C.-Z.; Liu, X.-Y. Design and Optimization of Four-Region Multistep Field Limiting Rings for 10 kV 4H-SiC IGBTs. In Proceedings of the 2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Qingdao, China, 31 October–3 November 2018. [CrossRef]
- Deng, X.; Xu, S.; Zhang, B.; Zeng, L.; Li, C.; Wu, J.; Li, J. A Near Ideal Edge Termination Technique for Ultrahigh-Voltage 4H-SiC Devices with Multi-Zone Gradient Field Limiting Ring. In Proceedings of the 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Xi'an, China, 16–18 May 2018; pp. 144–148. [CrossRef]
- 30. Broderick, L.Z.; Moult, J.; Rusch, O.; Tong, T.; Erlbacher, T.; Corcoran, Y.L. Highly Efficient Floating Field Rings for SiC Power Electronic Devices—A Systematic Experimental Study. *Key Eng. Mater.* **2023**, *946*, 103–110. [CrossRef]
- 31. Hiyoshi, T.; Hori, T.; Suda, J.; Kimoto, T. Simulation and Experimental Study on the Junction Termination Structure for High-Voltage 4H-SiC PiN Diodes. *IEEE Trans. Electron Devices* **2008**, *55*, 1841–1846. [CrossRef]
- 32. Feng, G.; Suda, J.; Kimoto, T. space-modulated junction termination extension for ultrahigh-voltage p-i-n diodes in 4H-SiC. *IEEE Trans. Electron Devices* **2012**, *59*, 414–418. [CrossRef]
- Salemi, A.; Elahipanah, H.; Zetterling, C.-M. Conductivity Modulated and Implantation-Free 4H-SiC Ultra-High-Voltage PiN Diodes. *Mater. Sci. Forum* 2018, 924, 568–572. [CrossRef]
- 34. Hu, R.; Deng, X.; Xu, X.J.; Li, X.; Li, J.; Li, Z.; Zhang, Y.; Zhang, B. An improved composite JTE termination technique for ultrahigh voltage 4H-SiC power devices. In Proceedings of the 16th China International Forum on Solid State Lighting & 2019 International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS), Shenzhen, China, 25–27 November 2019; pp. 18–21. [CrossRef]
- 35. Johannesson, D.; Nawaz, M.; Nee, H.P. Assessment of junction termination extension structures for ultrahigh-voltage silicon carbide pin-diodes; a simulation study. *IEEE Open J. Power Electron.* **2021**, *2*, 304–314. [CrossRef]
- Nakayama, K.; Mizushima, T.; Takenaka, K.; Koyama, A.; Kiuchi, Y.; Matsunaga, S.; Fujisawa, H.; Hatakeyama, T.; Takei, M.; Yonezawa, Y.; et al. 27.5 kV 4H-SiC PiN diode with space-modulated JTE and carrier injection control. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 395–398. [CrossRef]
- 37. Deng, X.; Li, L.; Wu, J.; Li, C.; Chen, W.; Li, J.; Li, Z.; Zhang, B. A multiple-ring-modulated JTE Technique for 4HSiC power device with improved JTE-dose window. *IEEE Trans. Electron Devices* 2017, 65, 5042–5047. [CrossRef]
- Yun, N.; Sung, W. Detailed Analysis on Determining Effective Dose for Various JTE-Based Edge Terminations Utilized on 4H-SiC Power Devices. *IEEE Trans. Electron Devices* 2022, 69, 3826–3832. [CrossRef]
- Yang, X.; Lee, B.; Misra, V. Electrical characteristics of SiO₂ deposited by atomic layer deposition on 4H-SiC after nitrous oxide anneal. *IEEE Trans. Electron Devices* 2016, 63, 2826–2830. [CrossRef]
- 40. Yu, S.; White, M.H.; Agarwal, A.K. Experimental determination of interface trap density and fixed positive oxide charge in commercial 4H-SiC power MOSFETs. *IEEE Access* **2021**, *9*, 149118–149124. [CrossRef]
- 41. Yen, C.T.; Hung, C.C.; Lee, C.Y.; Lee, L.S.; Huang, Y.F.; Yang, T.M.; Cheng, C.Y. Effect of fixed oxide charges and donor-like interface traps on the breakdown voltage of SiC devices with FGR and JTE terminations. *Mater. Sci. Forum* **2015**, *821–823*, 729–732. [CrossRef]
- 42. Balaji, S.; Karmalkar, S. Effects of oxide-fixed charge on the breakdown voltage of superjunction devices. *IEEE Electron Device Lett.* 2007, *28*, 229–231. [CrossRef]
- 43. Matsushima, H.; Okino, H.; Mochizuki, K.; Yamada, R. The impact of interface charge on the breakdown voltage of terminated 4H-SiC power devices. *Mater. Sci. Forum* **2015**, *821–823*, 652–655. [CrossRef]

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