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IR drop-independent 8T1C LTPS pixel circuit for medium-sized AMOLED displays

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ABSTRACT

OLED displays have been widely used in mobile devices due to their numerous advantages. The pixel circuits of OLED displays typically employ low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) for their high mobility and reliability. However, LTPS TFTs suffer from threshold voltage (V_{TH}) variation, sometimes leading to OLED current error (OCE) and non-uniform display. A diode connection method was used in the conventional OLED pixel circuit to compensate for this limitation. However, the impact of IR drop in the metal lines necessitates developing a new circuit to eliminate the adverse effect of IR drop. Accordingly, this paper proposed an 8T1C LTPS pixel circuit, featuring an additional reference voltage for V_{TH} compensation independent of IR drop. Simulation results demonstrate that the suggested circuit effectively compensates for V_{TH}, ensuring uniform OLED performance regardless of IR drop. This circuit design also enables consistent image quality, particularly in medium-sized displays, where IR drop would be severe, by maintaining uniform OLED current across the entire panel.

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SUBJECT CLASSIFICATION CODES
Display Circuits and Systems; AMD; OLED

1. Introduction

Organic light-emitting-diode (OLED) displays offer several advantages over liquid crystal displays (LCDs), including higher contrast ratio, wider viewing angle, faster response time, and wider color gamut [1–4]. Thus, OLED displays have been extensively used in smartphones. As a result, it is anticipated that OLED displays will be increasingly used in medium-sized mobile devices, such as tablets and laptops.

Most OLED display pixel circuits employ low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) due to their high mobility and reliability [5,6]. However, LTPS TFTs exhibit non-uniformity of threshold voltage (V_{TH}) due to non-uniform crystallinity of silicon films annealed by excimer laser beam [7]. Variations in V_{TH} of driving TFTs result in different OLED currents, even when an identical data voltage is applied. This leads to OLED current error (OCE). Therefore, it is essential to compensate for the threshold voltages of the driving TFTs to ensure a uniform image.

Threshold voltage compensation methods are typically divided into external and internal methods [8–16]. The external compensation method requires additional memory and logic blocks, which increases system cost [8–10]. On the other hand, internal compensation methods are usually employed in mobile displays to reduce system cost, with the diode connection method being commonly used [14–16].

Figure 1 illustrates a conventional seven-transistors-one-capacitor (7T1C) pixel circuit [16]. A data voltage is applied during the data writing and compensation phase while sensing V_{TH} of the driving TFT, M1. At this time, the voltage stored in the storage capacitor, as specified in Equation (1), leads to the OLED emission current during the emission phase as described in Equation (2).

$$(7T1C)V_{C\_ST} = ELVDD - (V_{DATA} - |V_{TH\_M1}|) \quad (1)$$

$$(7T1C)I_{OLED} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(ELVDD - V_{DATA})^2 \quad (2)$$

However, the circuit can result in non-uniform images because the ELVDD term remains and varies depending on the location across the display.

Figure 2 highlights the influence of metal line resistance on IR drop. Assuming that ELVDD is supplied from a driver located at the top of the panel, the voltage at the top remains stable. However, as OLED currents flow through the inherent resistance in the metal lines, the ELVDD of pixels far from the driver decreases. For

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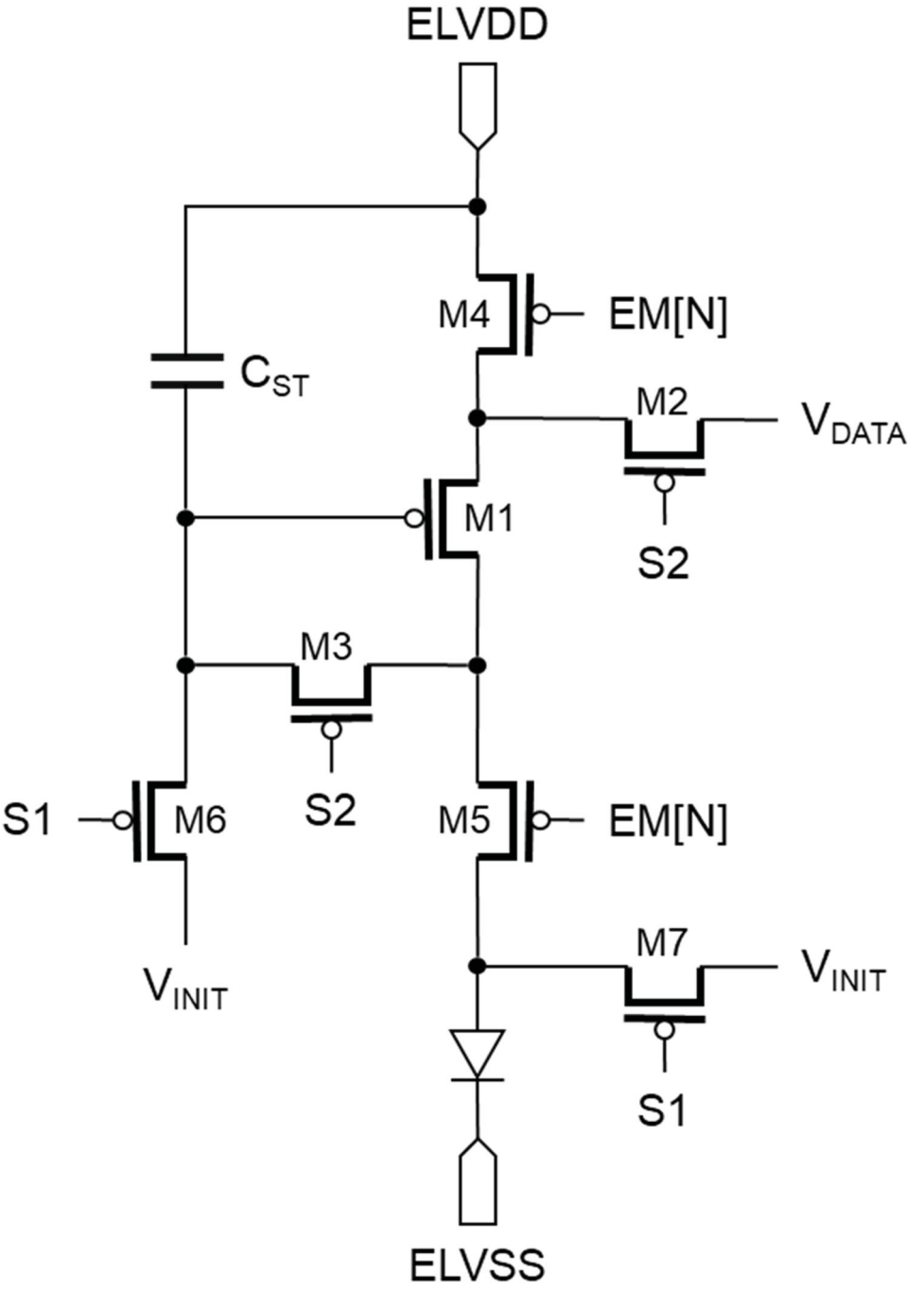


Figure 1. Schematic diagram of conventional 7T1C pixel circuit [16].

instance, the voltage drop across R1 is caused by the product of the resistance and the cumulative current flowing through the OLEDs in the lower sections of the panel, as reflected in Figure 2. As a result of the IR drop across each resistance, a lower ELVDD is applied to the lower pixel circuits. This leads to non-uniform luminance across the OLED panel, as each storage capacitor contains a different ELVDD term. IR drop can be severe in medium-sized panels due to their longer metal lines [17,18]. One approach to address this problem is to improve the layout using a mesh structure, which connects the metal lines in horizontal and vertical directions, supplying voltage from multiple sides to ensure a more uniform distribution [19]. Another method involves predicting the IR drop and compensating for it by adjusting the data voltage [20]. However, these methods do not completely resolve the IR drop issue and tend to increase the complexity of the operation. As a result, some previous studies have already proposed pixel circuits that compensate for V_{TH} independent of ELVDD [21–24]; however, they have

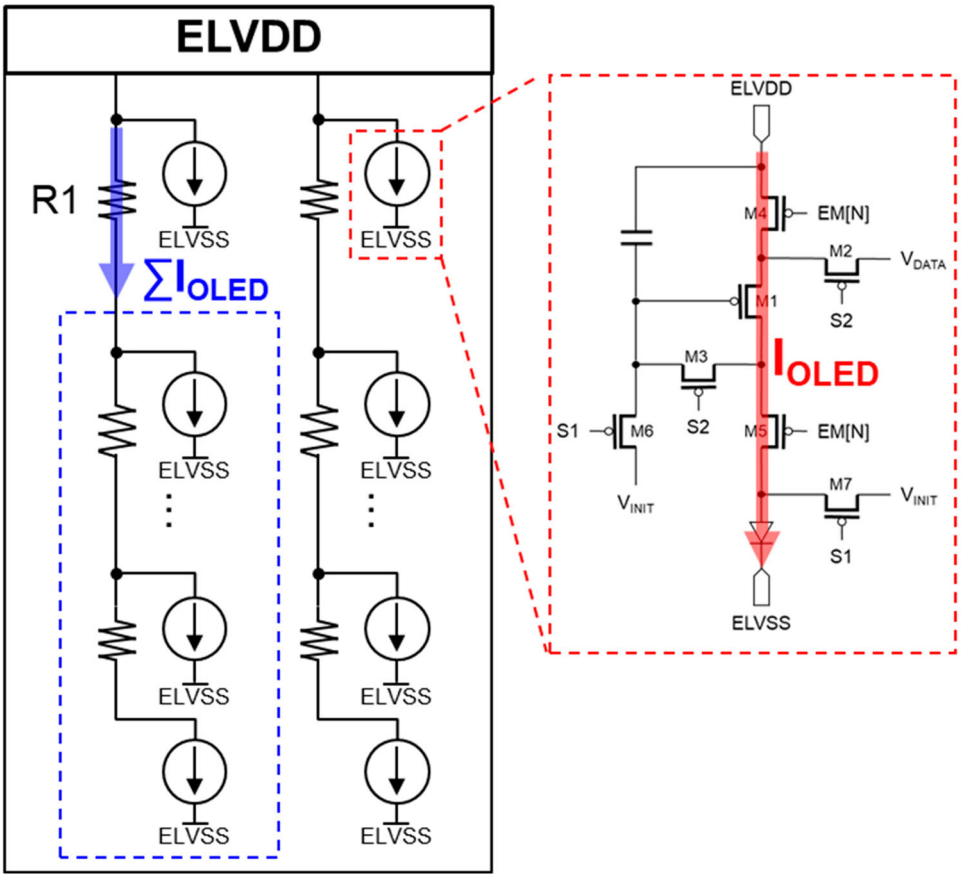


Figure 2. IR drop: Impact of metal line resistance on ELVDD.

encountered some problems, such as regarding settling time for stable operation, luminance distortion on various refresh rates (VRR) driving, and increased power consumption.

This paper proposes a novel LTPS TFT-based pixel circuit that ensures uniform OLED current, regardless of V_{TH} variation and IR drop, while effectively addressing the limitations of previous studies. The proposed circuit uses a reference voltage, allowing the storage capacitor to store both the data voltage and V_{TH} information without being affected by IR drop.

2. Proposed pixel circuit

Figure 3(a) is a schematic of the proposed pixel circuit, and Figure 3(b) is a timing diagram of its operation. The circuit consists of a driving TFT (M1), seven switching TFTs (M2–M8), and one storage capacitor (C_{ST}). All the TFTs are LTPS TFTs. The operation phases of the proposed circuit are synthesized in Figure 4. A cycle of the operation includes initialization (T_{INIT}), data writing and compensation (T_{COMP}), hold (T_{HOLD}), and emission (T_{EMS}) phases.

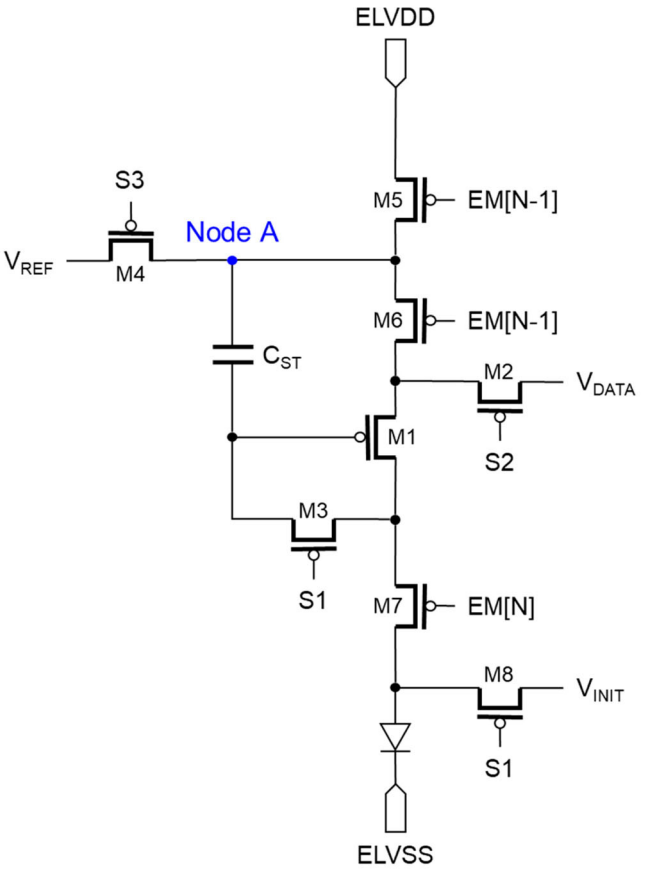
2.1. Initialization phase (T_{INIT})

In the initialization phase, EM[N] and S1 signals are set low to initialize the gate voltage of the driving TFT and OLED anode to V_{INIT}, as delineated in Figure 4(a). Since the S3 signal is also low, the voltage of node A becomes V_{REF}. At this point, the EM[N-1] signal is high to turn off M5 and M6, so no current flows through OLED.

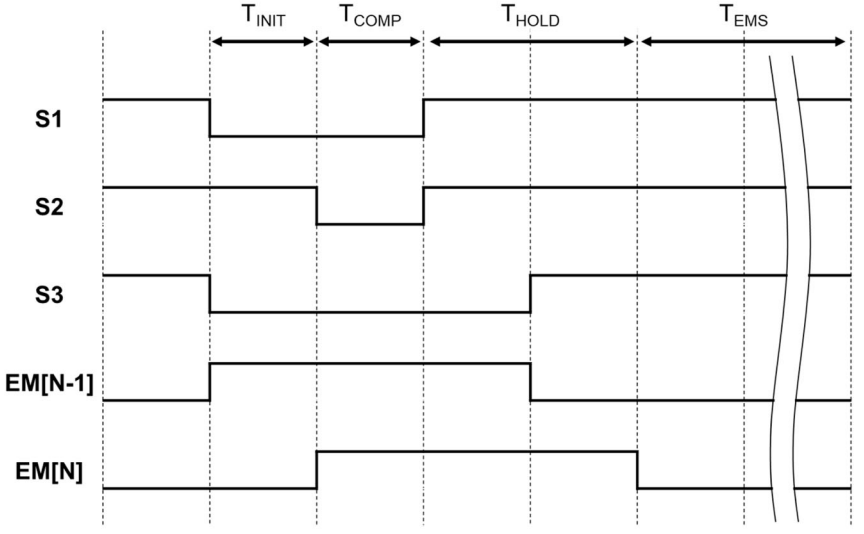
2.2. Data writing and compensation phase (T_{COMP})

In the data writing and compensation phase, S1 and S3 are low, which turns on M3, M4, and M8. Since EM[N-1] and EM[N] are high, M5, M6, and M7 remain off, as set up in Figure 4(b). Because S3 is low, node A maintains V_{REF}. At the same time, S2 goes low to transfer V_{DATA} to the source node of M1. Since M1 becomes diode-connected via M3, the gate node of M1 becomes $V_{DATA} - |V_{TH\_M1}|$, stored in the storage capacitor. In other words, the capacitor contains information regarding M1's data voltage and threshold voltage.

The proposed 8T1C pixel circuit has an additional signal, V_{REF}, for the threshold voltage compensation, which is not affected by IR drop, ensuring that data information can be accurately written to the target level across



(a)



(b)

Figure 3. (a) Schematic diagram of the proposed pixel circuit and (b) timing diagram of its operation.

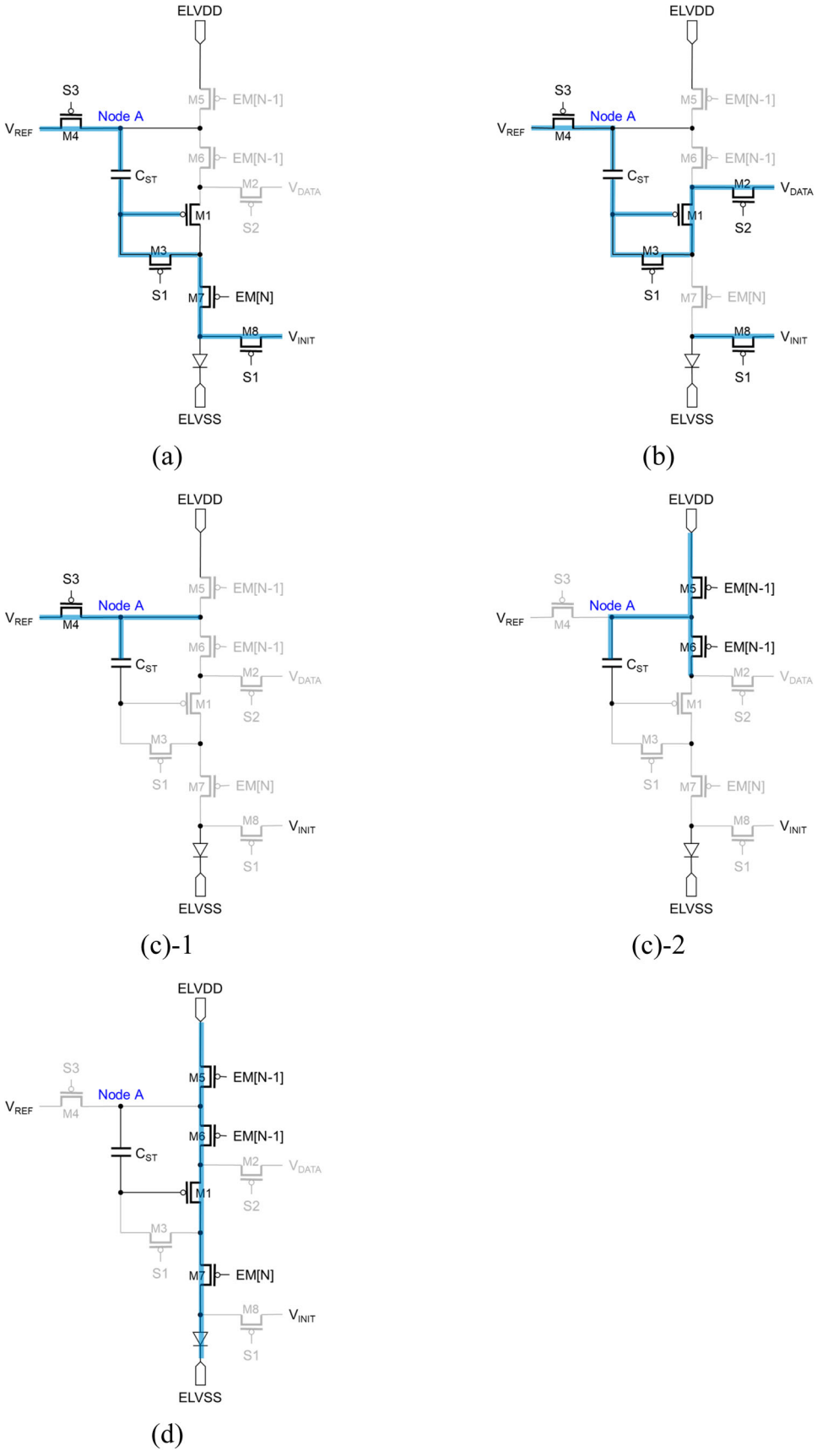


Figure 4. The operation of the proposed pixel circuit: (a) initialization phase, (b) data writing and compensation phase, (c) hold phase, and (d) emission phase.

Table 1. Design parameters of the proposed pixel circuit in the SPICE simulation.

Parameter	Value
W/L(M1)	10 µm/15µm
W/L(M2 – M8)	3 µm/3µm
V_{ELVDD}	7.0 V
V_{ELVSS}	−1.5 V
V_{REF}	7.0 V
V_{INIT}	0.0 V
C_{ST}	250 fF
C_{OLED}	1 pF
V_{GH}, V_{GL}	9 V, −6V
V_{DATA}	6.03 V to 7.53 V
T_{COMP}	3.8 µs

the entire panel. The following equations describe the voltage stored in the capacitor of the proposed circuit, thereby ensuring that the proposed circuit can maintain consistent luminance even if there is a drop in the ELVDD.

$$(8T1C)\, V_{C_{ST}} = V_{REF} - (V_{DATA} - |V_{TH\_M1}|) \qquad (3)$$

2.3. Hold phase (T_{HOLD})

In the hold phase, S1 and S2 go high first, turning off M2, M3, and M8, as indicated in Figure 4(c)-1. Then, S3 goes high to turn off M4, and EM[N-1] goes low, with node A becoming V_{ELVDD}, as displayed in Figure 4(c)-2. However, the voltage across C_{ST} remains unchanged, V_{REF} – (V_{DATA} – $|V_{TH}|$), because at least one terminal of C_{ST} is floating.

2.4. Emission phase (T_{EMS})

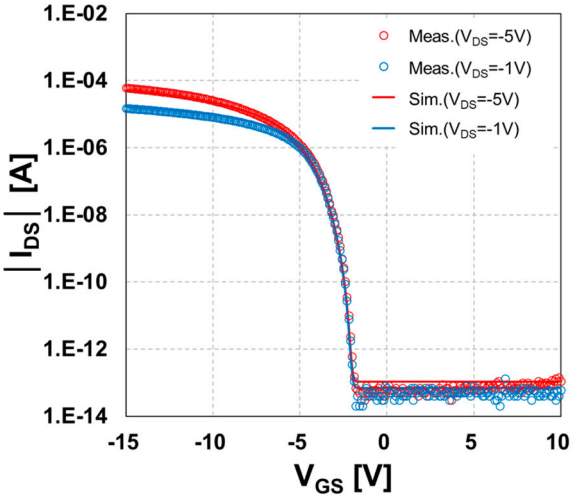
In the emission phase, EM[N] goes low to turn on M7, enabling the programed current to flow through OLED, while S1, S2, and S3 are high to turn off these switching TFTs, as laid out in Figure 4(d).

$$(8T1C)\ I_{OLED} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{REF} - V_{DATA})^2 \qquad (4)$$

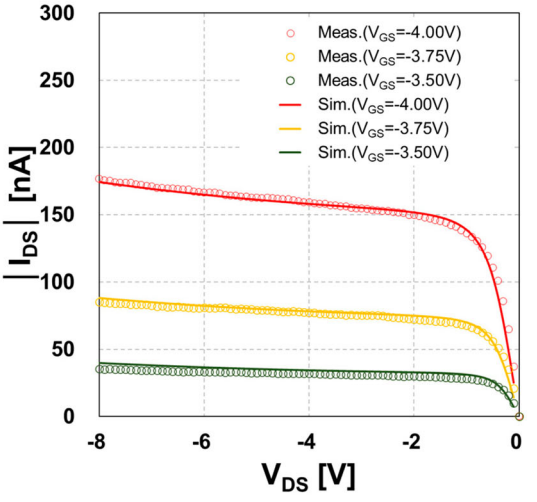
3. Results and discussion

Figure 5 compares the measured and simulated characteristics of the fabricated LTPS TFT (W/L = 10 µm/15 µm) and the OLED I-V curve used in the SPICE simulation. The SPICE simulations were conducted using SmartSpice (Level = 36) to validate the operation of the proposed pixel circuit. Table 1 summarizes the TFT dimensions and driving voltages used in the simulation.

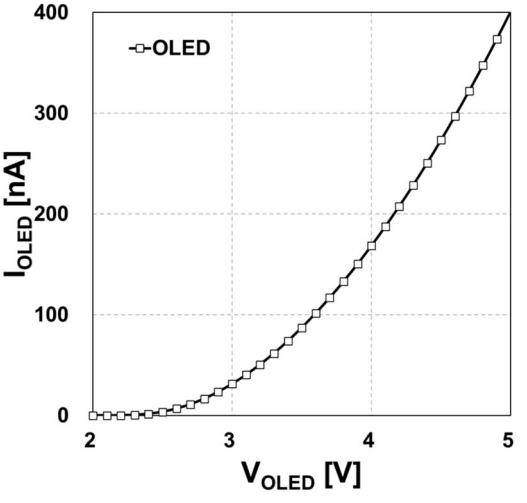
We have designed the layout of the proposed circuit, as represented in Figure 6. The layout rules are detailed in Table 2. The layout dimensions of the circuit were 33.3 µm × 99.9 µm. This corresponds to the pixel density



(a)



(b)



(c)

Figure 5. (a) Measured and simulated transfer curve of LTPS TFT (W/L = 10 µm/15 µm), (b) measured and simulated output curve of LTPS TFT, and (c) OLED I-V curve used in the SPICE simulation.

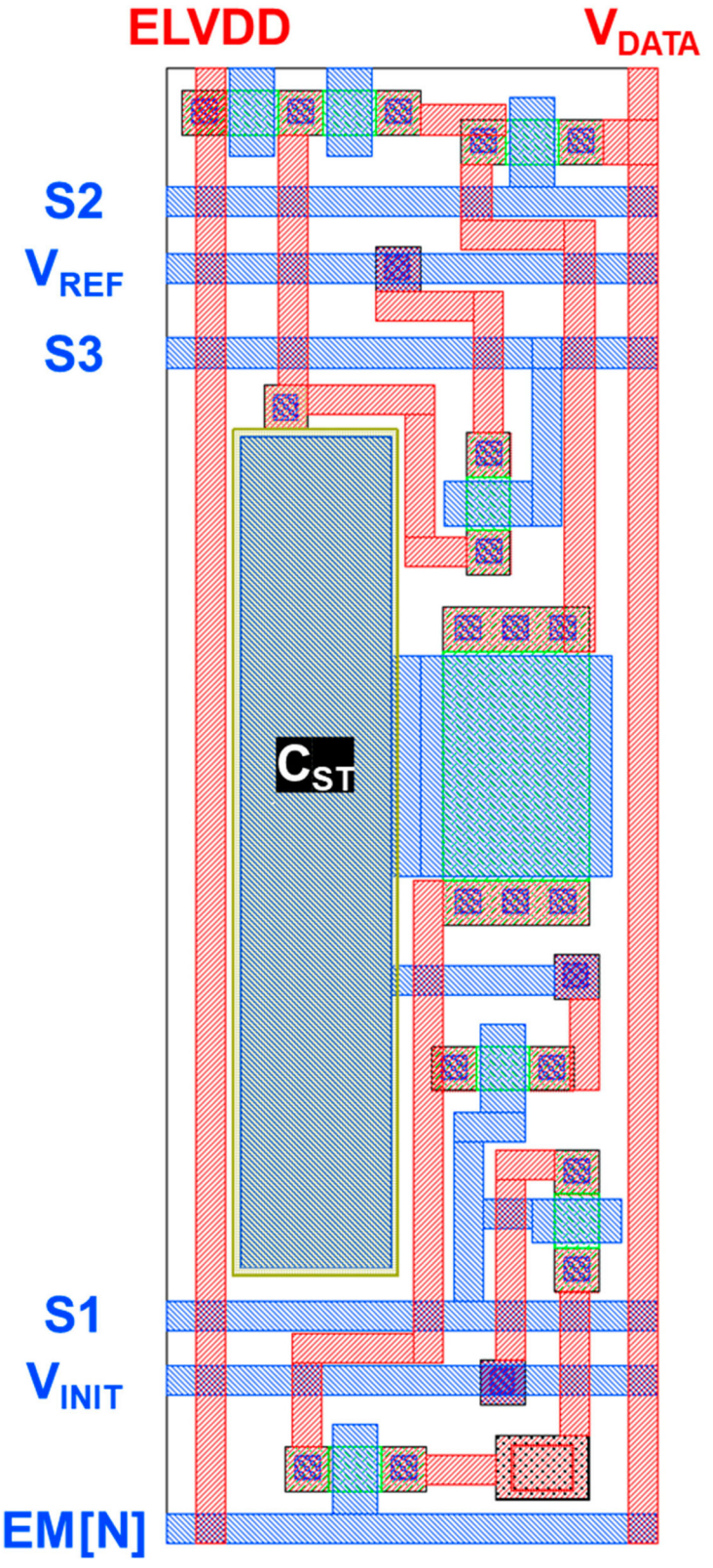


Figure 6. Layout of the proposed 8T1C pixel circuit.

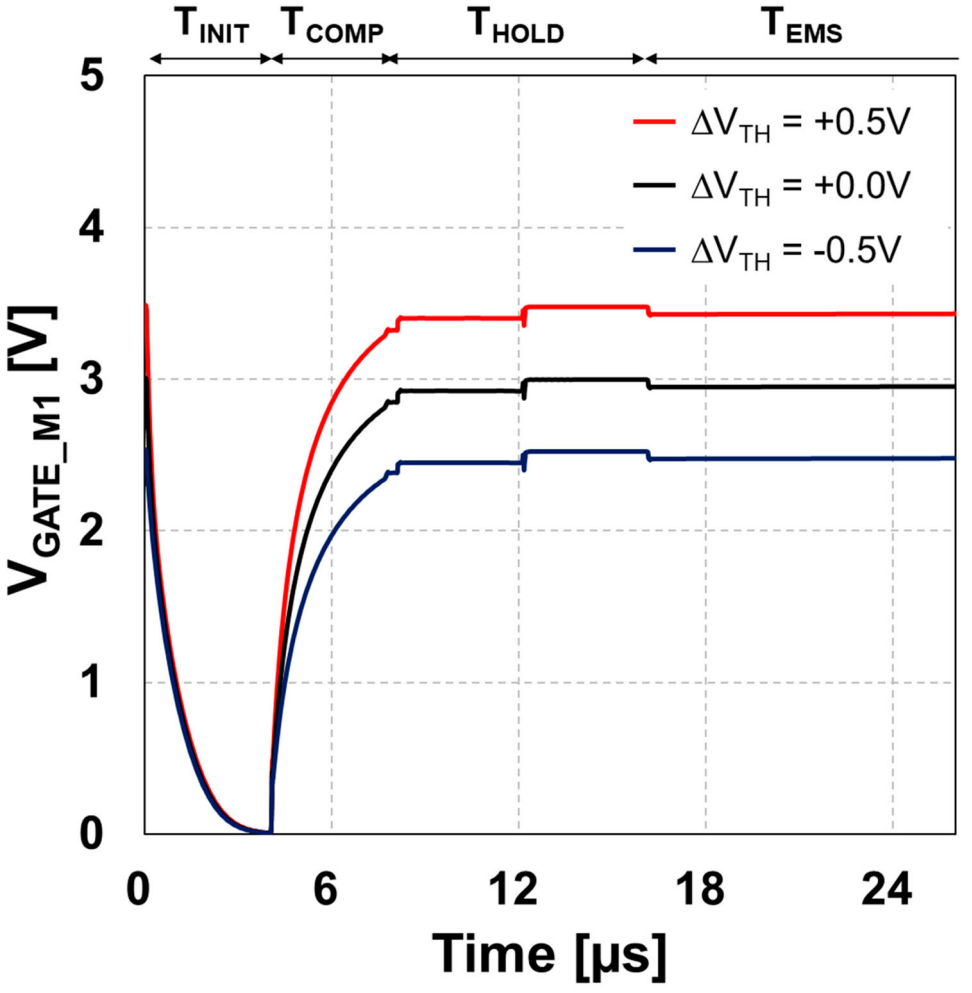


Figure 7. The transient waveforms of the gate voltage of the driving TFT according to the variation of V_{TH}.

Table 2. Layout design rule of the p-channel LTPS TFT process.

Parameter	Value
Minimum width of the active layer	2.0 μm
Minimum space between two active layers	2.0 μm
Minimum width of the gate	2.0 μm
Minimum space between two gates	2.0 μm
Minimum width of S/D	2.0 μm
Minimum size of CNT	1.6 μm
Minimum space between two S/Ds	2.0 μm
Minimum extension of the gate from CNT	1.4 μm
Minimum extension of S/D from CNT	1.4 μm
Minimum size of Via	4.0 μm × 3.0 μm
Minimum extension of S/D from Via	1.9 μm

of 254 pixels per inch (ppi) for a 14.2-inch display with a resolution of 3,024 × 1,964. Hence, the proposed circuit is expected to be applied in medium-sized displays. The parasitic capacitance was extracted from the overlapping area in the layout, which was incorporated into the simulation of the proposed circuit to evaluate whether it could effectively compensate for the IR drop even with the presence of parasitic capacitances.

Figure 7 depicts the simulated transient waveforms of the gate voltage of driving TFT (M1) at the current level of 100 nA according to the variation of the threshold voltage. The gate voltage was initialized to 0.0 V at T_{INIT}. Subsequently, the data voltage was programed, and the threshold voltage of M1 was compensated in T_{COMP}. After T_{HOLD}, the current flows through OLED. For ΔV_{TH} of +0.5, 0.0 V, and −0.5 V, the gate voltages at 24 μs were 3.65, 3.16, and 2.66 V, respectively. Likewise, the proposed pixel circuit can compensate for the threshold voltage variation of the driving TFT.

The conventional circuit (7T1C) was compared with the proposed circuit (8T1C) under identical simulation conditions. Figure 8 illustrates the current levels according to the data voltages.

Figure 9 plots OCEs for two circuits under threshold voltage variation, assuming no IR-drop at current levels of 2, 5, 10, 20, 50, 100, 150, 200, and 250 nA. The OCE was calculated using the following

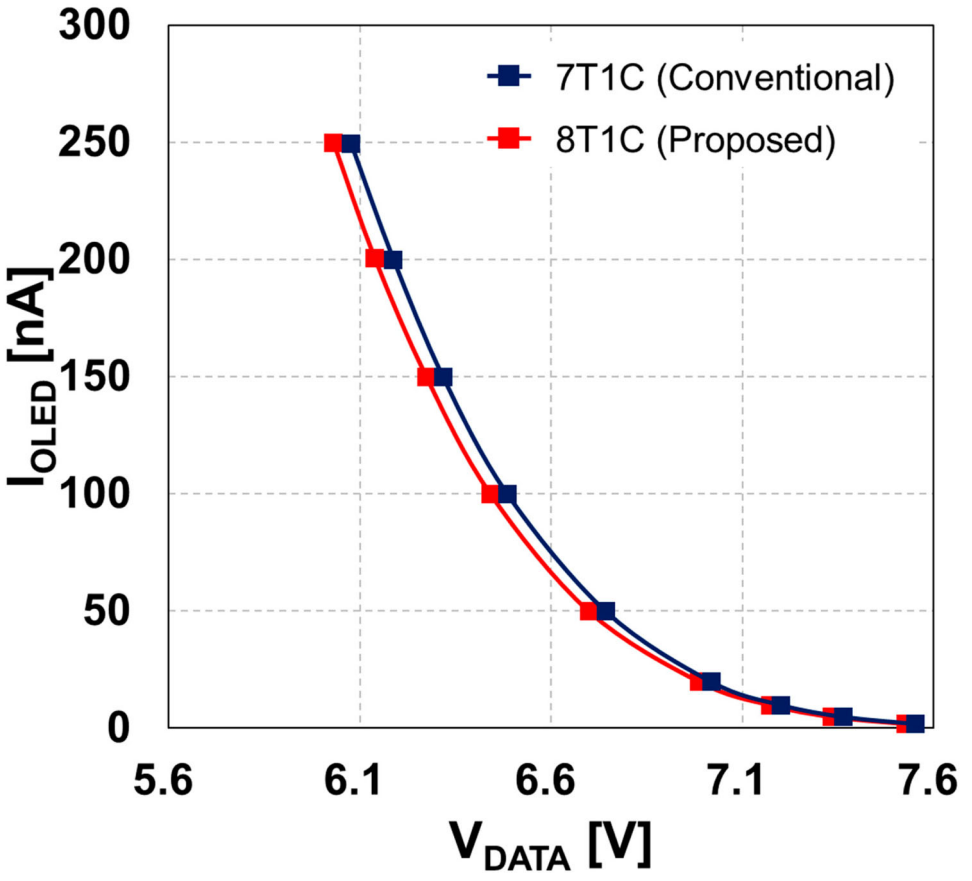


Figure 8. The current levels are according to the data voltages of the conventional and proposed circuits.

equation:

$$OCE[\%] = \frac{I_{OLED}(\Delta V_{TH} = 0V) - I_{OLED}(\Delta V_{TH})}{I_{OLED}(\Delta V_{TH} = 0V)} \times 100 \quad (5)$$

Both circuits presented OCE variations of less than 5%, demonstrating that both circuits can achieve threshold voltage compensation effectively.

Figure 10 illustrates OCE according to the OLED current levels with IR drop of ELVDD or IR rise of ELVSS. The researchers performed simulations considering that ELVDD could decrease by up to 0.55 V for the 14-inch display [20], and ELVSS could increase by up to 0.55 V. The conventional circuit exhibited significant OCE ranging from 72.5% to almost 100.0% as the ELVDD decreases. Contrarily, the proposed circuit maintains the target current levels with a maximum OCE of less than 3.9%. Indeed, the proposed circuit achieves threshold voltage compensation performance comparable to conventional circuits and remains unaffected by IR drop. However, the ELVSS rise did not have any significant impact under these simulation conditions, as the driving TFT operated in the saturation mode.

Table 3 compares previous studies on IR drop-independent pixel circuits [16,21–24]. Although the conventional circuit supports V_{TH} compensation and anode voltage initialization for luminance expression at low gray level [16], it cannot compensate for IR drop, leading to significantly high OCE, as described in Figure 10. Nevertheless, although other circuits can compensate for IR drop, they have certain disadvantages when applied to OLED displays. For example, when the data voltage increases in the next frame, V_{TH} compensation may become ineffective since the storage capacitor voltage may not be initialized properly [21]. Consequently, some studies used a short-circuit current to initialize the storage capacitor; however, this approach results in higher power consumption [22,23].

One method, the advanced power de-coupled (aPDC) technique, utilizes a mesh line to connect an additional DC line for V_{TH} compensation and connects ELVDD during emission [24]. However, due to the high RC loads and the use of a single switching TFT to switch mesh line voltage transition, this method poses some settling issues. While increasing the width of the switching TFT could help reduce the impact of RC loads on settling time,

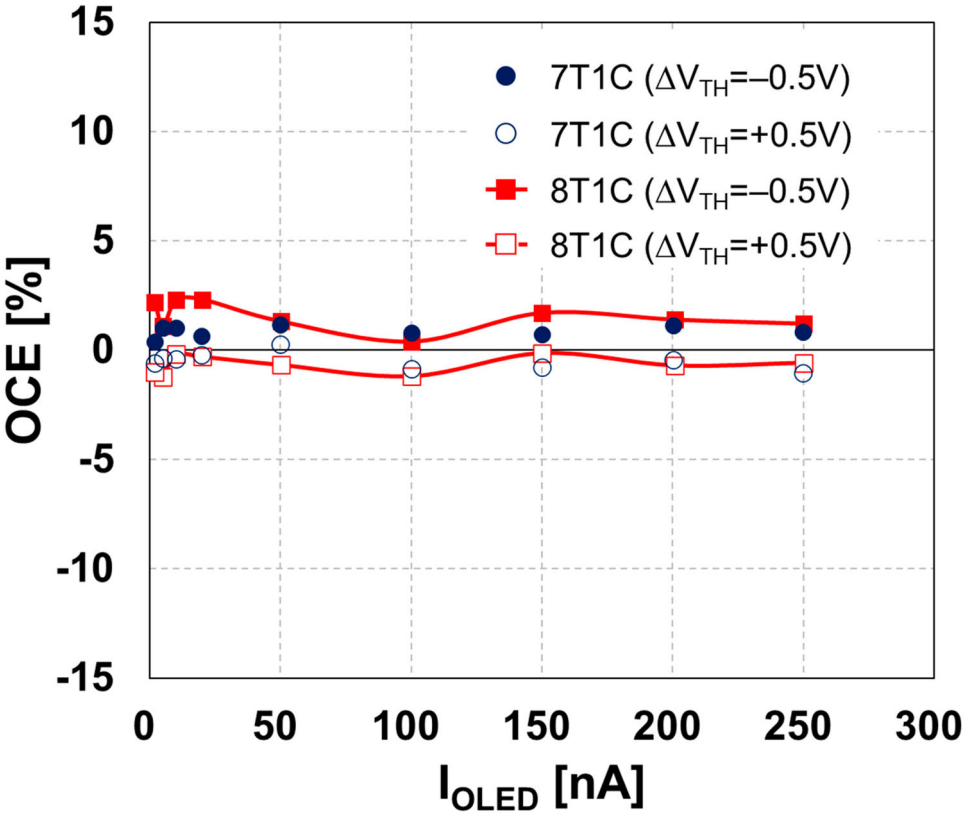


Figure 9. OCEs according to the OLED current levels with the variation of threshold voltage, assuming no IR-drop.

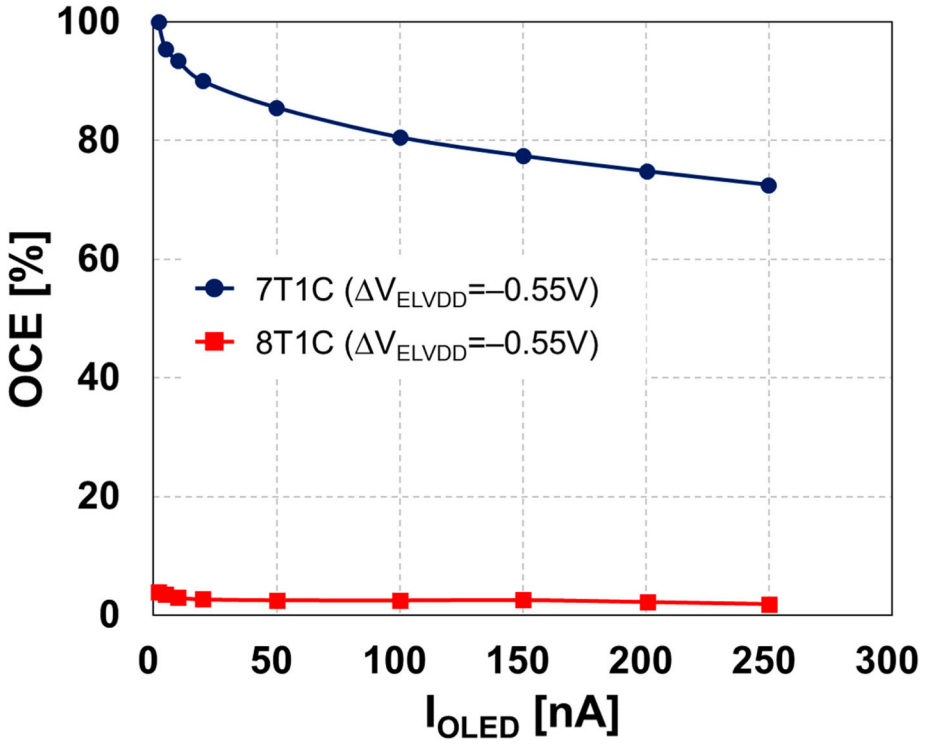
Table 3. Comparison with previous works.

	This work	Ref. [16]	Ref. [21]	Ref. [22]	Ref. [23]	Ref. [24]
Pixel structure	8T1C	7T1C	7T1C	5T1C	6T1C	aPDC 7T1C
IR drop compensation	O	X	O	O	O	O
V_{TH} compensation performance	O	O	△	O	O	O
Settling time	O	O	O	O	O	X
Luminance expression at low gray level on VRR driving	O	O	X	X	X	X
Power efficiency	O	O	O	X	X	O

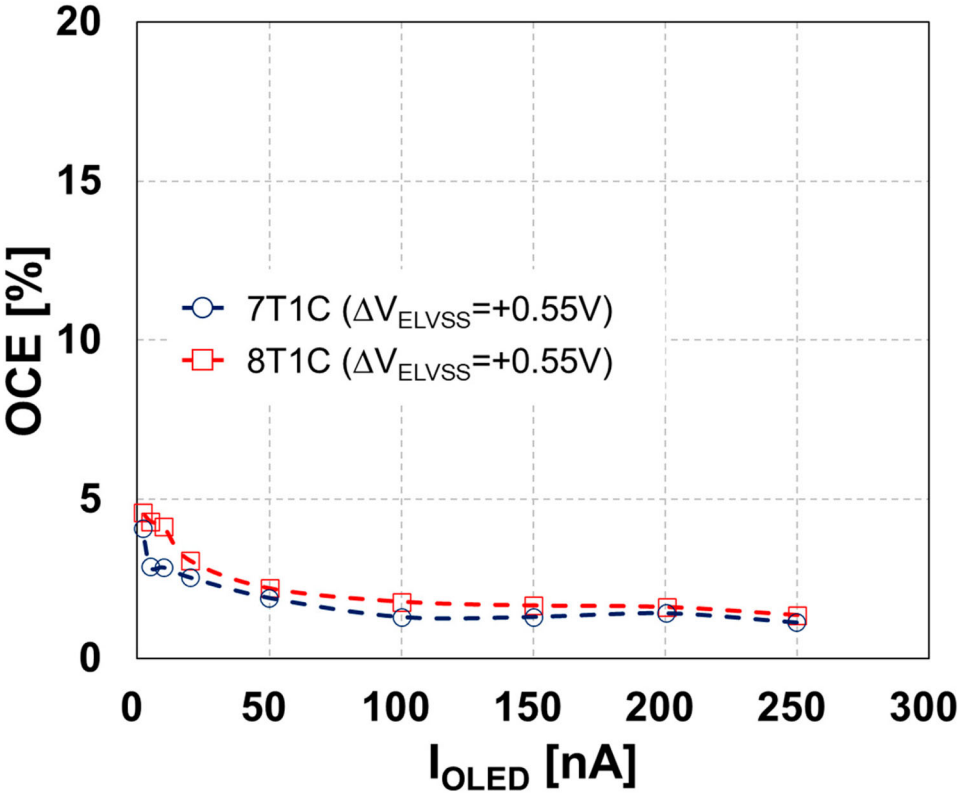
its placement outside the pixel area may lead to a larger bezel [24]. Furthermore, to implement the VRR technique crucial for low-power operation in mobile displays, the OLED anode voltage should be initialized differently based on the refresh rate to prevent luminance distortion at low gray levels [25,26]. However, traditional circuits are deemed unsuitable for VRR operation, as they often do not initialize the anode voltage [21,22,24] or require the data voltage to be adjusted according to the initialized anode voltage [23]. Accordingly, the suggested circuit effectively compensates for both V_{TH} and IR drop, overcoming the limitations of previous designs and offering a valuable improvement for medium-sized OLED displays.

4. Conclusion

This study proposed a p-type LTPS-TFT pixel circuit comprising eight TFTs and one capacitor. The featured circuit includes additional TFTs and a reference voltage line compared to the conventional 7T1C pixel circuit to ensure threshold voltage compensation independently of IR drop. Simulation results demonstrate that the proposed circuit can compensate for the TFT's threshold voltage and maintain a constant OLED current regardless of IR drop. The circuit enables a 254 ppi display, suggesting that medium-sized displays can achieve uniform image quality irrespective of pixel position.



(a)



(b)

Figure 10. OCE, according to the OLED current levels, has (a) an IR drop of ELVDD and (b) an IR rise of ELVSS.

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Disclosure statement

No potential conflict of interest was reported by the author(s).

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Seung-Woo Lee (Senior Member, IEEE) received his B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology in 1993, 1995, and 2000, respectively, where he researched integrated driver circuits for poly-Si TFT-LCDs. He joined Samsung in 2000, where he focused on developing key driving technologies for active-matrix liquid-crystal displays. He has played a key role in image quality enhancement, high-end LCD timing-controller design, FPGA evaluation of new driving schemes, next-generation LCD interface technologies, and advanced LCD driving schemes for large-size TV applications. He was also responsible for creating analog–digital mixed-signal ICs for TFT-LCDs. He joined Kyung Hee University, Seoul, South Korea, where he has been studying novel display systems and visual perception. He is currently a professor of the university's Department of Information Display. He has been active as a Senior Member of the Society for Information Display since 2010. He was also a recipient of the 2008 Chester Sall Award from the IEEE Consumer Electronics Society in 2010.

References

[1] M. Baldo, D. O'Brien, Y. You, A. Shoustikov, S. Sibley, M.E. Thompson and S.R. Forrest, Nature **395**, 151–154 (1998).
[2] B. Geffroy, P.L. Roy and C. Prat, Polym. Int. **55** (6), 572–582 (2006).
[3] M. Stewart, R.S. Howell, L. Pires and M.K. Hatalis, IEEE Trans. Electron Devices **48** (5), 845–851 (2001).
[4] S. Takasugi, H.-J. Shin, M.-K. Chang, S.-M. Ko, H.-J. Park, J.-P. Lee, H.-S. Kim and C.-H. Oh, J. Soc. Inf. Disp. **24** (7), 410–418 (2016).
[5] M. Tada, K. Mochizuki, T. Tsunashima, H. Tanaka, T. Ito, H. Watakabe, A. Hanada, R. Kimura and Y. Ishii, SID Symp., Dig. **49** (1), 117–120 (2018).
[6] H. Watakabe, T. Jinnai, I. Suzumura, A. Hanada, R. Onodera, M. Tada, K. Mochizuki, H. Tanaka and T. Ito, SID Symp., Dig. **50** (1), 541–544 (2019).
[7] T.F. Chen, C.F. Yeh and J.C. Lou, IEEE Electron Device Lett. **24** (7), 457–459 (2003).
[8] W. Liu, G. Yao, C. Jiang, Q. Cui and X. Guo, J. Disp. Technol. **10** (12), 991–994 (2014).
[9] Y.-F. Jin and H.-J. Xie, SID Tech. Dig. **49**, 541–543 (2018).
[10] K.-S. Kang, J.-K. Lee, J.-M. Kang and S.-Y. Lee, IEEE J. Electron Devices Soc. **9**, 311–317 (2021).
[11] C.-L. Lin, W.-Y. Chang and C.-C. Hung, IEEE Electron Device Lett. **34** (9), 1166–1168 (2013).
[12] C.-L. Lin, P.-S. Chen, P.-C. Lai, T.-C. Chu, M.-X. Wang and C.-L. Lee, J. Disp. Technol. **12** (12), 1664–1667 (2016).
[13] D. Kim, Y. Kim, S. Lee, M.-S. Kang, D.-H. Kim and H. Lee, IEEE J. Electron Devices Soc. **5** (5), 372–377 (2017).
[14] C.-L. Lin, F.-H. Chen, Y.-T. Liu, C.-M. Lu and W.-L. Wu, SID Tech. Dig. **47**, 1254–1256 (2016).
[15] N.H. Keum, S.K. Hong and O.K. Kwon, IEEE J. Solid-State Circuits **55** (11), 3087–3096 (2020).
[16] J.S. Lee and S.K. Lee, US Patent No. 10,170,048 (1 January 2019).
[17] J. Park, M. Fujii, J. Moon and I. Wang, SID Tech. Dig. **50** (1), 81–84 (2019).
[18] S.-Y. Lee, S.-H. Kuk, S.-M. Song, M.-K. Song and M.-K. Han, ECS Trans. **500** (8), 269–275 (2012).
[19] M.-H. Jung, O. Kim and H.-J. Chung, J. Korean Phys. Soc. **48** (9), S5–S9 (2006).
[20] P.C.-P. Chao, S.-S. Cheng, C.-H. Chen and K.-Y. Lee, IEEE J. Electron Devices Soc. **10**, 627–636 (2022).
[21] S.Y. Lee, S.-H. Kuk, S.-M. Song, M.-K. Song and M.-K. Han, ECS Trans. **50** (8), 269–275 (2013).
[22] C.-L. Fan, M.-C. Shang, W.-C. Lin, H.-C. Chang, K.-C. Chao and B.-L. Guo, Adv. Mater. Sci. Eng. **2012**, 5 (2012).
[23] LG Display Co., Ltd., KR Patent No. 10,194,577 (2012).
[24] S.-M. Choi, D.-H. Ryu, K.-N. Kim, J.-B. Choi, B.-H. Kim and B. Berkeley, Jpn. J. Appl. Phys. **50**, 03CC04 (2011).
[25] L.J. Kim, S. Jung, H.J. Kim, B.H. Kim, K.J. Kwon, Y.M. Ha and H.J. Kim, Sci. Rep. **12**, 5977 (2022).
[26] N.-Y. Kim, D.-S. Sim, C.-H. Jeon, N.-B. Choi, H.-W. Hwang and S.-W. Lee, IEEE Access **12**, 105346–105353 (2024).