Self-Refresh Memory in Pixel Circuit With 18-bit Color Depth for Liquid Crystal Displays

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***Abstract*— In this letter, we propose memory in pixel (MIP) circuit that achieves 6-bit depth per sub-pixel, resulting in an 18-bit color depth for RGB displays. The circuit integrates two memory cells, each storing 3-bit gray level data, allowing the pixel to self-refresh without requiring continuous input from the graphics processor. This is achieved with a novel driving scheme that eliminates the need for continuous data processing for a static image. The proposed circuit achieves a 97.2% reduction in power consumption compared to the conventional pixel circuit. Furthermore, it extends the bit depth per sub-pixel from 3-bit in our previous work to 6-bit, significantly enhancing grayscale resolution. In addition, the circuit supports gamma correction, allowing precise grayscale reproduction across the full dynamic range.**

***Index Terms*— Low power display, memory in pixel (MIP), thin film transistor (TFT), self-refresh.**

I. Introduction

PANEL self-refresh (PSR) is a technology that enables displays to maintain static images without continuous operation of the system's graphics processor [1], [2], [3]. In conventional display systems, the graphics processor renders and delivers every image frame to the panel in a repetitive sequence [1]. However, for static images, this constant updating of image data becomes redundant and consumes unnecessary system resources [2]. PSR addresses this inefficiency by storing images in a frame memory within the panel. This mechanism allows the panel to display static images without requiring additional input from the processor. Consequently, the system can enter an idle mode where the processor neither renders nor delivers image information, resulting in significant power savings [3].

Despite its advantages, PSR implementation faces challenges. The technology requires an additional frame buffer to store image data. As a display resolution increases, the volume of data to be stored grows correspondingly, leading to increased costs for frame buffers [3]. To address these challenges, extensive research has been conducted on memory in pixel (MIP) circuits for liquid crystal displays (LCDs). These MIP circuits aim to display static images without a frame buffer by integrating memory within the pixel circuit [4], [5], [6], [7], [8], [9], [10], [11]. MIP designs typically incorporate automatic polarity inversion of pixel voltages to prevent image sticking.

MIP circuits have been developed in two primary categories. The static type requires more than six thin-film transistors (TFTs) [4], [5], [6], which can impede the achievement of high-resolution. In contrast, the dynamic type utilizes one capacitor to store pixel voltage and more than one TFT [7], [8], [9]. This design offers advantages for high-resolution displays. A significant limitation of early MIP circuits was their ability to drive only one-bit depth displays [7], [10], [11]. This constraint resulted in inaccurate color representation and artifacts along object edges [12]. Consequently, increasing the bit depth became essential for implementing high-quality displays.

In our previous work, we proposed an MIP circuit for LCD comprising two TFTs and one capacitor, which was verified to implement 3-bit depth [13]. Building on this foundation, this letter introduces a 6-bit depth MIP circuit consisting of four TFTs and two capacitors. We have employed a novel driving scheme and validated the proposed circuit's 6-bit depth capability through experimental measurements.

II. Proposed Circuit

Fig. 1 illustrates the proposed MIP circuit and its corresponding timing diagram. The circuit comprises two memory cells, each capable of discriminating 3-bit depth, thereby enabling a total of six bits for gray level representation. Upper memory cell determines the upper three bits (U3B), while lower memory cell determines the lower three bits (L3B). The combination of U3B and L3B forms a six-bit value corresponding to a gray level, which determines the pixel voltage. U3B and L3B are programmed using data voltages (V_{DATA_UP}, V_{DATA_LO}), which can assume eight distinct voltage levels. RF_UP and RF_LO are global signals for self-refresh, modulating the gate voltages of M1 and M2 through capacitive coupling with C_{ST1} and C_{ST2}, respectively. REF functions as a global signal that charges the pixel node based on the gate-source voltages (V_{GS}) of M1 and M2.

A. Programming Period (T_{PRG})

The voltages of DATA_UP and DATA_LO are programmed into pixels as eight distinct voltage levels, corresponding to

Received 10 April 2025; revised 24 April 2025; accepted 30 April 2025. Date of publication 5 May 2025; date of current version 1 July 2025. This work was supported in part by the Basic Science Research Program through NRF under Grant NRF-2020R1I1A3A04037918 and in part by the Brain Korea 21 Four Program in 2024. The review of this letter was arranged by Editor T.-Y. Seong. *(Corresponding authors: Seung-Woo Lee; Hoon-Ju Chung.)*

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Digital Object Identifier 10.1109/LED.2025.3566707

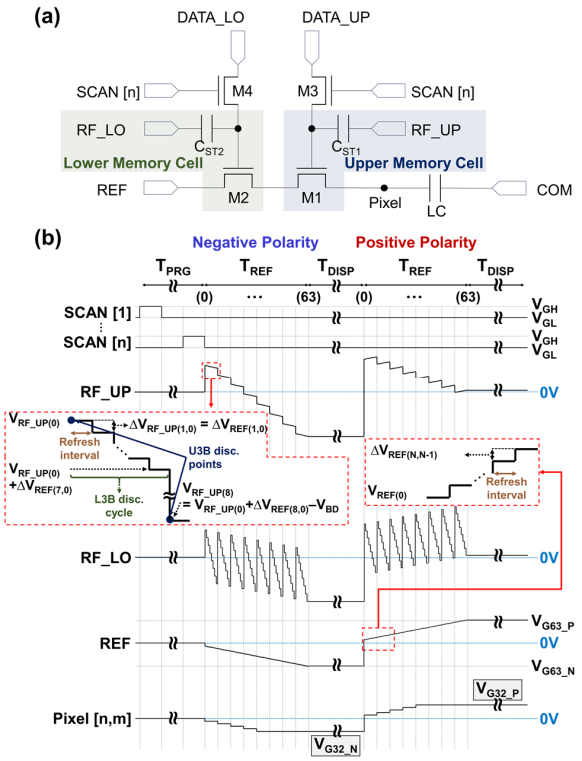

Fig. 1. (a) Proposed circuit and (b) Timing diagram for the circuit.

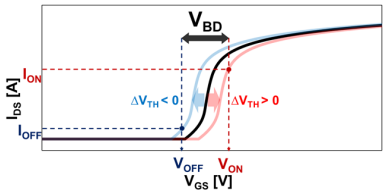

Fig. 2. Minimum V_{BD} defined by $V_{ON} - V_{OFF}$.

the U3B and L3B, respectively. The global signals of RF_UP, RF_LO, and REF are kept at 0V indicated by the blue horizontal lines in Fig. 1.

B. Refresh Period (T_{REF})

During the refresh period, all pixels are refreshed simultaneously using global signals. The REF signal exhibits negative/positive stepped waveforms consisting of 64 voltage levels corresponding to gray level 0 to 63, as shown in Fig. 1(b). We define V_{BD} as the key parameter for bit discrimination voltage to be larger than the difference between V_{ON} and V_{OFF}, as illustrated in Fig. 2. I_{ON} represents a high current level sufficient to charge the pixel node to REF voltage within unit refresh interval, while I_{OFF} is a low current level that results in almost no changes of the pixel voltage. Since V_{ON} and V_{OFF} can vary due to the threshold voltage (V_{TH}), V_{TH} variations must be considered to determine V_{BD}. Thus, V_{BD} is determined as V_{ON} ($\Delta V_{TH} > 0$) − V_{OFF} ($\Delta V_{TH} < 0$) + V_{MARGIN}, where V_{MARGIN} is added to ensure reliable discrimination.

Table I explains the impact of V_{BD} on bit discrimination, specifically for L3B discrimination. This is achieved by modulating the voltages of DATA_LO and RF_LO to control V_{GS} of M2 as shown in Fig. 1(a). Each L3B corresponds to a unique V_{DATA_LO}, which defines the bit value by setting the gate voltage of M2 at T_{PRG}. As L3B increments, DATA_LO

TABLE I
VOLTAGE LEVELS OF DATA_LO FOR L3B DISCRIMINATION AND RF_LO DURING T_{REF}

L3B	DATA_LO	T_{REF}	RF_LO
000	$V_{DATA\_LO\_GL0}$	(0)	$V_{RF\_LO(0)}$
001	$V_{DATA\_LO\_GL0}+1\times V_{BD}$	(1)	$V_{RF\_LO(0)}-1\times V_{BD}+\Delta V_{REF(1,0)}$
010	$V_{DATA\_LO\_GL0}+2\times V_{BD}$	(2)	$V_{RF\_LO(0)}-2\times V_{BD}+\Delta V_{REF(2,0)}$
011	$V_{DATA\_LO\_GL0}+3\times V_{BD}$	(3)	$V_{RF\_LO(0)}-3\times V_{BD}+\Delta V_{REF(3,0)}$
100	$V_{DATA\_LO\_GL0}+4\times V_{BD}$	(4)	$V_{RF\_LO(0)}-4\times V_{BD}+\Delta V_{REF(4,0)}$
101	$V_{DATA\_LO\_GL0}+5\times V_{BD}$	(5)	$V_{RF\_LO(0)}-5\times V_{BD}+\Delta V_{REF(5,0)}$
110	$V_{DATA\_LO\_GL0}+6\times V_{BD}$	(6)	$V_{RF\_LO(0)}-6\times V_{BD}+\Delta V_{REF(6,0)}$
111	$V_{DATA\_LO\_GL0}+7\times V_{BD}$	(7)	$V_{RF\_LO(0)}-7\times V_{BD}+\Delta V_{REF(7,0)}$
		(8)	$V_{RF\_LO(0)}+\Delta V_{REF(8,0)}$

increases by a multiple of V_{BD} starting from $V_{DATA\_LO\_GL0}$. RF_LO modulates the gate voltage of M2 over time to enable bit discrimination across T_{REF}. As T_{REF} progresses, RF_LO gradually decreases the V_{GS} of M2 for bit discrimination, turning M2 off based on the programmed V_{DATA_LO}. Each RF_LO step also must account for the change in V_{REF} steps, which affects the V_{GS} of M2 as a source/drain node of M2. For example, if L3B = 000, M2 should be turned on only at $T_{REF(0)}$ which is ensured by setting $V_{ON}+V_{MARGIN} > V_{GS\_M2} = V_{DATA\_LO\_GL0}+V_{RF\_LO(0)}-V_{REF(0)} \geq V_{ON}$ at $T_{REF(0)}$. At $T_{REF(1)}$, RF_LO is adjusted by V_{BD} for bit discrimination while also incorporating $\Delta V_{REF(1,0)}$, which represents the difference between REF voltages at $T_{REF(1)}$ and $T_{REF(0)}$. At $T_{REF(8)}$, RF_LO is controlled to restore V_{GS_M2} to its initial voltage as at $T_{REF(0)}$, which is given by $V_{DATA\_LO\_GL0}+V_{RF\_LO(0)}-V_{REF(0)}$.

As shown in Fig. 1(b), L3B and U3B are independently controlled through the combination of DATA_LO with RF_LO and DATA_UP with RF_UP, respectively. Bit values are defined by DATA voltages, and the corresponding RF signals modulate the gate voltage of M1 or M2 to enable bit discrimination. The initial voltages of RF_UP ($V_{RF\_UP(0)}$) and DATA_UP ($V_{DATA\_UP\_GL0}$) are chosen to initially turn on M1, while allowing bit discrimination across different U3B, similar to how $V_{RF\_LO(0)}$ and $V_{DATA\_LO\_GL0}$ are determined for M2. Although DATA_UP and DATA_LO operate independently and can be set independently, their voltage levels should be chosen considering the operating range of the display driver IC.

RF_LO and RF_UP feature 64 voltage levels during T_{REF}s, modulating the V_{GS} of M2 and M1, respectively. Thus, RF_LO is responsible for L3B and RF_UP is responsible for U3B. Specifically, to enable the discrimination of L3B = M at the corresponding $T_{REF(N)}$, RF_LO is set to $V_{RF\_LO(0)}-\times V_{BD} + \Delta V_{REF(N,0)}$ at $T_{REF(N)}$, where M satisfies M = N mod 8. Similarly, RF_UP is set to $V_{RF\_UP(0)}-M\times V_{BD} + \Delta V_{REF(N,0)}$ at $T_{REF(N)}$ to discriminate for U3B = M, where M satisfies M = floor(N/8).

As T_{REF} progresses, REF incrementally charges the pixel node when both M1 and M2 are on. Specifically, T_{REF} consists of 64 refresh intervals which is divided into two segments: L3B discrimination cycles (L3B disc. cycles) and U3B discrimination points (U3B disc. points), as illustrated by the left dashed box in Fig. 1(b). Each L3B disc. cycle consists of eight refresh intervals, repeated eight times throughout one T_{REF}

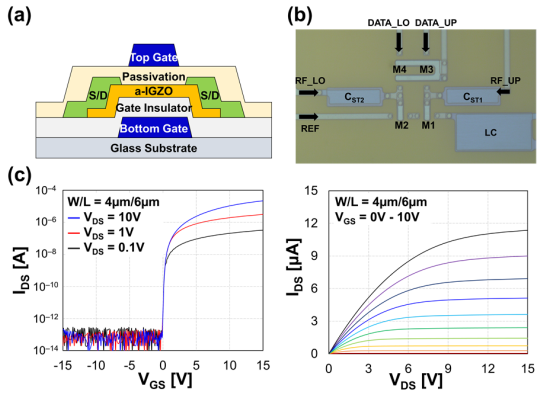

Fig. 3. (a) The cross-section view of oxide TFT [13] (b) Micrograph of the fabricated circuit (c) Transfer curve and output curve of oxide TFT (W/L=4μm/6μm).

period, creating consistent on-off sequences based on the programmed DATA_LO. U3B disc. points occur eight times at the start of each L3B disc. cycle, dividing the 64 refresh intervals into eight segments used to determine the U3B based on DATA_UP.

For example, If the voltages of DATA_LO and DATA_UP are programmed to correspond 000 for the L3B and to 100 for the U3B, respectively, M1 remains on through the fifth U3B disc. point and turns off at the sixth U3B disc. point of $T_{REF(40)}$. M2 is activated for only one refresh interval in each L3B disc. cycle, specifically at $T_{REF(0)}$, $T_{REF(8)}$, $T_{REF(16)}$, $T_{REF(24)}$ and $T_{REF(32)}$. As a result, the pixel is charged to the voltage level corresponding to the gray level of 32 as shown in Fig. 1(b).

C. Display Period (T_{DISP})

Pixel maintains the voltage determined during T_{REF} and displays the corresponding gray level during T_{DISP}. After T_{DISP}, the cycle reverts to T_{REF}, and a polarity inversion takes place, repeating the process. The proposed circuit can prevent image sticking in the LCDs through self-refresh with polarity inversion [14].

III. Results and Discussion

We fabricated the proposed circuit and verified the 6-bit depth implementation through measurement. Fig. 3 shows a micrograph of the fabricated circuit, along with a cross-sectional view of an oxide TFT, and its transfer and output curves (W/L = 4μm/6μm) [13]. We employ a dual-gate structure to enhance carrier mobility and reduce the subthreshold swing [15]. The channel length of all TFTs was 6 μm. M1 and M2 had a channel width of 4 μm, while M3 and M4 had a width of 6 μm. C_{ST1} and C_{ST2} were 300 fF and C_{LC} was 1 pF.

Fig. 4 illustrates the measurement results for implementation of 64 gray levels at a driving frequency of 10 Hz. The on and off levels of scan signals were 10 V and and RF_LO during T_{REF}20 V, respectively. T_{REF} was set to 200 μs, and V_{BD} was 1.4 V, taking into account the voltage difference between V_{ON} and V_{OFF}, as well as a voltage margin to accommodate V_{TH} variations. The measured pixel voltages were ranging from $\pm$0.6 V to $\pm$4.38 V, in steps of 0.06 V.

LCDs inherently exhibit nonlinear electro-optical characteristics. By nonlinearly adjusting REF and modulating RF_LO/RF_UP accordingly, gamma correction can be

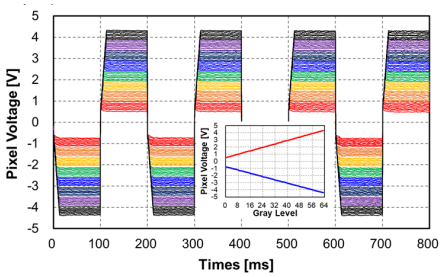

Fig. 4. The measurement results show that the proposed circuit can implement 64 gray levels.

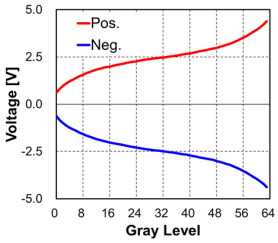

Fig. 5. The simulation results incorporating LCD gamma characteristics with gamma correction.

achieved. This technique has been already reported in integrated TFT data drivers [16], [17] and in column driver ICs [18], [19]. Simulation results confirm that the proposed circuit maintains accurate and stable 6-bit grayscale operation per sub-pixel without requiring additional compensation bits, as shown in Fig. 5. In our previous study, we investigated V_{TH} distribution and reliability using the same fabrication process [13]. For 21 oxide TFTs, V_{TH} ranged from -0.30 V to 0.06 V. Additionally, V_{TH} shifted by 0.004 V and 0.031 V after positive bias stress (PBS) and negative bias stress (NBS) tests conducted for 10,000 seconds, respectively [13]. Reflecting the V_{TH} distribution in V_{BD} determination ensures stable operation as shown in Fig. 2. While a higher V_{BD} improves tolerance to V_{TH} variations, it also increases the signal voltage range and power consumption. Thus, V_{BD} must be optimized considering the V_{TH} distribution.

We calculated the power consumption of the proposed circuit under the same conditions as our previous work [13], achieving a 97.2% reduction compared to conventional 1T1C circuit. The proposed circuit also extends the sub-pixel bit depth from 3-bit to 6-bit, enabling 18-bit RGB color and increasing total colors from 512 to 262,144, increasing by 512 times. Additionally, self-refresh and gamma correction enhance grayscale accuracy while minimizing power.

IV. Conclusion

In this letter, we have proposed a 6-bit MIP circuit utilizing a novel driving scheme, effectively reducing graphics processor power consumption and preventing image sticking through self-refresh. This eliminates the need for frame memory and continuous data processing for static images. The proposed circuit achieves a substantial power reduction of 97.2 % compared to conventional circuit while it enhances grayscale representation by extending the bit depth per sub-pixel from three bits to six bits ultimately achieving an 18-bit color depth.

Acknowledgment

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

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