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RESEARCH ARTICLE

A 1.8-V 95.8-dB SNDR Incremental Delta-Sigma ADC With Analog Noise Reduction Techniques for Sensor ROIC

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ABSTRACT A delta-sigma modulator (DSM)-based incremental analog-to-digital converter (ADC) is proposed for use in the readout integrated circuit of low-power high-resolution sensors. The proposed incremental delta-sigma ADC (IADC) consists of a second-order cascaded-of-integrators feedforward (CIFF) DSM with a successive approximation register (SAR) ADC-based 3-bit quantizer and a digital filter with a cascaded of integrators (CoI) structure. Design techniques to reduce analog noise such as flicker, thermal noise, and nonlinearities in the digital-to-analog converter (DAC) generated by a second-order CIFF DSM with a 3-bit quantizer are introduced and their effectiveness is verified by measured results of the DSM and IADC. In particular, the measurement results confirm that the improvement in the characterization of the flicker noise of the reference driver, including the band-gap reference for generating the reference voltage used in the feedback path of the DSM, determines the overall characterization of the DSM. Furthermore, the proposed low-power high-resolution IADC is implemented using a second-order CoI filter optimized for the designed DSM. The proposed IADC, implemented using a 180-nm CMOS process with a supply of 1.8 V, has an area of 0.296 mm^2 and a power consumption of 124.5 μW. It has an input bandwidth of 500 Hz and a sampling rate of 1 kHz. To implement this, the DSM operating synchronized to an external clock with a frequency of 3.584 MHz has an oversampling ratio of 512 and a sampling rate of 512 kHz. When the differential analog input signal has a frequency of 100 Hz and an amplitude of 0.94 Vpp, the measured peak SNDR of the DSM is about 97.4 dB, while the measured SNDR of the IADC in this case is about 95.8 dB.

INDEX TERMS Delta-sigma modulator, incremental analog-to-analog converter, successive approximation register, flicker noise, thermal noise, band-gap reference, cascaded of integrators.

I. INTRODUCTION

Because low-frequency analog signals such as temperature, humidity, and geomagnetic fields have narrow bandwidths but wide dynamic ranges, readout integrated circuits (ROICs) for sensors that acquire these signals require high-resolution sensor interface circuits [1], [2], [3]. Analog-to-digital converters (ADCs) that convert analog signals to digital signals in low-bandwidth, high-resolution ROICs can be implemented using either successive approximation register (SAR) structures or delta-sigma modulator (DSM)-based structures [4], [5]. SAR ADCs minimize the use of analog blocks, enabling low power ROIC. In particular, the lack of operational amplifiers with high voltage gain in SAR ADCs facilitates the implementation of ROICs in systems-on-chip (SoCs) with other digital blocks, even in submicron processes. On the other hand, the resolution characteristics of the SAR ADC can be mainly determined by the characteristics of the capacitor-based digital-to-analog converter (CDAC), where the linearity of the CDAC limits the resolution of the SAR

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ADC to about 10 to 12 bits. Of course, SAR ADCs can further increase the resolution by applying oversampling and noise shaping techniques, but this increases design complexity, area, and power consumption [6], [7].

ADCs using DSMs typically use operational amplifiers to implement analog integrators, which increases the use of analog circuits compared to SAR ADCs. However, DSM-based ADCs can significantly reduce quantization noise, which inevitably occurs in the form of white noise in the ADC, by applying the oversampling and noise shaping techniques of the DSM and the decimation operations of digital filters. This makes it suitable for implementing high-resolution ADCs because of its structure rather than the individual performance of its component circuits. It is also possible to implement an ADC with a target resolution by adjusting the order of the DSM, the number of bits of the quantizer, and the oversampling ratio (OSR). In addition, incremental delta-sigma ADCs (IADCs) that utilize DSMs can facilitate data conversion for other signals by resetting the DSM after data conversion of one signal. These behavioral features of IADCs make them a good candidate for ROICs that selectively convert analog signals from multiple sensors into digital signals [8]. On the other hand, despite these advantages of DSM-based ADCs, analog noise, such as thermal and flicker noise from analog integrators, including operational amplifiers and reference voltage generators, and nonlinearities in the DACs used due to multibit quantizers, can degrade the characteristics of the DSM. This can make it difficult for delta-sigma ADCs to achieve their theoretical dynamic characteristics, which are determined by the order of the DSM, the OSR, and the number of bits in the quantizer.

In this work, design techniques to eliminate various noises that can be generated by IADCs are presented for the implementation of low-power, high-resolution ADCs for ROICs that acquire low-frequency analog signals. In addition, a 16-bit high-resolution IADC with the introduced design techniques for noise reduction is designed and fabricated. Finally, the effectiveness of the design techniques for noise reduction is analyzed by analyzing the measurement results of the fabricated IADC.

II. INCREMENTAL DELTA-SIGMA ADC

A. BASIC INCREMENTAL DELTA-SIGMA ADC

Figure 1 shows a block diagram of a typical DSM-based incremental ADC that can be used for sensor interfaces, where Fig. 1(a) and (b) are the block diagrams of a second-order cascaded-of-integrators feedforward (CIFF) DSM and a second-order decimation filter, respectively. In the second-order CIFF DSM, the analog input signal and the output of the first integrator are fed directly to the quantizer along with the output of the second integrator to implement the feed-forward path of the CIFF structure. The feed-forward path of the CIFF DSM allows the integrator in the DSM to perform noise shaping only on the quantization error. This has the advantage of reducing the output swing required by

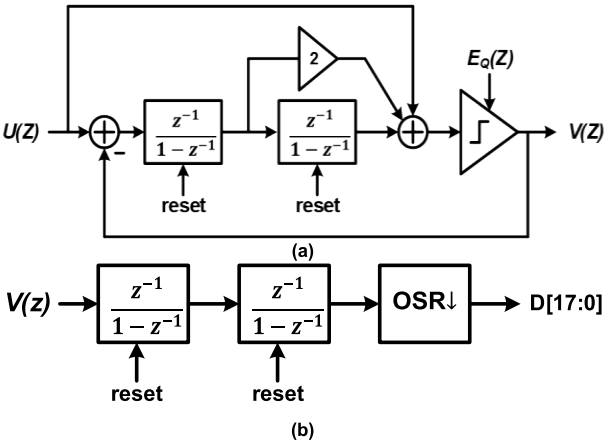

FIGURE 1. Block diagram of IADC (a) second-order CIFF DSM (b) decimation filter.

the integrator in the DSM, which reduces the burden on the integrator design. The output of the DSM appears as a PWM waveform, which is the sum of the input signal and the noise-shaped quantization noise. To obtain the ADC's output from the DSM's output, a decimation filter must be used to remove noise outside the input signal bandwidth. While a conventional delta-sigma ADC's decimation filter must use a complex structure, an IADC that periodically initializes the DSM and decimation filter can use a simple decimation filter. The decimation filter with the cascaded of integrators (CoI) structure shown Fig. 1(b) is implemented as a second-order filter to match the order of the DSM.

The dynamic characteristic of the DSM, SNR, can be expressed as shown in Equation (1), depending on the number of output digital bits (N) of the quantizer used in the DSM, the order (L) of the DSM, and the OSR [9].

$$SNR = 6.02N + 1.76 + 10 \cdot \log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1) \cdot 10 \cdot \log(OSR) \quad (1)$$

While the DSM can improve SNR by significantly reducing the quantization noise $E_Q(z)$ through oversampling and noise shaping techniques, it may not have the ideal SNR characteristics shown in Equation (1) due to noise from multiple analog blocks used in the DSM. Therefore, to implement a high-resolution IADC, it is necessary to analyze the noise generated by the DSM and discuss design techniques to reduce it.

B. NOISE OF DSM

Figure 2 shows the various noise sources in the DSM that can degrade the performance of the IADC. In addition to the quantization noise (E_Q) inherent in the IADC, other noise sources that degrade the SNDR of the DSM include thermal noise, kT/C, due to sampling operations, flicker noise and offset voltage in the integrator, and noise including nonlinearities in the feedback DAC (E_{DAC}). kT/C noise is generated by thermal noise during the sampling process of switched

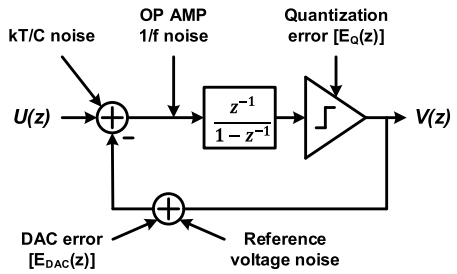

FIGURE 2. Noise sources in DSM.

capacitor circuit. In the DSM, kT/C noise is represented in the form of Equation (2), where k is the Boltzmann constant, T is the temperature, and C_S is the value of the sampling capacitor [10]. It is possible to reduce kT/C noise by increasing the OSR or the value of the sampling capacitor.

$$v_{n\_thermal}^2 = \frac{kT}{OSR \cdot C_s} \tag{2}$$

In order for the DSM to achieve the desired resolution, the magnitude of the kT/C noise must be less than the voltage of 1 least significant bit (LSB) of the IADC, which is calculated by Equation (3) [11]. In this equation, V_P is the magnitude of the analog input signal fed to the DSM.

$$v_{LSB}^2 = \frac{V_P^2/2}{10^{(SNR+3)/10}} \tag{3}$$

From the two equations (2) and (3), the minimum value of the required sampling capacitor of the DSM can be calculated for a given OSR to achieve the targeted resolution of the IADC. In conclusion, the effect of kT/C noise in the DSM can be eliminated by using a sampling capacitor larger than the minimum calculated value.

Flicker noise from the integrator used in the DSM is another factor that can degrade the SNDR of a DSM. Flicker noise is inversely proportional to the frequency and the area of the channel of the transistors used in the operational amplifier for the integrator, as shown in Equation (4), where K is the process constant [12].

$$v_{n\_flicker}^2 = \frac{K}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f} \tag{4}$$

Since the magnitude of flicker noise is inversely proportional to frequency, it affects DSMs for sensor interfaces that receive input signals with low frequencies close to DC. In particular, flicker noise generated in the operational amplifier of the first integrator of the DSM affects the overall SNDR of the DSM. To reduce the effect of flicker noise in the operational amplifier, chopping or auto zeroing techniques can be used [13], [14].

Unlike the quantization noise (E_Q), the noise (E_{DAC}) including reference noise generated by the DAC in the feedback process of the quantization results in the DSM, has a transfer function of the low-pass filter similar to that of the input signal, as shown in Equation (5) [15].

$$V(z) = z^{-1} \cdot [U(z) - E_{DAC}(z)] + (1 - z^{-1}) \cdot E(z) \tag{5}$$

Therefore, the noise generated by the DAC significantly degrades the overall performance of the DSM. In particular, noise in the reference voltage for the DAC has a significant impact on the signal-to-noise and distortion (SNDR) characteristics of the DSM. It has the same effect as noise in the input signal of the DSM, reducing the peak SNDR of the DSM by raising the noise floor of the power spectrum for the output of the entire DSM. It is important to reduce the absolute noise of the reference voltage supplied to the DAC because it is difficult to remove this noise through the structural behavior of the DSM. In addition, the mismatch between each unit-element of a multi-bit DAC, which is required by the use of a multi-bit quantizer in the DSM, introduces nonlinearity, which is a large dominant noise in multi-bit DACs. The nonlinearity caused by mismatches in multi-bit DACs can be reduced by applying data weighted averaging (DWA) techniques to improve the characteristics of the DSM [16].

III. DESIGN OF INCREMENTAL DELTA-SIGMA ADC

This chapter describes the design of a high-resolution DSM-based IADC for sensor ROIC that applies the design techniques presented in Chapter II to reduce various noises in the DSM.

A. ARCHITECTURE OF DSM-BASED IADC

The proposed IADC consists of a second-order CIFF DSM with a 3-bit quantizer and a second-order decimation filter of a CoI structure, as shown in Fig. 3. For the implementation of the CIFF structure, the voltage gains for the analog input signal, the output of the first integrator, and the output of the second integrator are set to 1:2:1, respectively. The use of the 3-bit quantizer in the DSM minimizes the increase in capacitors for integration by setting the coefficients of the

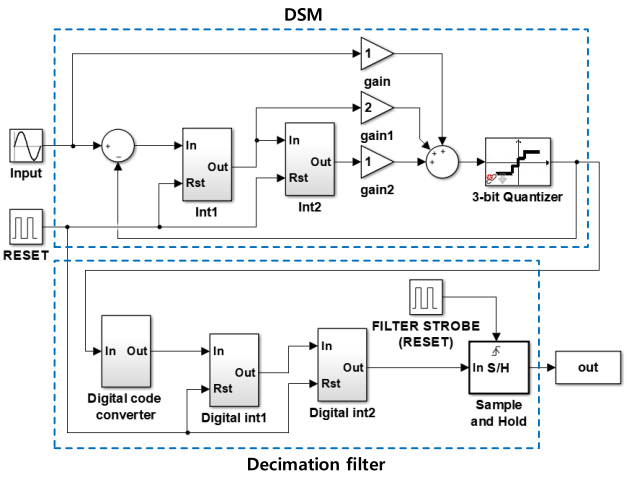

FIGURE 3. Block diagram of proposed IADC.

two integrators to 1. The proposed IADC has a bandwidth of 500 Hz and a sampling rate of 1 kHz for the analog input signal, while the DSM has an OSR of 512 and the DSM and decimation filter are reset to 1 kHz.

B. SECOND-ORDER CIFF DSM

Figure 4 shows the block and timing diagrams of the DSM used for the proposed IADC. The designed DSM has a second-order CIFF structure, consisting of a first integrator with a 3-bit CDAC(C_{S1}), a second integrator, a 3-bit SAR ADC used as a quantizer, and digital logics including the DWA. The first integrator of the DSM uses a chopper that performs chopping at a frequency of 1/2 of the sampling frequency, fs, to reduce the effect of flicker noise in the operational amplifier. In order for the DSM to be used for the IADC, reset switches are added to each integrator to reset the integration capacitors. In addition, a reference voltage generator is used to supply the reference voltage for the 3-bit CDAC and 3-bit SAR ADC and the bias current for the operational amplifier used in each integrator.

The designed DSM is synchronized to an external clock of 3.584 MHz. The DSM operates in the order of sample, data conversion of the 3-bit SAR ADC, and integration, which is repeated through 7 cycles of the external clock. After the DSM finishes sampling, the chopper changes the input and output paths of the integrator, and the DWA is performed to improve the linearity of the 3-bit CDAC.

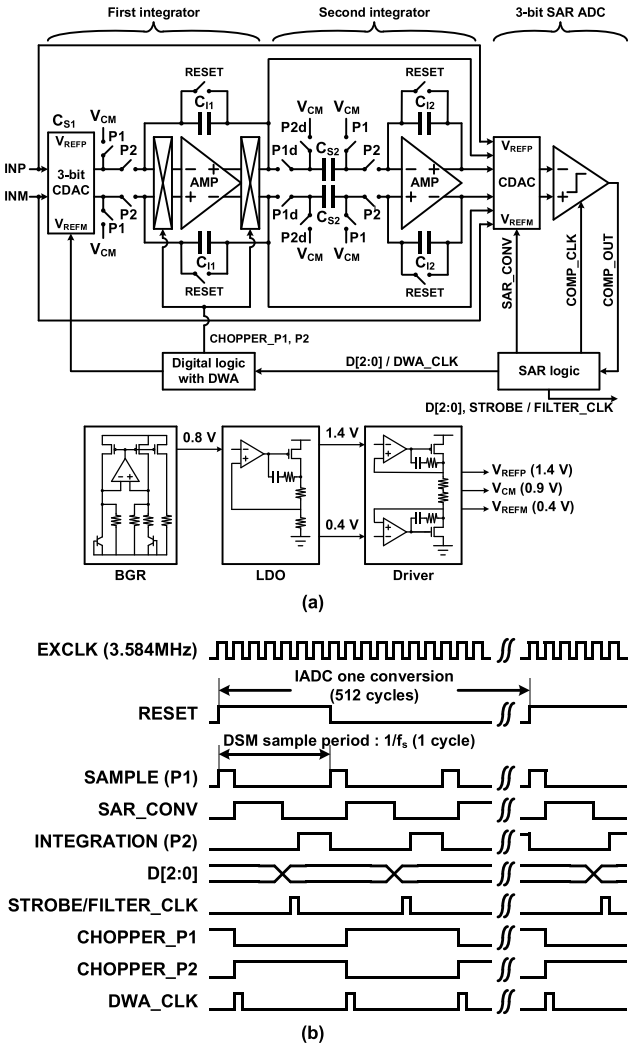

FIGURE 4. Delta-sigma modulator (a) block diagram (b) timing diagram.

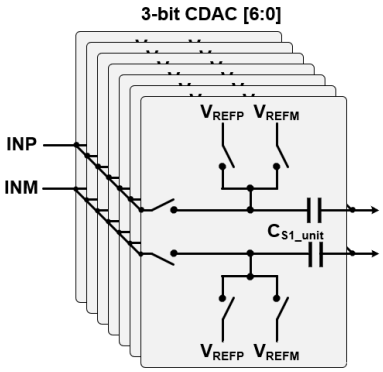

FIGURE 5. Circuit diagram of 3-bit CDAC.

The 3-bit CDAC in the first integrator, shown in Fig. 5, is used as a sampling capacitor for sampling an analog input signal and a CDAC for feedback corresponding to the 3-bit quantization. Therefore, the 3-bit CDAC consists of seven unit-capacitors (C_{S1_unit}), and when it is used as a sampling capacitor (C_{S1}), all seven C_{S1_unit}s are connected in parallel and controlled identically. When it is operated as a 3-bit CDAC for the feedback operation of the DSM, the tops of all seven C_{S1_unit}s are connected to each other, but the bottoms of the C_{S1_unit}s are connected as V_{REFP} or V_{REFM}, respectively, depending on the results of the 3-bit quantizer and DWA. The value of the sampling capacitor can be determined by the calculations in Equations (2) and (3) to reduce the effect of kT/C noise at the input stage of the DSM. A sampling capacitor of at least 1.29 pF is required to realize a DSM characterized by an SNR of 100 dB for an analog input signal with a voltage range of ±500 mV and an OSR of 512. In this work, the value of the sampling capacitor (C_{S1}), which is configured as the 3-bit CDAC, is set to 6.23 pF, which is approximately five times larger than the minimum value required by the design specification, in order to analyze the design technique to reduce the noise of the DSM after the effect of thermal noise of kT/C noise is eliminated.

The design specifications of the operational amplifiers used in the two integrators of the DSM can be determined by the simulation results of the MATLAB behavioral model [17]. In order for the proposed second-order CIFF DSM with a 3-bit quantizer and an OSR of 512 to have an SNDR of more than 100 dB, the operational amplifiers used in the two integrators need to have a voltage gain of more than 50 dB and an output swing voltage of more than ±330 mV.

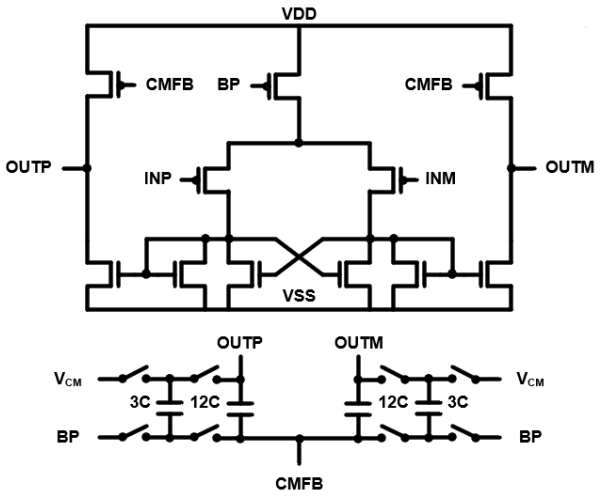

FIGURE 6. Circuit diagram of operational amplifier with CMFB circuit.

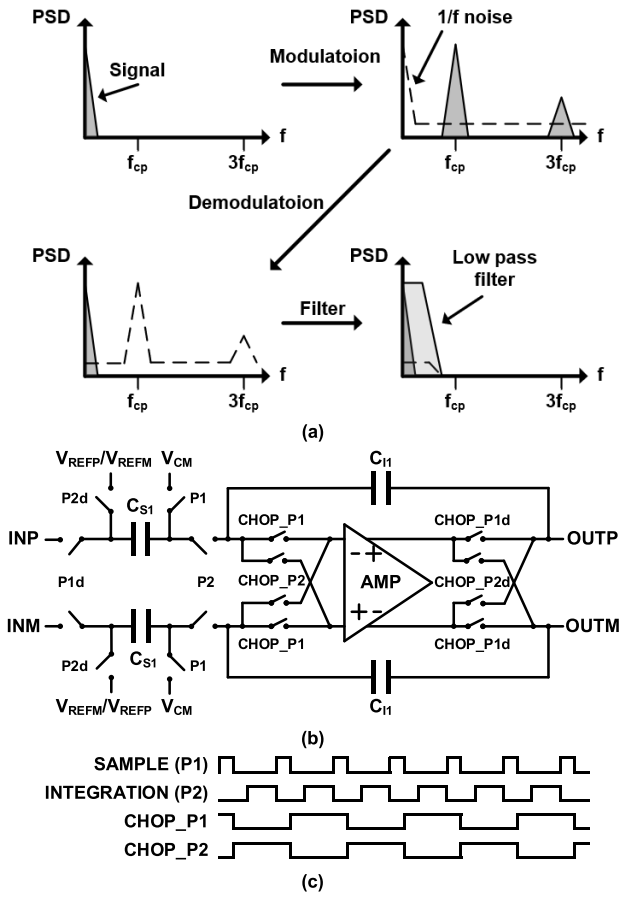

FIGURE 7. Chopping (a) concept (b) block diagram of first integrator with chopper (c) timing diagram for chopping in first integrator.

To realize the required voltage gain, an operational amplifier with a single-stage structure can be used to reduce power consumption and area [18]. However, in this work, a two-stage operational amplifier is used to ensure a margin in the output voltage range of the integrator. Figure 6 shows the block diagram of the operational amplifier with common-mode feedback (CMFB) circuit used for the first and second integrators of the DSM in this work. Due to the increase in the value of the sampling capacitor in the DSM, the integration capacitor of the first integrator also has a value of 6.23 pF. As a result, the operational amplifier of the first integrator drives a large capacitor load, including the sampling capacitor of the second integrator. Since a conventional two-stage operational amplifier using Miller capacitors would have difficulty driving large capacitors, a gain-enhanced current mirror operational amplifier is used in this work [19], [20]. The operational amplifier of the first integrator has a dc gain of 57.3 dB, a gain bandwidth of 21.5 MHz, and a phase margin of 68.3° in the case of a typical process with a 1.8 V supply voltage. Also, the operational amplifier of the second integrator has a dc gain, gain bandwidth, and phase margin of 50.9 dB, 23.1 MHz, and 68.8°, respectively, for the same case.

Figure 7(a) shows the concept of the chopping technique. The chopper improves the SNDR of the DSM by reducing the noise in the input signal band by modulating the flicker noise and offset to the chopping frequency region by periodically cross-switching the input and output of the operational amplifier used in the integrator. To prevent the SNDR of the DSM from being degraded by the flicker noise and offset caused by the operational amplifier, a chopper consisting of a few switches is used on the operational amplifier used in the first integrator, as shown in Fig. 7(b). The chopper used in the DSM performs chopping at a frequency of 256 kHz, which is half the sample frequency of 512 kHz, in order to move noise away from the input signal band. The chopping is performed after the sample operation of the DSM has finished, as shown in Fig. 7(c).

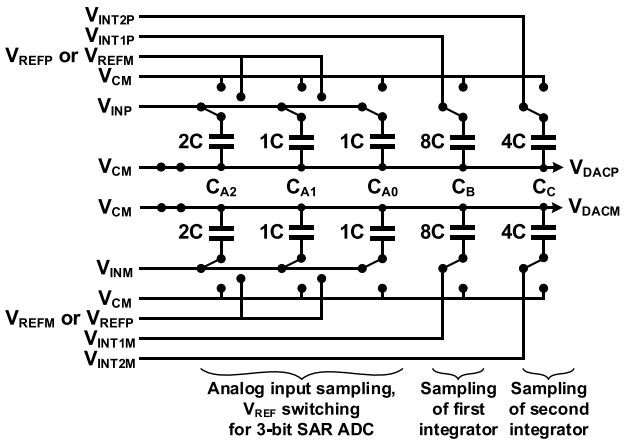

FIGURE 8. Circuit diagram of CDAC for 3-bit SAR ADC.

In this work, the 3-bit SAR ADC is used as the quantizer to increase the dynamic range of the DSM by 12 dB more than when using a 1-bit quantizer [9]. It also increases the integration factor of the DSM, which allows the value of the capacitor for integration to be reduced. The SAR ADC

consists of a CDAC, a comparator, and a SAR logic. The CDAC performs V_{REF} switching for the operation of the 3-bit SAR ADC along with summing the input signal and the outputs of the two integrators to perform the operation of the DSM with CIFF structure. To perform these operations, it consists of a total of 16 unit-capacitors to achieve a voltage gain of 1:2:1 for the analog input signal, the first integrator output, and the second integrator output, as shown in Fig. 8 [17]. For sampling the analog input signal, 4 C_Us of capacitors C_{A2}, C_{A1}, and C_{A0} are used. $8 \cdot C_U$ of C_B and $4 \cdot C_U$ of C_C are used to sum the first integrator output signal and the second integrator output signal.

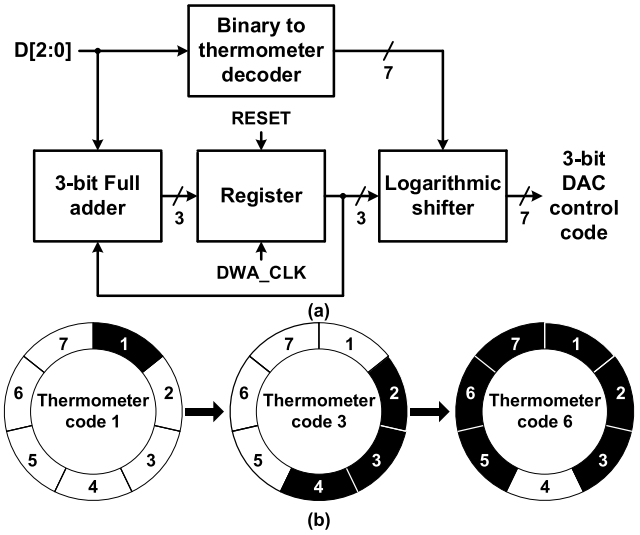

FIGURE 9. DWA (a) block diagram (b) example of unit-capacitor selection of 3-bit CDAC.

On the other hand, by using a 3-bit quantizer, the DSM requires a 3-bit DAC for feedback of the quantizer results. The nonlinearity of the 3-bit DAC worsens the dynamic characteristics of the DSM regardless of the noise shaping performed by the DSM. In this work, the 3-bit DAC is implemented as a CDAC in the first capacitor array shown in Fig. 5, where the mismatch between the seven C_{S1_unit}s worsens the linearity of the 3-bit CDAC. To solve this problem, the DWA technique is applied to the behavior of the 3-bit CDAC. By sequentially selecting the unit capacitors based on the feedback results from the DSM, the DWA averages out the mismatch between the unit capacitors to remove the high-frequency harmonic components contained in the output signal of the DSM. Figure 9(a) is the block diagram of the designed DWA. The DWA consists of a decoder to convert the output of the 3-bit SAR ADC into thermometer code, a full-adder, a register, and a logarithmic shifter. The DWA is operated synchronized at DWA_CLK with a frequency of 512 kHz shown in Fig. 4(b). The current 3-bit data output (D[2:0]) of the SAR ADC and the previous data stored in the register are summed by the 3-bit full adder in the DWA. Based on this value, the DWA is performed with the logarithmic shifter shifting the currently entered thermometer code. The logarithmic shifter receives the data stored in the register and shifts the thermometer code and outputs it. The CDAC receives the output code of the logarithmic shifter and prioritizes the unit capacitors that was not used in the previous integration operation to proceed with the feedback of the DSM. Figure 9(b) shows an example where the thermometer code is rotated by the operation of the DWA to select the unit capacitor. The logarithmic shifter outputs a digital code to select the first unit-capacitor out of 7 unit-capacitors when the initial thermometer code is 1. The next time a thermometer code of 3 is entered, the second through fourth unit capacitors are selected. Finally, the thermometer code of 6 entered causes the logarithmic shifter to select the fifth through seventh unit capacitors and the first through third unit capacitors. This behavior allows the DWA to rotate the control code of the 3-bit CDAC to avoid deteriorating the dynamic performance of the DSM due to the nonlinearity of the DAC.

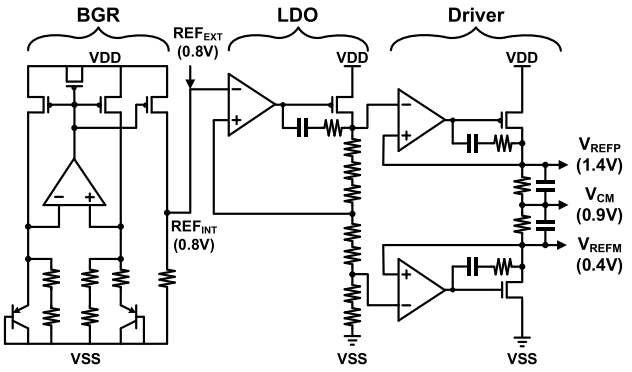

FIGURE 10. Block diagram of reference voltage generator.

Figure 10 is the block diagram of the reference voltage generator that supplies the reference voltage and bias current required for the operation of the 3-bit CDAC, 3-bit SAR ADC, and two integrators. The low-dropout (LDO) circuit of the reference voltage generator produces voltages of 0.4 V and 1.4 V from a voltage of 0.8 V generated by the bandgap reference (BGR) circuit designed in current mode. Then, the driver circuit with analog buffers takes the two output voltages from the LDO circuit and generates V_{REFP}, V_{CM}, and V_{REFM} voltages of 1.4 V, 0.9 V, and 0.4 V to feed into the DSM. Because the reference voltage generator supplies the reference voltage for the DAC to perform feedback, a low-noise design for this block is critical [21]. As mentioned in Chapter II-B, the noise contained in the reference voltage for the 3-bit CDAC has a significant impact on the performance of the DSM, as does the nonlinearity introduced by the 3-bit CDAC. Since the DSM designed in this work operates at low speed, the design of the reference voltage generator is required to reduce noise, including flicker noise. To reduce the flicker noise in the reference voltage generator, there are methods such as using choppers in the operational amplifiers used in the BGR circuit and LDO circuit, or increasing the

Device	Param	Noise Contribution	% Of Total
/I0/M0	fn	8.50206e-06	25.49
/I0/M27	fn	5.43101e-06	10.40
/I0/I3/M10	fn	3.76141e-06	4.99
/I0/I3/M11	fn	3.76121e-06	4.99
/I1/I8/M0	fn	3.18811e-06	3.58
/I1/I8/M9	fn	3.18791e-06	3.58
/I0/I3/M18	fn	3.10965e-06	3.41
/I0/I3/M21	fn	3.10963e-06	3.41
/I0/M1	fn	3.05291e-06	3.29
/I0/I3/M10	id	2.72403e-06	2.62
/I0/I3/M11	id	2.724e-06	2.62
/I1/I8/M1	fn	2.66371e-06	2.50
/I1/I8/M3	fn	2.63124e-06	2.44
/I0/I3/M9	id	2.58459e-06	2.36
/I0/I3/M8	id	2.58455e-06	2.36
/I0/M0	id	2.12994e-06	1.60
/I0/I3/M21	id	2.12938e-06	1.60
/I0/I3/M18	id	2.12934e-06	1.60
/I0/I3/M9	fn	2.08867e-06	1.54
/I0/I3/M8	fn	2.0886e-06	1.54

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 1.68391e-05
Total Input Referred Noise = 0.0338501
The above noise summary info is for noise data

FIGURE 11. Noise simulation results of reference voltage circuit.

area of the circuit affected by flicker noise. In this work, the flicker noise is reduced by increasing the size of the transistor used in the reference voltage generator to avoid using a separate clock signal for the reference circuit.

Figure 11 shows the noise simulation results of the designed reference voltage generator, showing the 20 largest noises in the frequency range of 1 Hz to 500 Hz. Among the noise elements, fn is the flicker noise and id is the thermal noise. The components grouped in blue are noise generated by the MOSFETs used in the BGR circuit, while the components grouped in red are noise generated by the MOSFETs used in the LDO circuit. The noise from the BGR circuit accounts for about 80% of the total noise in the reference voltage generator. Also, the flicker noise accounts for about 80% of the total noise. If all blocks in a DSM are ideally designed except for the reference voltage generator, the noise characteristics of the reference voltage generator determine the overall dynamic characteristics of the DSM. The total summarized noise of the designed reference voltage generator is 1.68391e-5 Vrms. From this value, the value of the SNDR of the designed DSM can be predicted to be approximately 95 dB.

Figure 12 shows the results of the dynamic characteristics obtained by performing a fast Fourier transform (FFT) on a 3-bit binary code obtained through transient noise simulation of the designed DSM. The transient noise simulations of the designed DSM were performed with a sampling rate of 512 kHz to realize an oversampling ratio of 512 for an input band-width of 500 Hz. For these transient noise simulations, the frequency of EX_CLK was determined to be 3.584 MHz. In addition, these transient noise simulations were performed by feeding the DSM a sine wave with a

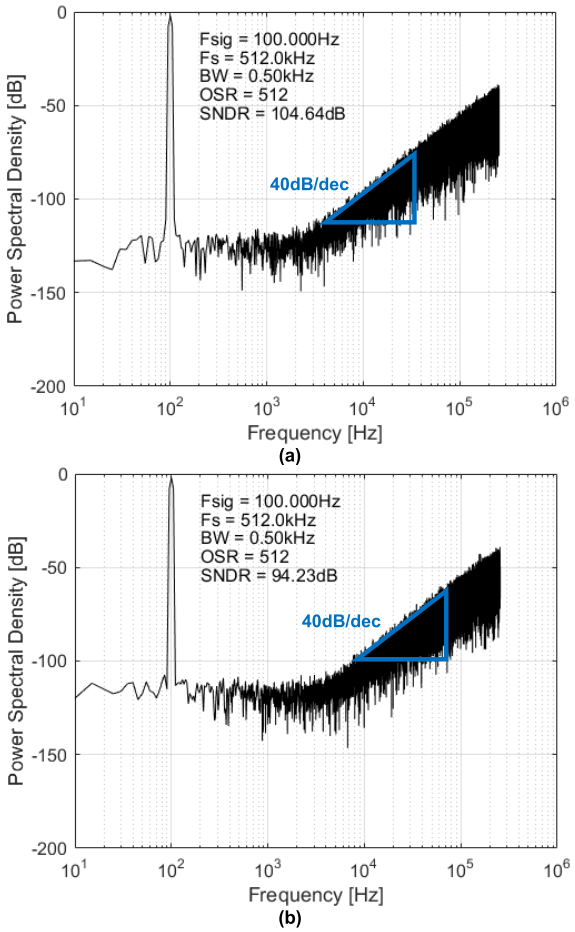

FIGURE 12. Simulated dynamic performance of DSM (a) noise simulation result without reference voltage generator (b) noise simulation result with reference voltage generator.

magnitude of −1.938 dBFS under the conditions of a supply voltage of 1.8 V, a typical process corner, and room temperature. Figure 12(a) shows the result of transient noise simulation of only the core block of the DSM without the reference voltage generator. As the DSM has a second-order structure, it is observed that the quantization noise performs noise shaping with a slope of +40 dB/dec as the frequency increases. In this case, there is no additional noise due to the reference voltage in the feedback process of the DSM, so the kT/C noise of the sampling capacitor becomes the main factor affecting the SNDR. In this design, a sampling capacitor of 6.23 pF is used, which results in a SNDR of 104.6 dB at the in-band of the DSM. The SNDR of the DSM with the reference voltage generator has a dynamic characteristic of 94.23 dB, which is 10.4 dB lower, as shown in Fig. 12(b). This value is similar to the dynamic characteristic of the DSM calculated from the total summarized noise of the reference voltage generator shown in Fig. 10. This shows that the noise characteristics of the reference voltage generator have a significant impact on the overall characteristics of the DSM. As a result, managing the noise generated during the sample process of the input analog signal and the reference voltage

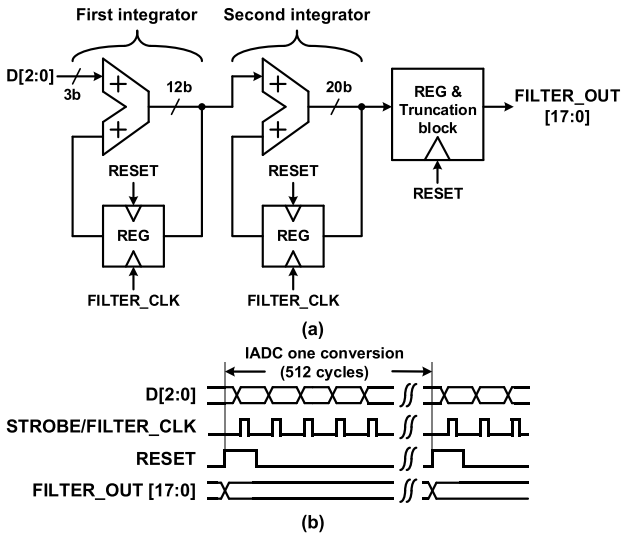

FIGURE 13. Decimation filter (a) block diagram (b) timing diagram.

generation process is very important to improve the dynamic characteristics of the DSM.

C. DECIMATION FILTER

Figure 13 shows the block and timing diagrams of the COI filter used as a decimation filter for the IADC in this work [22]. The decimation filter, which basically consists of a second-order digital integrator, is used to remove noise that has been shifted out of the input signal band by the noise shaping and oversampling performed by the DSM. This ultimately allows the DSM to act as an IADC with improved general dynamic characteristics. The IADC, which combines the DSM and decimation filter, periodically applies a reset operation to the DSM and decimation filter. Due to this reset behavior, the decimation filter does not overflow, so the COI filter, which is a simple structure compared to other filters, can be used as a decimation filter. The designed decimation filter takes D[2:0], which is output synchronously to the STROBE signal with a frequency of 512 kHz from the 3-bit quantizer of the DSM, and generates a 18-bit output code using two digital integrators consisting of an adder and a register. The clock signal for the operation of the digital filter, FILTER_CLK, has a frequency of 512 kHz, which is the same as the frequency of the STROBE signal of the DSM. The IADC requires a reset of the DSM and the decimation filter with an OSR of 512 to perform its operation. For this purpose, a RESET signal with a frequency of 1 kHz is applied to the DSM and the decimation filter, the output of the decimation filter is stored in a register, and the DSM and the decimation filter are initialized.

IV. CHIP IMPLEMENTATION AND MEASUREMENT RESULTS

The proposed IADC is designed and fabricated in 180-nm CMOS process with a supply voltage of 1.8 V. Figure 14 is

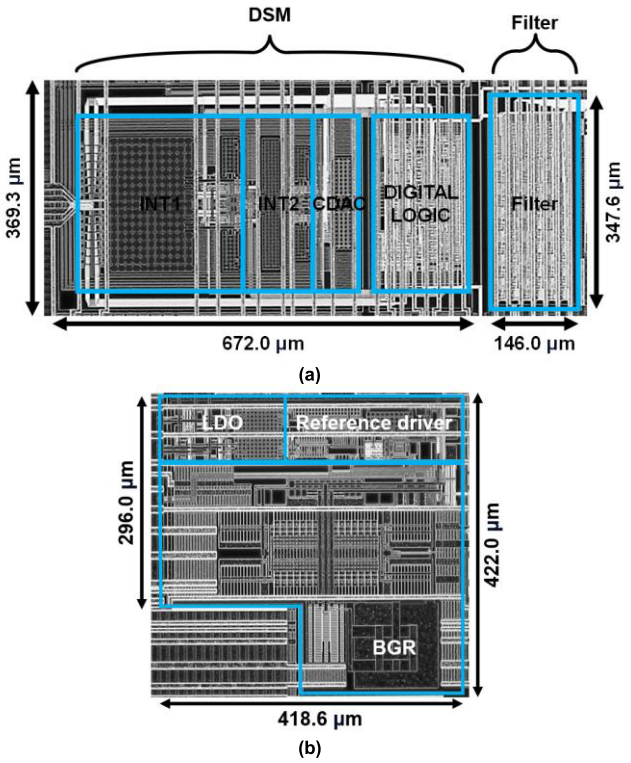

FIGURE 14. Photograph of fabricated IADC (a) DSM and decimation filter (b) reference voltage generator with BGR circuit.

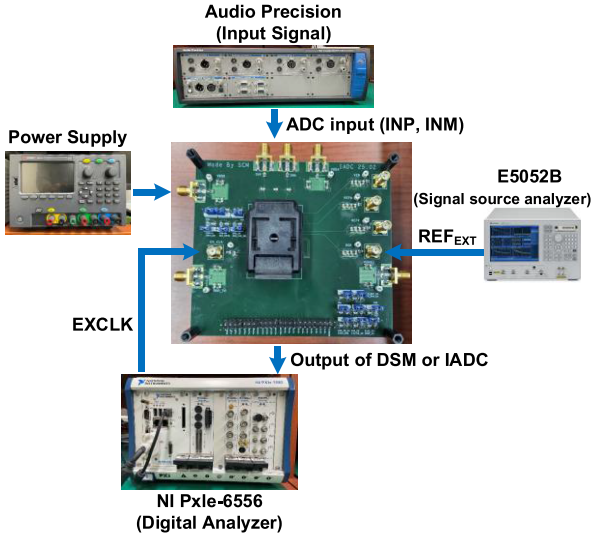

FIGURE 15. Test environment of fabricated IADC.

a chip microphotograph of the fabricated IADC. The IADC basically consists of the DSM and the digital decimation filter, as shown in Fig. 14(a). The DSM and digital decimation filter have an area of 0.245 mm^2 and 0.051 mm^2, respectively. In addition, the reference voltage generator with BGR circuit has been implemented, as shown in Fig. 14(b). The area of the reference voltage generator has been increased for a low-noise design. The power consumption of the incremental

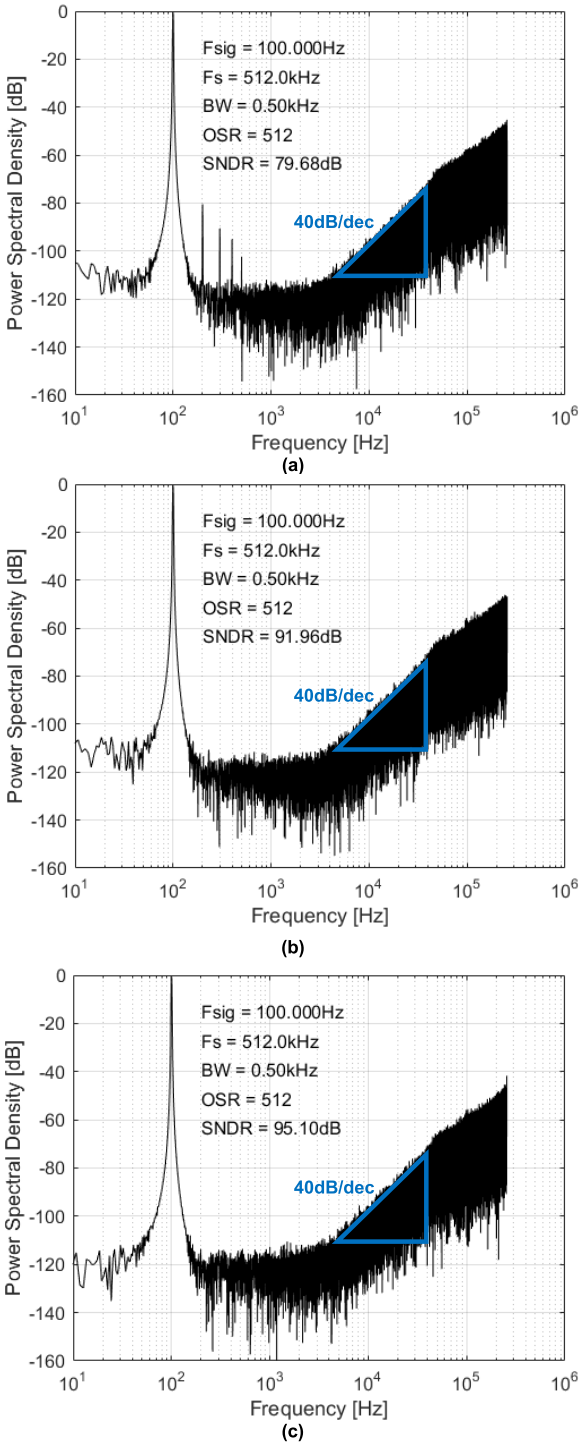

FIGURE 16. Measured dynamic performance of DSM (a) DWA and chopper off (b) DWA on and chopper off (c) DWA and chopper on.

delta-sigma ADC is 124.5 μW total, including the DSM, which consumes 118.4 μW of power. The IADC has a sampling rate of 1 kHz and a bandwidth of 500 Hz of input signal. To achieve this, the DSM and decimation filter are synchronized to an external clock of 3.584 MHz, and the DSM has an OSR of 512.

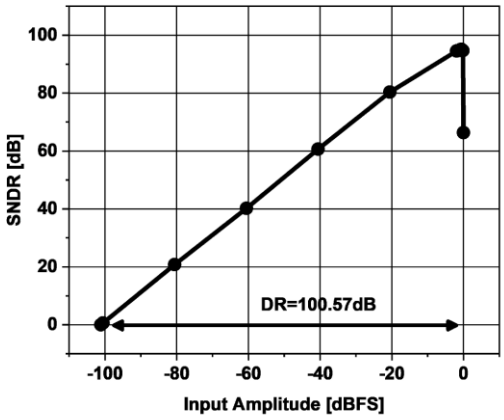

FIGURE 17. Dynamic range of delta-sigma modulator.

Figure 15 shows the measurement environment for evaluating the fabricated IADC. The fabricated chip was mounted via a socket on a printed circuit board on a six-layer FR4 substrate. The Audio precision APX555 supplies the differential analog input signal, and the NI-PXIe-5451 is used to supply the external clock and acquire the digital output data of the DSM and IADC.

Figure 16 shows the measured characteristics of the DSM of the fabricated IADC. The dynamic performance was measured by feeding a sine wave with a frequency of 100 Hz and a magnitude of −0.54 dBFS as the analog input signal. Figure 16(a) shows the dynamic characteristics of the DSM obtained from the power spectrum of the 3-bit output signal of the DSM when both the DWA, which improves the DAC nonlinearity of the DSM, and the chopper of the DSM are disabled. The result of this power spectrum shows an in-band SNDR of 79.7 dB due to the generation of several harmonic components in addition to the input signal. The DWA significantly reduces the harmonic components by improving the nonlinearity of the 3-bit CADC used in the DSM, which improves the SNDR of the DSM to 92.0 dB in-band, as shown in Fig. 16(b). Figure 16(c) shows that the simultaneous use of DWA and chopper improves the dynamic characteristics of the DSM. In particular, it is observed that the use of the chopper improves the noise floor characteristics at low frequencies below 100 Hz. This results in the DSM having an SNDR of 95.1 dB, which is an increase of 3.1 dB over the dynamic characterization improvement by the DWA shown in Fig. 16(b). The DSM of the fabricated IADC has a peak SNDR of 95.1 dB when the magnitude of the analog input signal with a frequency of 100 Hz is −0.54 dBFS, and it has an SNDR of about 0 dB for an input signal with a magnitude of −101.1 dBFS, as shown in Fig. 17. Based on these results, the DSM has a dynamic range of 100.57 dB.

Figure 18 shows the measurement results for the dynamic characteristics of the entire IADC including the decimation filter. The IADC with an OSR of 512 performs the basic operation of an ADC by repeating the process of resetting the DSM and decimation filter after 512 input signal samples

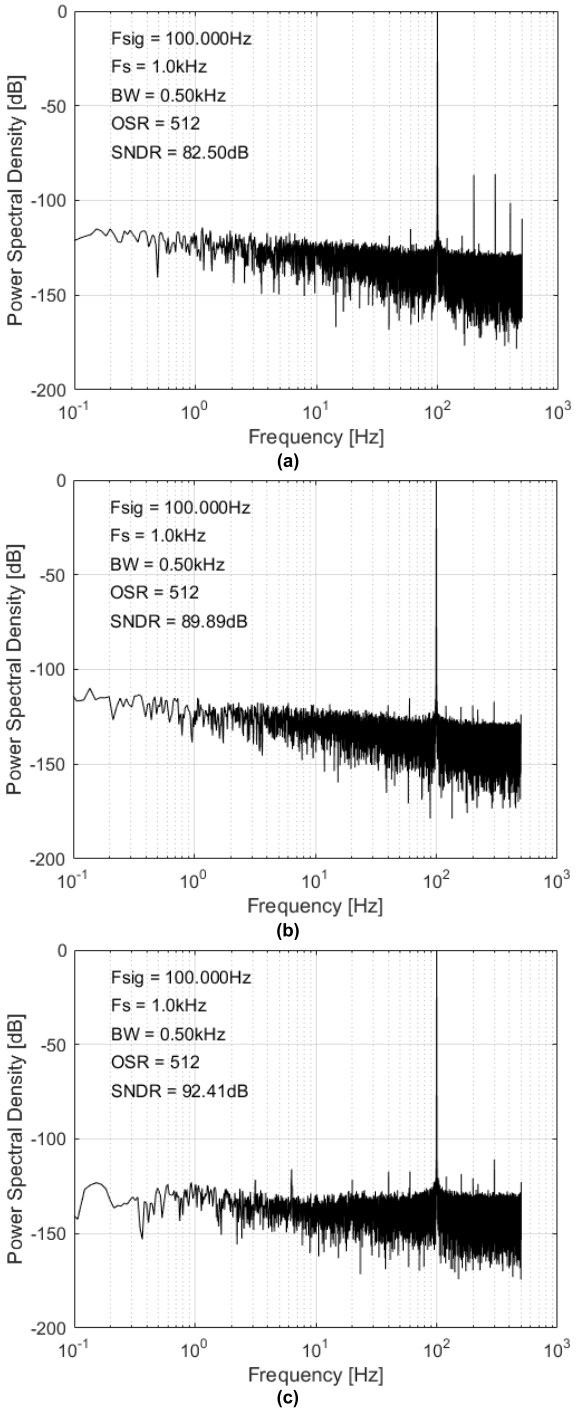

FIGURE 18. Measured dynamic performance of IADC (a) DWA and chopper off (b) DWA on and chopper off (c) DWA and chopper on.

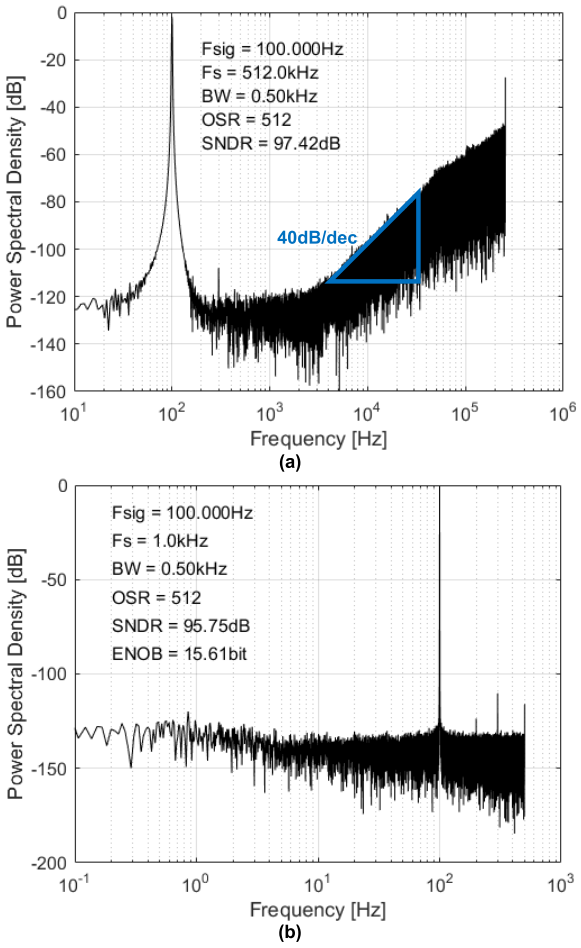

FIGURE 19. Measured dynamic performance with an external reference voltage (a) DSM (b) IADC.

and data conversion. As a result, the IADC has a sample rate of 1 kHz. Therefore, the evaluation of the fabricated IADC was performed by analyzing the power spectrum for an 18-bit digital output code at 1 ksample/s of the IADC under the same measurement conditions as performed in Fig. 16. Figures 18(a) and (b) show the dynamic characteristics of the IADC with and without the application of the DWA in a situation where the chopper used in the DSM is disabled. Similar to the case in Figs. 16(a) and (b), the DWA used in the DSM improves the SNDR characteristics of the IADC from 82.5 dB to about 90 dB. Furthermore, the dynamic characteristic of the IADC is improved to 92.4 dB by the activation of the chopper, as shown in Fig. 18(c).

From the simulated dynamic characteristics of the DSM shown in Chapter III, it was verified that the noise characteristics of the reference voltage generator with BGR circuit determine the dynamic characteristics of the DSM. This is also confirmed by the measurements of the fabricated IADC. Figure 19 shows the dynamic characteristics of the fabricated DSM and IADC using an external reference voltage supplied from the E5052B instrument shown in Fig. 15. The REF_{EXT} of 0.8 V, generated by external equipment rather than the BGR circuitry designed inside the chip, is supplied to the LDO of the reference voltage generator inside the fabricated chip shown in Fig. 10, so that the reference voltages (V_{REFP}, V_{CM}, and V_{REFM}) for the 3-bit CDAC and 3-bit SAR ADC are generated by the driver of the reference voltage generator. In this test condition, the fabricated DSM and IADC are characterized by an SNDR of 97.4 dB and 95.8 dB, respectively.

TABLE 1. Performance comparison and summary of DSMs.

Reference	[23]	[24]	[25]	[26]	[27]	This work	
Process [nm]	180	180	90	65	110	180	
Supply voltage [V]	1.5	1.8	1.2	1.0	1.5	1.8	
Architecture	3rd DSM	3rd DSM	3rd DSM	2nd DSM	2nd DSM	2nd DSM	IADC
Power [μW]	4	340	30	43.5	62.4	118.4	124.5
Sample freq. [MHz]	0.2	3.072	0.25	10	0.512	0.512	0.001
Oversampling ratio	125	64	500	256	128	512	
Bandwidth [kHz]	0.8	24	0.25	19.5	2	0.5	
SNDR [dB]	89.3	96.2	91	88.5	93.9	97.4	95.8
Area [mm^2]	0.75	0.8	0.39	0.04	0.165	0.245	0.296
FoMs [dB]	172.3	174.7	164.8	175.0	169.0	163.7	161.8

$\text{FoMs} = \text{SNDR} + 10 \cdot \log_{10}(\text{BW}/\text{Power})$

It is confirmed that the characteristics of the reference noise still have a great influence on the characteristics of the DSM and IADC, as the noise in the BGR circuit is partially reduced, resulting in an improvement of 2.3 dB of SNDR for the DSM and 3.3 dB of SNDR for the IADC.

Table 1 compares the characteristics of the DSM and DSM-based IADC implemented in this work to other recently published second- or third-order DSMs with relatively low input bandwidth. The DSMs reported in the literature [23], [24] have a third-order architecture and exhibit good FoM characteristics due to their wide input bandwidth. However, the increased area due to the use of the third-order structure of the DSM makes it difficult to realize a small ROIC. In [25], a third-order DSM with a relatively small area was reported, which has similar OSR and input bandwidth to the DSM proposed in this work, but the peak SNDR is only 91 dB. The DSMs reported in the literature in [26] and [27] have a similar structure to the DSM proposed in this work, which is realized in a small area and has a good FoM with low power consumption. The proposed DSM does not have high FoM values due to the application characteristics of low input bandwidth and sampling rate, but they have high SNDR dynamic characteristics. In addition, the second-order CoI filter was implemented along with the DSM including the reference voltage generator to enable the operation of a high-resolution IADC for sensor ROIC.

V. CONCLUSION

The IADC for ROIC of low-power high-resolution sensors has been fabricated in a 180-nm CMOS process using a supply voltage of 1.8 V. The proposed IADC consists of the second-order CIFF DSM with the 3-bit SAR ADC and the reference voltage generator, followed by the second-order CoI digital filter, so it can be used as a full IP with a sensor interface. The simulation and measurement results show that the reference noise for the 3-bit CDAC used in the feedback path of the DSM has a significant impact on the dynamic characteristics of the IADC. In particular, the impact of the reference voltage generator on high-end IADCs and design techniques based on these results are presented. The proposed DSM and IADC with design techniques to reduce various noises generated by the DSM have SNDRs of 97.4 dB and 95.8 dB, respectively, and can be used as an ADC with a resolution of 16 bits. The area and power consumption of the fabricated IADC are 0.296 mm^2 and 124.5 μW, respectively.

ACKNOWLEDGMENT

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REFERENCES

[1] C.-H. Weng, C.-K. Wu, and T.-H. Lin, "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution FoM of 0.65 pJ °C^2," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2131–2139, Sep. 2015.

[2] J. Jun, S. Shin, M. Kim, Y. Ahn, and S. Kim, "A ±0.15% RH inaccuracy humidity sensing system with ±0.44 °C (3s) inaccuracy on-chip temperature sensor," *IEEE Sensors J.*, vol. 21, no. 2, pp. 2115–2123, Jan. 2021.

[3] I. Akita and S. Tatematsu, "3.5 a 4 mW 45pT/√Hz magnetoimpedance-based ΔΣ magnetometer with background gain calibration and short-time CDS techniques," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 62–64.

[4] H. Xin, M. Andraud, P. Baltus, E. Cantatore, and P. Harpe, "A 174 pW–488.3 nW 1 S/s–100 kS/s all-dynamic resistive temperature sensor with speed/resolution/resistance adaptability," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 70–73, Mar. 2018.

[5] H. Hwang, H. Lee, M. Han, H. Kim, and Y. Chae, "A 1.8-V 6.9-mW 120-fps 50-channel capacitive touch readout with current conveyor AFE and current-driven ΔΣ ADC," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 204–218, Jan. 2018.

[6] C.-C. Liu and M.-C. Huang, "28.1 A 0.46 mW 5MHz-BW 79.7dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 466–467.

[7] S. Li, B. Qiao, M. Gandara, D. Z. Pan, and N. Sun, "A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3484–3496, Dec. 2018.

[8] Z. Tan, C.-H. Chen, Y. Chae, and G. C. Temes, "Incremental delta-sigma ADCs: A tutorial review," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4161–4173, Dec. 2020.

[9] J. M. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 1–21, Jan. 2011.

[10] X. Zhang, J. Ma, and Y. Hu, "A high resolution chemical sensing front-end with integrated sigma delta quantisation," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2022, pp. 2831–2835.

[11] S. Pavan, R. Schreier, and G. C. Temes, "Circuit design for discrete-time delta-sigma ADCs," in *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2017, pp. 165–222.

[12] H.-L. Chen, P.-S. Chen, and J.-S. Chiang, "A low-offset low-noise sigma-delta modulator with pseudorandom chopper-stabilization technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 12, pp. 2533–2543, Dec. 2009.

[13] C.-H. Chen, Y. Zhang, T. He, P. Y. Chiang, and G. C. Temes, "A micro-power two-step incremental Analog-to-Digital converter," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1796–1808, Aug. 2015.

[14] R. Wei, W. Wang, X. Xiao, and Q. Chen, "A low-power delta-sigma capacitance-to-digital converter for capacitive sensors," *IEEE Access*, vol. 7, pp. 78281–78288, 2019.

[15] M. De Bock, X. Xing, L. Weyten, G. Gielen, and P. Rombouts, "Calibration of DAC mismatch errors in ΣΔ ADCs based on a sine-wave measurement," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 9, pp. 567–571, Sep. 2013.

[16] B. Wang, S.-W. Sin, S.-P. U., F. Maloberti, and R. P. Martins, "A 550-μw 20-kHz BW 100.8-dB SNDR linear-exponential multi-bit incremental $\Sigma\Delta$ ADC with 256 clock cycles in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1161–1172, Apr. 2019.
[17] J. Kim, N. Jeon, W. Do, E. Jung, H. Kim, H. Park, and Y.-C. Jang, "A 96 dB DR second-order CIFF delta-sigma modulator with rail-to-rail input voltage range," *Electronics*, vol. 13, no. 6, p. 1084, Mar. 2024.
[18] E. Eland, S. Karmakar, B. Gönen, R. van Veldhoven, and K. A. A. Makinwa, "A 440-μW, 109.8-dB DR, 106.5-dB SNDR discrete-time zoom ADC with a 20-kHz BW," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1207–1215, Apr. 2021.
[19] M. Dei, F. Gagliardi, and P. Bruschi, "Slew-rate enhancement techniques for switched-capacitors fast-settling amplifiers: A review," *Chips*, vol. 3, no. 2, pp. 98–128, Apr. 2024.
[20] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140-μW 88-dB audio sigma-delta modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.
[21] Y.-G. Kim, M.-H. Cho, K.-D. Kim, J.-K. Kwon, and J. Kim, "A 105.5 dB, 0.49 mm^2 audio delta-sigma modulator using chopper stabilization and fully randomized DWA," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2011, pp. 1–4.
[22] J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental $\Delta\Sigma$ converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 5, pp. 678–690, Jan. 2004.
[23] M. Zhao, Y. Zhao, H. Zhang, Y. Hu, Y. Bao, L. Ye, W. Qu, and Z. Tan, "A 4-μW bandwidth/power scalable delta–sigma modulator based on swing-enhanced floating inverter amplifiers," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 709–718, Mar. 2022.
[24] R. S. A. Kumar, N. Krishnapura, and P. Banerjee, "Analysis and design of a discrete-time delta-sigma modulator using a cascoded floating-inverter-based dynamic amplifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3384–3395, Nov. 2022.
[25] A. Boni, L. Giuffredi, G. Pietrini, M. Ronchi, and M. Caselli, "A low-power sigma-delta modulator for healthcare and medical diagnostic applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 207–219, Jan. 2022.
[26] A. Matsuoka, T. Nezuka, and T. Iizuka, "Fully dynamic discrete-time $\Delta\Sigma$ ADC using closed-loop two-stage cascoded floating inverter amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 944–948, Mar. 2022.
[27] J.-H. Han, K.-I. Cho, H.-J. Kim, J.-H. Boo, J. S. Kim, and G.-C. Ahn, "A 96dB dynamic range 2 kHz bandwidth 2nd order delta-sigma modulator using modified feed-forward architecture with delayed feedback," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 5, pp. 1645–1649, May 2021.

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